IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Intel Corporation
Petitioner

v.

Qualcomm Incorporated
Patent Owner

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IPR2018-01334[1]
U.S. Patent No. 8,838,949

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**PETITIONER'S REPLY**

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

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# I. INTRODUCTION

In its Petitions, Intel Corporation ("Petitioner") explained in detail how each challenged claim is invalid in view of Bauer in combination with Svensson (for claims 1-15 and 22-23), or alternatively, in view of the combination of Bauer and Svensson with one or more of Kim (for claims 1-23), Zhao (for claims 16 and 17), and Lim (for claims 18-21). And after considering the arguments that Qualcomm Incorporated ("Patent Owner") advanced in its Preliminary Responses, the Board found that Petitioner had established a reasonable likelihood that the challenged claims are invalid, and instituted *inter partes* review on all challenged grounds.

In its Response, Patent Owner just repeats many of the same arguments that it previously raised in its Preliminary Responses, and that the Board considered and rejected in its Institution Decisions. Those arguments should be rejected again here, along with Patent Owners new arguments, none of which has merit.

***First***, for many of its arguments, Patent Owner rests on proposed claim constructions for certain terms (e.g., "system memory," "hardware buffer," "scatter loader controller") that are inconsistent with the terms' plain meanings and find no support in the intrinsic record. Patent Owner cannot avoid invalidity based on such improper attempts to re-write the claims.

***Second***, Patent Owner argues that a POSITA would not have been motivated to combine the asserted prior art references, including Bauer and Svensson. But as

explained in the Petitions, and as the Board recognized in its Institution Decisions, compelling record evidence demonstrates that such a motivation existed—including because Bauer and Svensson share the same inventors and much of the same disclosure, and Bauer ***explicitly references*** Svensson as disclosing a program loader that can read and process information contained in Bauer's disclosed file format. Ex. 1009 at [0031].

***Finally***, Patent Owner argues that, even if combined, the references still fail to teach certain limitations of the challenged claims. As an initial matter, however, many of those arguments hinge on the untenable proposed constructions referenced above—and should be rejected for that reason alone. Moreover, Patent Owner's remaining arguments largely rely on attempts to restrict the prior art references in a manner that simply cannot be squared with the express disclosures of the references themselves. As Intel's expert, Dr. Bill Lin, has confirmed, when considered from the perspective of a person of ordinary skill in the art (POSITA), the asserted prior art references teach all limitations of the challenged claims.

In sum, because Patent Owner has failed to rebut Petitioner's compelling evidence establishing that each challenged claim is invalid, the claims should be found unpatentable and cancelled.

## II. PATENT OWNER'S PROPOSED CONSTRUCTIONS SHOULD BE REJECTED

Attempting to avoid the prior art, Patent Owner proffers constructions that effectively seek to re-write—and narrow—the scope of the challenged claims. Because none of those proposed constructions is grounded in the intrinsic record or otherwise consistent with the broadest reasonable interpretation of the terms, each should be rejected. *See* 37 C.F.R. § 42.100(b).[2]

### A. "System Memory"

Patent Owner asserts that the term "system memory" in independent claims 1, 10, 16, 18, 20, and 22 (and dependent claims 2, 4, 5, 8, and 12) should be interpreted to mean "memory that is addressable by the secondary processor." POR at 9. Petitioner did not ask to construe this term, the Board found it unnecessary in its Institution Decisions to construe this term, 1334 DI at 8; 1335 DI at 15; 1336 DI at 8, and Patent Owner itself did not seek a construction of "system memory" in the district court or ITC litigations. *See* Ex. 1008; Ex. 1024. Nevertheless, to the extent to Board decides to construe this term, Patent Owner's proposed construction should be rejected for two reasons.

[2] Because the Board only applies the *Phillips* standard to IPR petitions filed on or after November 13, 2018, that standard does not apply here.

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