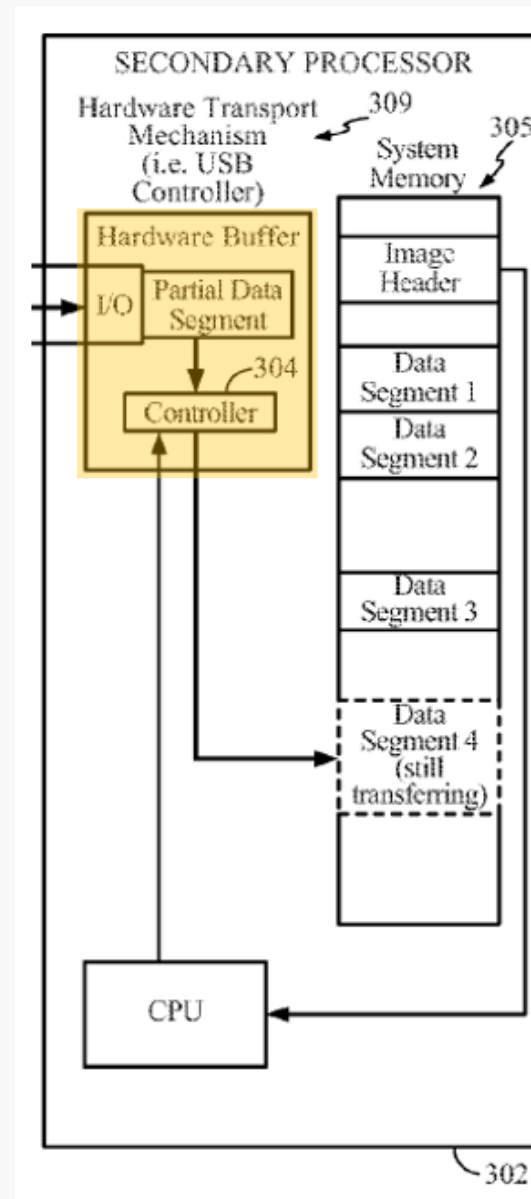# Intel Corporation
v.
Qualcomm Incorporated

IPR2018-01334

U.S. Patent No. 8,838,949

**Patent Owner's Demonstrative
Exhibits for Oral Argument on Remand**

U.S. Patent No. 8,838,949 – Claim 1

. A multi-processor system comprising:

secondary processor comprising:

system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and

a scatter loader controller configured:

to load the image header; and

to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;

primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and

n interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.

SECONDARY PROCESSOR

Hardware Transport Mechanism (i.e. USB Controller) — 309

System Memory — 305

Hardware Buffer

I/O | Partial Data Segment

— 304

Controller

Image Header

Data Segment 1

Data Segment 2

Data Segment 3

Data Segment 4 (still transferring)

CPU

— 302

Ex. 1001 at Fig. 3; 12:60-13:10.

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The Federal Circuit's Opinion

First, because every buffer in our (physical) world is ultimately implemented on a physical device (*i.e.*, hardware), a "hardware buffer" must mean something more than just a "buffer implemented in hardware," as Intel urges, or else the word "hardware" would be erased from the claims.

the word "hardware" superfluous.[2] *Second*, because claim 1 requires both a "system memory" and a "hardware buffer," there must be some distinction between those two concepts. *Third*, because claim 2 requires loading the executable software image "directly from the hardware buffer to the system memory of the secondary processor without copying data between system memory locations on the secondary processor," the meaning of "hardware buffer" relates to the ability to move the software image "directly" to the second processor's system memory and to avoid "copying data between system memory locations."

21 F.4th 801, 809-10 (Fed. Cir. 2021).

The Federal Circuit's Opinion (cont'd)

tion of "hardware buffer." What is needed, then, is an analysis of the specification to arrive at an understanding of what it teaches about what a "hardware buffer" is, based on both how it uses relevant words and its substantive explanations.[3] In this crucial respect, the Board fell short in

21 F.4th 801, 810 (Fed. Cir. 2021).

sion about the proper claim construction. We identify some of the deficiencies without suggesting how, if at all, a proper construction will be substantively different from the limited, negative one (excluding "temporary" buffers) that the Board adopted.

Id.

rary). To resolve even that uncertainty requires the kind of additional, substantive understanding discussed above, which seems likely to support an affirmative construction in place of the Board's purely negative one.

Id. at 812.

The Federal Circuit's Opinion (cont'd)

Finally, we note two matters that would benefit from attention on remand. In a trial transcript from the Qualcomm-Apple litigation (a transcript that was before the Board here), a named inventor of the '949 patent testified in some detail about the difficulty of "design[ing] [the] system so the hardware could place the data right where it needed to be." Transcript of Jury Trial Day 2 (Vol. 2B) at 222, *Intel Corp. v. Qualcomm Inc.*, IPR2018-01334, Exhibit No. 2004 (P.T.A.B. Dec. 12, 2019). That testimony may bear on the remand inquiry. Additionally, our cases sometimes speak of hardware and software implementations of computer functions, reflecting a distinction that appears in usage in the field. *See Tomita Techs. USA, LLC v. Nin-*

21 F.4th 801, 812 (Fed. Cir. 2021).

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