UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C. 20436

In the Matter of	
CERTAIN MOBILE ELECTRONIC DEVICES AND RADIO FREQUENCY AND PROCESSING COMPONENTS THEREOF	**Inv. No. 337-TA-1065**

ORDER NO. 28: CONSTRUING TERMS OF THE ASSERTED PATENTS

(March 5, 2018)

The claim terms construed in this Order are done so for the purposes of this Investigation. Hereafter, discovery and briefing in this Investigation shall be governed by the construction of the claim terms in this Order. Those terms not in dispute need not be construed. *See Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms).

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The following abbreviations may be used in this Order:

ALJ	Administrative Law Judge
Compl.	Complainants or Complainants'
Decl.	Declaration
EDIS	Electronic Document Imaging System
IMB	Initial Markman Brief
PMB	Post-Markman "Bullet-Point" Brief
PTO	U.S. Patent and Trademark Office
Resp.	Respondents or Respondents'
RMB	Reply Markman Brief
Tr.	Transcript

I. Introduction

By publication of a notice in the *Federal Register* on August 14, 2017, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted this investigation to determine:

> Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain mobile electronic devices and radio frequency and processing components thereof by reason of infringement of one or more of claims 1–27, 29, 38, 49, 55–60, 67, and 68 of the '936 patent [U.S. Patent No. 8,633,936]; claims 1 and 6–20 of the '558 patent [U.S. Patent No. 8,698,558]; claims 9, 10, 12, 14, and 20–22 of the '658 patent [U.S. Patent No. 8,487,658]; claims 1–8, 10–14, 16, 20, and 22 of the '949 patent [U.S. Patent No. 8,838,949]; claims 1–6, 8, 10, 16, 17, and 31 of the '490 patent [U.S. Patent No. 9,535,490]; and claims 1–3 and 7–14 of the '675 patent [U.S. Patent No. 9,608,675]; and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

82 Fed. Reg. 37899 (Aug. 14, 2017).

Additionally, pursuant to Commission Rule 210.50(b)(1), the Commission ordered:

> Pursuant to Commission Rule 210.50(b)(1), 19 CFR 210.50(b)(1), the presiding Administrative Law Judge shall take evidence or other information and hear arguments from the parties or other interested persons with respect to the public interest in this investigation, as appropriate, and provide the Commission with findings of fact and a recommended determination on this issue, which shall be limited to the statutory public interest factors set forth in 19 U.S.C. 1337(d)(1), (f)(1), (g)(1).

Id.

The complainant is Qualcomm Incorporated ("Qualcomm") of San Diego, California. The named respondent is Apple Inc. ("Apple") of Cupertino, California. The Commission Investigative Staff ("Staff") is also a party to this investigation. *Id.*

Qualcomm subsequently moved to terminate the '658 patent from the investigation based on withdrawal of allegations from the complaint. I granted the motion in an initial determination. Order No. 6 (Aug. 30, 2017), *aff'd*, Notice of Comm'n Non-Review (Sept. 20, 2017).

The parties submitted a Joint Claim Construction Chart (EDIS Doc. No. 629504) identifying claim terms that needed construction.[1] The parties subsequently submitted Initial and Reply Claim Construction Briefs in which they narrowed the number of claim terms to be construction to ten. I held a one-day combined technology tutorial and *Markman* hearing on January 23, 2018, and ordered the parties to submit Bullet-Point briefs the following week. *See, e.g.*, Markman Tr. 1-305.

Qualcomm subsequently moved to terminate claims 9 and 10 of the '558 patent from the investigation based on withdrawal of allegations from the complaint. I granted the motion in an initial determination. Order No. 24 (Feb. 20, 2018). That initial determination remains pending before the Commission.

II. Relevant Law

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim

[1] A copy of the parties' joint chart can be found at Exhibit JDX-1 to Qualcomm's Initial Claim Construction Brief.

language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms." *Id.* at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.*

The specification "is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be . . . the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Phillips*, 415 F.3d at 1317; *see also Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see also Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (i.e., all evidence ~~external~~ to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered.

Phillips, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* at 1317. "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, "if the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid." *Id.*

III. The Asserted Patents

A. U.S. Patent No. 8,698,558

Asserted U.S. Patent No. 8,698,558 is titled, "Low-Voltage Power-Efficient Envelope Tracker." The '558 patent issued on April 15, 2014, and the named inventors are Lennart K. Mathe, Thomas Domenick Marra, and Todd R. Sutton. Qualcomm asserts claims 1, 6-8, and 11-20 of the '558 patent. 82 Fed. Reg. 37899 (Aug. 14, 2017). Claims 1, 6, 8, 12, and 15 are independent claims. *See* '558 patent.[2]

[2] A copy of the '558 patent can be found at Exhibit JX-1 to Qualcomm's Initial Claim Construction Brief. The '558 prosecution history can be found at Exhibit JX-6 to Qualcomm's Initial Claim Construction Brief.

B. U.S. Patent No. 9,608,675

Asserted U.S. Patent No. 9, 608,675 is titled, "Power Tracker for Multiple Transmit Signals Sent Simultaneously." The '675 patent issued on March 28, 2017, and the named inventor is Alexander Dorosenco. Qualcomm asserts claims 1-3 and 7-14 of the '675 patent. 82 Fed. Reg. 37899 (Aug. 14, 2017). Claim 1 is an independent claim. *See* '675 patent.[3]

C. U.S. Patent No. 8,838,949

Asserted U.S. Patent No. 8,838,949 is titled, "Direct Scatter Loading of Executable Software Image From a Primary Processor to One or More Secondary Processor in a Multi-Processor System." The '949 patent issued on September 16, 2014, and the named inventors are Nitin Gupta, Daniel H. Kim, Igor Malamant, and Steve Haehnichen. Qualcomm asserts claims 1-8, 10-14, 16, 20, and 22 of the '949 patent. 82 Fed. Reg. 37899 (Aug. 14, 2017). Claims 1, 10, 16, 20, and 21 are independent claims. *See* '949 patent.[4]

D. U.S. Patent No. 8,633,936

Asserted U.S. Patent No. 8,663,936 is titled, "Programmable Streaming Processor With Mixed Precision Instruction Execution." The '936 patent issued on January 21, 2014, and the named inventors are Yun Du, Chun Yu, Guofang Jiao, and Stephen Molloy. Qualcomm asserts

[3] A copy of the '675 patent can be found at Exhibit JX-2 to Qualcomm's Initial Claim Construction Brief. The '675 prosecution history can be found at Exhibit JX-7 to Qualcomm's Initial Claim Construction Brief.

[4] A copy of the '949 patent can be found at Exhibit JX-4 to Qualcomm's Initial Claim Construction Brief. The '949 prosecution history can be found at Exhibit JX-9 to Qualcomm's Initial Claim Construction Brief.

claims 1-27, 29, 38, 49, 55-60, 67, and 68 of the '936 patent. 82 Fed. Reg. 37899 (Aug. 14, 2017). Claims 1, 10, 19, 29, 38, 49, 55, and 67 are independent claims. *See* '936 patent.[5]

E. U.S. Patent No. 9,535,490

Asserted U.S. Patent No. 9,535,490 is titled, "Power Saving Techniques in Computing Devices." The '490 patent issued on January 3, 2017, and the named inventors are Vinod Harimohan Kaushik, Uppinder Singh Babbar, Andrei Danaila, Neven Klacar, Muralidhar Coimbatore Krishnamoorthy, Arunn Coimbatore Krishnamurthy, Vaibhav Kumar, Vanitha Aravamudhan Kumar, Shailesh Maheshwari, Alok Mitra, Roshan Thomas Pius, and Hariharan Sukumar. Qualcomm asserts claims 1-6, 8, 10, 16, 17, and 31 of the '490 patent. 82 Fed. Reg. 37899 (Aug. 14, 2017). Claims 1, 16, and 31 are independent claims. *See* '490 patent.[6]

F. Level of Ordinary Skill in the Art

Apple addressed the level of ordinary skill in the art in its Ground Rule 7.5 Disclosure of Invalidity Contentions on October 23, 2017.[7] In that disclosure, Apple proposed that one of ordinary skill in the art of the '936 patent would have had "a Master's Degree in Electrical Engineering, Computer Engineering, or in Computer Science combined with at least 2 years of experience in processor architecture or a related field, or alternatively, a Bachelor's Degree in Electrical Engineering, Computer Engineering, or in Computer Science combined with at least 4 years of experience in processor architecture or a related field." *Id.* at 5. For the '949 patent,

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[5] A copy of the '936 patent can be found at Exhibit JX-5 to Qualcomm's Initial Claim Construction Brief. The '936 prosecution history can be found at Exhibit JX-10 to Qualcomm's Initial Claim Construction Brief.

[6] A copy of the '490 patent can be found at Exhibit JX-3 to Qualcomm's Initial Claim Construction Brief. The parties do not seek construction of terms from the '490 patent.

[7] Excerpts of Apple's invalidity disclosure can be found at Exhibit SXM-004 to the Staff's Initial Claim Construction Brief.

Apple proposed that one having ordinary skill in the art would have had "a Master's degree in Computer Science or Computer Engineering with at least two years of experience in multiprocessor systems, or a Bachelor's degree in Computer Science or Computer Engineering with at least two to four years of experience in multiprocessor systems." *Id.* at 197. For the '490 patent, Apple proposed that one of ordinary skill in the art would have had "a Master's degree in Computer Science with at least two years of experience in multiprocessor systems and/or interconnection networks, or a Bachelor's degree in Computer Science with two to four years of experience in multiprocessor systems and/or interconnection networks." *Id.* at 444. Apple's invalidity disclosure did not address the level of ordinary skill for the '558 or '675 patent.

In view of Apple's proposals, I find that one of ordinary skill in the relevant art for each of the asserted patents would have had a Master's degree in Electrical Engineering, Computer Engineering, or Computer Science plus at least two years of relevant experience, or a Bachelor's degree in one of those fields plus at least four years of relevant experience. "Relevant experience," in the context of the asserted patents, refers to experience with mobile device architecture as well as the following:

- '558 patent: transmission and power circuitry for radio frequency devices. *See* '558 patent at Abstract, 1:7-9, 30-31 ("Techniques for efficiently generating a power supply for a power amplifier and/or other circuits are described herein.").
- '675 patent: transmission and power circuitry for radio frequency devices. *See* '675 patent at Abstract, 1:8-10, 35-38 ("The present disclosure relates generally to electronics, and more specifically to techniques for generating a power supply voltage for a circuit such as an amplifier.").

- '936 patent: graphics processing and processor architectures. *See* '936 patent at Abstract, 1:7-8, 53-56 ("The disclosure relates to graphics processing and, more particularly, to graphics processor architectures.").
- '949 patent: multi-processor systems. *See* '490 patent at Abstract, 1:20-21, 1:64-2:3 ("Aspects disclosed in the detailed description include power saving techniques in computing devices. In particular, as data is received by a modem processor in a computing device, the data is held until the expiration of a modem timer. The data is then passed to an application processor in the computing device over a peripheral component interconnect express (PCie) interconnectivity bus.").
- '490 patent: multi-processor systems. *See* '490 patent at Abstract, 1:20-21, 1:64-2:3 ("Aspects disclosed in the detailed description include power saving techniques in computing devices. In particular, as data is received by a modem processor in a computing device, the data is held until the expiration of a modem timer. The data is then passed to an application processor in the computing device over a peripheral component interconnect express (PCie) interconnectivity bus.").

I reserve the right to amend this determination in my final initial determination if new, persuasive information on this issue is presented at the evidentiary hearing.

IV. Construction of Disputed Claim Terms

A. '558 Patent

1. "based on"

The term "based on" appears in asserted claims 1, 6-8, 11-14, 16, and 18-19 of the '558 patent. The parties agree that the term "based on" can be given its plain and ordinary meaning for claims 6, 8, 12-14, 16, and 18-19. *See* Qualcomm PMB at 1; Apple PMB at 1; Staff PMB at 2.

'675 prosecution history (Notice of Allowance of Jan. 27, 2017) at QCAppleITC-00002751 to -2754. In particular, the examiner stated: "Prior art of record fails to disclose determining a single power tracking signal based on a plurality of inphase (I) and quadrature (Q) components of a plurality of carrier aggregated transmit signals being sent simultaneously." *Id.* at QCAppleITC-00002752.

In view of the intrinsic evidence summarized above, the word "single," as used in context of the claim term at issue, indicates a singular value, *i.e.*, only one in number. "Single" should not be construed to include the use of multiple signals, such as two differential signals, as long as the multiple signals are common to multiple transmit signals.

Therefore, I construe the claim term "single power tracking signal" to mean "one (single-ended) power tracking signal."

C. '949 Patent

1. "means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor" (claim 16)

The claim term "means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor" is recited in asserted claim 16 of the '949 patent. The parties agree that this term is a means-plus-function term subject to 35 U.S.C. § 112, para. 6.[10]

Construing a means-plus-function claim term is a two-step process. The first step is to identify the claimed function. The second step is to determine what structure disclosed in the

[10] The '949 patent is subject to the pre-America Invents Act version of 35 U.S.C. § 112. *See* America Invents Act, Pub. L. No. 112-29 § 4(c).

specification, if any, corresponds to the claimed function. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1351-52 (Fed. Cir. 2015). "Structure disclosed in the specification qualifies as 'corresponding structure' if the intrinsic evidence clearly links or associates that structure to the function recited in the claim." *Id.* at 1352. "While corresponding structure need not include all things necessary to enable the claimed invention to work, it must include all structure that actually performs the recited function." *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005).

The parties' positions with respect to this claim term are as follows:

Complainant's Construction	**Respondent's Construction**	**Staff's Construction**
Function: receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor		
Structure: a modem processor, or a controller in the modem processor, and equivalents thereof (*see* '949 Patent at 4:58-5:43, 5:59-6:39, 7:60-10:44, 11:1-10, and Figs. 1-3)	**Structure:** a secondary processor connected to a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof, as described at column 5, lines 35-43, and shown in Figure 3	

All parties agree that the function performed by this claim element is "receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor." Qualcomm proposes that the corresponding structure

disclosed in the specification is "a modem processor,[11] or a controller in the modem processor, and equivalents thereof," whereas Apple and the Staff take the position that the corresponding structure is "a secondary processor connected to a primary processor via [certain specific types of inter-chip communication buses] and equivalents thereof." *See* Qualcomm PMB at 17-19; Apple PMB at 16; Staff PMB at 14.

The parties agree that the corresponding structure includes at least a modem processor or secondary processor, but Apple and the Staff propose that the corresponding structure should also include a primary processor and a bus interface connecting the two processors. Qualcomm argues that including these additional items discounts the embodiment set forth in Figure 4, "which mirrors the recited function verbatim, and which states that it is the secondary or modem processor that performs the claimed function." *See* Qualcomm PMB at 18. Qualcomm cites to two excerpts from the specification in support of its position:

> [A] secondary processor receives, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor . . . .
>
> [T]he secondary processor receives, from a primary processor via the inter-chip communication bus, the at least one data segment.

'949 patent at 10:53-57; 10:62-65.

Qualcomm's argument that the corresponding structure comprises only the secondary or modem processor is not persuasive, inasmuch as Qualcomm's proposal fails to include all structure needed to perform the function agreed-to by the parties. The claim limitation at issue recites a means for receiving an image header (1) at a secondary processor (2) from a primary

[11] The '949 specification uses the terms "secondary processor" and "modem processor" interchangeably. '949 patent at 6:65-66 ("The secondary processor (modem processor 210).").

processor (3) via an inter-chip communication bus. Therefore, all three of these elements must be included in the structure.

With respect to the claimed inter-chip communication bus, the '949 specification teaches:

> The inter-processor communication bus **134** may be, for example, a HSIC bus (USB-based High Speed Inter-Chip), an HSI bus (MIPI High Speed Synchronous Interface), a SDIO bus (Secure Digital I/O interface), a UART bus (Universal Asynchronous Receiver/Transmitter), an SPI bus (Serial Peripheral Interface), an I2C bus (Inter-Integrated Circuit), or any other hardware interface suitable for inter-chip communication available on both the modem processor **110** and the application processor **104**.

JX-004 ('949 patent) at 5:35-43; *see also id.* Figs. 1, 3.

This language is "clearly link[ed]" to the claim 16 function "receiving at a secondary processor, from a primary processor via an inter-chip communication bus." This portion of the specification describes a "primary processor" (application processor **104**), a "secondary processor" (modem processor **110**), and an "inter-chip communication bus" (bus **134**), all of which comprise the corresponding structure associated with the recited function. The teachings of the intrinsic evidence are thus reflected in the construction proposed by Apple and the Staff, but not in the construction proposed by Qualcomm.

Therefore, I construe the claim 16 term "means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor" to be a means-plus-function term subject to 35 U.S.C. § 112, para. 6. The function performed by this claim element is "receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor." The corresponding structure disclosed in the specification is "a secondary processor connected to

a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof."

2. "means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment" (claim 16)

The claim term "means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment" is recited in asserted claim 16 of the '949 patent. The parties agree that this term is a means-plus-function term subject to 35 U.S.C. § 112, para. 6.

Complainant's Construction	**Respondent's Construction**	**Staff's Construction**
Function: receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment		
Structure: a modem processor, or a controller in the modem processor, and equivalents thereof (*see* '949 Patent at 4:58-5:43, 5:59-6:39, 7:60-10:44, 11:1-10, and Figs. 1-3)	**Structure:** a secondary processor connected to a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof, as described at column 5, lines 35-43, and shown in Figure 3	

The parties agree that the function performed by this claim element is "receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment." As with the claim term discussed immediately above, the parties disagree as to the corresponding structure. Qualcomm proposes that the corresponding structure disclosed in the

specification is "a modem processor, or a controller in the modem processor, and equivalents thereof," whereas Apple and the Staff take the position that the corresponding structure is "a secondary processor connected to a primary processor via [certain specific types of inter-chip communication buses] and equivalents thereof." *See* Apple PMB at 21; Staff PMB at 15.

For the reasons discussed above with respect to "means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor," I hereby construe the claim 16 term "means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment" to be a means-plus-function term subject to 35 U.S.C. § 112, para. 6.

Also consistent with my reasons for "means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor," the function performed by this claim element is "receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment." Likewise, I find that the corresponding structure disclosed in the specification is "a secondary processor connected to a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof."

different data precision," a construction that is consistent with the intrinsic evidence set forth in the '936 patent specification and prosecution history.

SO ORDERED.

Thomas B. Pender
Administrative Law Judge

CERTAIN MOBILE ELECTRONIC DEVICES AND RADIO FREQUENCY AND PROCESSING COMPONENTS THEREOF

INV. NO. 337-TA-1065

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **Order No. 28** has been served by hand upon the Commission Investigative Attorney, **Lisa Murray, Esq.** and the following parties as indicated, on MAR 0 6 2018.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
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