

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01334
U.S. Patent No. 8,838,949

PETITIONER'S REPLY BRIEF ON REMAND¹

¹ IPR2018-01335 and IPR2018-01336 have been consolidated with IPR2018-01334, and Petitioner will file this brief only in IPR2018-01334. All citations are to IPR2018-01334 unless otherwise noted.

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I. INTRODUCTION

Patent Owner's construction of "hardware buffer" is tantamount to the negative construction already rejected by the Federal Circuit as "inadequate." *Intel v. Qualcomm*, 21 F.4th 801, 811 (Fed. Cir. 2021). Moreover, Patent Owner fails to show that its construction is necessary to achieve its sweeping, out-of-context assertions about the claimed invention's purpose. Regardless, because the intermediate storage area ("ISA") of Bauer and Svensson is neither a temporary buffer nor part of any "system memory," let alone the claimed system memory, it satisfies either party's construction of "hardware buffer."

II. PATENT OWNER'S CONSTRUCTION OF HARDWARE BUFFER IS INCORRECT.

A. The Intrinsic Evidence Does Not Support Patent Owner's Construction.

Patent Owner's construction is incorrect because the "hardware buffer" can be a temporary buffer as long as it is physically separate from the claimed system memory.

First, the statements that Patent Owner cites as support for excluding all temporary buffers (PO Resp. Br. 5 (citing Ex. 1001, 2:17-55, 4:43-47, 5:31-35, 7:16-30, 9:42-50, 11:17-24)) do not evidence such a purpose. *See* Pet. Op. Br. 7-11. Statements such as "the direct scatter load technique avoids use of a temporary buffer" (PO Resp. Br. 12 (citing Ex. 1001, 4:46-47)) are taken out of context, because they are surrounded by discussion of other specific aspects of using temporary buffers, *see* Pet.

Op. Br. 7-11. It is these specific uses, such as a temporary buffer that stores the entire executable software image, that the '949 specification distinguishes. *Id.*; Ex. 1026 ¶¶ 21-29; Ex. 1027 ¶¶ 8, 30. Further, as discussed in Section II.B, the '949 statements cited by Patent Owner to demonstrate that the “hardware buffer” is necessary for the asserted advance evince at best a general intent to provide a more efficient loading technique but do not call for a permanent, dedicated buffer. *See* Ex. 1027 ¶¶ 7-9.

Second, the '949 specification does not require that the “hardware buffer” be separate from all memory that might be characterized as system memory, as Patent Owner suggests, PO Resp. Br. 6-7. Patent Owner’s construction imports this restriction, contrary to the Board’s finding in its Final Written Decision that the '949 patent “does not foreclose the possibility of implementing a [hardware] buffer in some other system memory.” *See* FWD (Paper 30) at 13; Pet. Op. Br. 6.

Finally, Patent Owner’s attempts to use claim 2 to support its construction also fail. PO Resp. Br. 10-11. Although Patent Owner argues that claim differentiation is not a rigid rule (*id.*, 10), there is a presumption that claim differentiation applies. *Wi-Lan USA, Inc. v. Apple, Inc.*, 830 F.3d 1374, 1391 (Fed. Cir. 2016). Regardless, even Patent Owner concedes that claim 2 is narrower than claim 1. Indeed, while making sweeping assertions across all claims, including claim 1, about the critical objectives achieved by “the elimination of ‘extra memory copy operations’ in system memory,” Patent Owner simultaneously argues that claim 2 is narrower than claim 1 because

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