Nos. 2020-1828, -1867

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

INTEL CORPORATION,

Appellant,

v.

QUALCOMM INCORPORATED,

Cross-Appellant.

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2018-01334, IPR2018-01335, and IPR2018-01336

BRIEF FOR APPELLANT INTEL CORPORATION

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PATENT CLAIMS AT ISSUE

Intel challenges the patentability of claims 1-9, 12, and 16-17 of U.S. Patent No. 8,838,949. Those claims and claim 10 (from which claim 12 depends) are reproduced below.

> **Claim 1.** A multi-processor system comprising:
>
> a secondary processor comprising:
>
> system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and
>
> a scatter loader controller configured:
>
> to load the image header; and
>
> to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;
>
> a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and
>
> an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.

Appx78-79(12:60-13:10).

> **Claim 2.** The multi-processor system of claim 1 in which the scatter loader controller is configured to load the executable software image directly from the hardware buffer to the system memory of the secondary processor without copying data between system memory locations on the secondary processor.

Appx79(13:11-16).

> **Claim 3.** The multi-processor system of claim 1 in which raw image data of the executable software image is received by the secondary processor via the interface.

Appx79(13:17-19).

> **Claim 4.** The multi-processor system of claim 1 in which the secondary processor is configured to process the image header to determine at least one location within the system memory to store the at least one data segment.

Appx79(13:20-23).

> **Claim 5.** The multi-processor system of claim 4 in which the secondary processor is configured to determine, based on the received image header, the at least one location within the system memory to store the at least one data segment before receiving the at least one data segment.

Appx79(13:25-29).

> **Claim 6.** The multi-processor system of claim 1, in which the secondary processor further comprises a non-volatile memory storing a boot loader that initiates transfer of the executable software image for the secondary processor.

Appx79(13:30-33).

> **Claim 7.** The multi-processor system of claim 1 in which the primary and secondary processors are located on different chips.

Appx79(13:34-36).

> **Claim 8.** The multi-processor system of claim 1 in which the portion of the executable software image is loaded into the system memory of the secondary processor without an entire executable software image being stored in the hardware buffer.

Appx79(13:37-41).

Claim 9. The multi-processor system of claim 1 integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

Appx79(13:42-46).

Claim 10. A method comprising:

receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

rccciving at thc sccondary proccssor, from thc primary proccssor via the inter-chip communication bus, each data segment; and

scatter loading, by the secondary processor, each data segment reedy [sic] to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

Appx79(13:47-67).

Claim 12. The method of claim 10 further comprising loading the executable software image directly from a hardware buffer to the system memory of the secondary processor without copying data between system memory locations.

Appx79(14:3-6).

Claim 16. An apparatus comprising:

means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

means for processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment; and

means for scatter loading, by the secondary processor, each data segment directly to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

Appx79(14:17-37).

Claim 17. The apparatus of claim 16 integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

Appx79(14:38-42).

CERTIFICATE OF INTEREST

Counsel for Appellant Intel Corporation certifies the following:

1. Represented Entities. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

Intel Corporation

2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

Apple Inc.

3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

WILMER CUTLER PICKERING HALE AND DORR LLP: Thomas Anderson

5. Related Cases. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). See also Fed. Cir. R. 47.5(b).

None. This Court has identified the following companion cases: *Qualcomm Inc. v. Intel Corp.*, 20-1587 (Fed. Cir.); and *Intel Corp. v. Qualcomm Inc.*, No. 20-1664 (Fed. Cir.). These cases do not concern U.S. Patent No. 8,838,949.

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None.

Dated: November 16, 2020

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STATEMENT OF RELATED CASES

No other appeal in or from the same proceeding was previously before this or any other appellate court. Qualcomm Incorporated ("Qualcomm") previously asserted U.S. Patent No. 8,838,949 (the "'949 patent") against various Apple Inc. ("Apple") products that contain baseband processors manufactured by Intel Corp. ("Intel") in *Qualcomm Inc. v. Apple Inc.*, No. 3:17-cv-01375 (S.D. Cal.), and *Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof*, Inv. No. 337-TA-1065 (International Trade Commission). Those cases are no longer pending.

This Court has identified the following companion cases: *Qualcomm Inc. v. Intel Corp.*, No. 20-1587 (Fed. Cir.); and *Intel Corp. v. Qualcomm Inc.*, No. 20-1664 (Fed. Cir.). These cases do not concern the '949 patent.

JURISDICTIONAL STATEMENT

Intel appeals from the Board's final written decision in an inter partes review ("IPR"). The Board had jurisdiction pursuant to 35 U.S.C. § 314. The Board entered its final written decision on March 16, 2020, and Intel filed a timely notice of appeal on May 15, 2020. Appx1-65; Appx4581-4584. This Court has jurisdiction pursuant to 28 U.S.C. § 1295(a)(4)(A) and 35 U.S.C. § 141(c).

INTRODUCTION

Intel manufactures baseband processors used in electronic devices. When Intel began supplying its baseband processors to Apple, Qualcomm brought two proceedings against Apple claiming infringement of its '949 patent. Central to Qualcomm's infringement case was Apple's use of Intel's baseband processors—which Qualcomm alleged was the "secondary processor" claimed in the '949 patent. While those proceedings were ongoing, Intel initiated an IPR, naming Intel and Apple as the real-parties-in-interest and challenging all claims of the patent as obvious. The Board found numerous claims of the '949 patent obvious and thus unpatentable, but determined that Intel had not shown claims 1-9, 12, and 16-17 to be unpatentable based on an erroneous understanding of this Court's precedent and the patent. The Court should reverse or vacate and remand on claims 1-9, 12, and 16-17.

The Board's ruling as to claims 1-9 and 12 turned principally on its construction of "hardware buffer"—a term that, as the Board acknowledged, the '949 patent does not define and rarely mentions. Under the broadest reasonable interpretation, "hardware buffer" has the ordinary meaning of a buffer implemented in hardware. The Board agreed with that construction initially, but changed its view in the final written decision on the ground that the patent specification distinguishes the disclosed loading techniques from prior art

techniques that use temporary buffers and thus "hardware buffer" does not encompass the use of a temporary buffer. But the two statements in the specification on which the Board relied do not disavow the use of a temporary buffer with any clarity, as required by this Court. For that reason alone, the Court should vacate the Board's ruling. In any event, if those statements disclaim anything, it is the prior art's copying of an entire software image into a buffer, not the use of a temporary buffer.

Even if the Court were to agree with the Board's construction, the Board's decision as to claims 1-9 and 12 is unsupported by substantial evidence. The Board found that Intel had not shown those claims to be obvious under the Board's construction of "hardware buffer," because the intermediate storage area in Svensson and Bauer is a "temporary buffer." But the only evidence the Board cited for that finding was that the intermediate storage area in those prior art references is reserved at runtime of the program loader to receive information to be transferred to the system memory for later execution. The Board cited no evidence that the intermediate storage area is *deallocated*, to be used for another purpose at a later time, which is necessary to make a buffer "temporary."

The Board also erred in ruling against Intel on claims 16 and 17. Although claims 16 and 17 contain means-plus-function limitations, the '949 patent fails to disclose a corresponding structure, and on that basis, the Board found that Intel had

failed to meet its burden to show unpatentability. As an initial matter, the Board should have reached the unpatentability of claims 16 and 17 despite the lack of a corresponding structure, because as Intel and Qualcomm agreed, it was unnecessary to construe the means-plus-function terms in assessing the claims' validity. Further, to the extent the Board found claims 16 and 17 indefinite, the Board should have declined to find Intel responsible for the patent's failure to disclose a corresponding structure, so that Intel would not be estopped under 35 U.S.C. § 315(e) from challenging those claims in other proceedings. *See Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 948 F.3d 1342, 1353 & n.3 (Fed. Cir. 2020).

Finally, Intel has standing to appeal. Intel suffers injury in fact because it faces a concrete, particularized, and sufficiently imminent risk that Qualcomm would allege infringement or use the '949 patent to constrain Intel's and its customers' actions. Qualcomm has already sued Apple precisely because Apple began using Intel's baseband processors in its devices, and much of Qualcomm's infringement case at trial focused on Intel components, documents, and software.

STATEMENT OF ISSUES ON APPEAL

1. Whether the Board misconstrued the "hardware buffer" limitation recited in claims 1-9 and 12 of the '949 patent.

2. Whether even under the Board's incorrect construction of "hardware buffer," the Board's decision is not supported by substantial evidence.

3. Whether it was necessary for the Board to construe the means-plus-function terms in claims 16 and 17 and, if so, whether the Board should have declined to rule on the merits upon determining that the '949 patent fails to disclose the necessary corresponding structure.

4. Whether Intel has standing to appeal the Board's final written decision regarding the patentability of the '949 patent.

STATEMENT OF THE CASE

A. Multi-Processor Systems

The '949 patent generally relates to multi-processor systems in which software stored in the memory of one processor is loaded to another processor to be executed. Multi-processor systems are common in modern computing devices because they allow each processor to handle different responsibilities. A mobile phone, for example, may include a (1) baseband/modem processor responsible for communicating with a base station, and (2) an application processor responsible for running applications and other computer programs (*e.g.*, email, text messaging, GPS applications). Appx1015-1016; *see* Appx73(1:41-44). The processors communicate with each other by sending data over a "bus," typically a set of wires over which electrical signals are sent. Appx1017.

A processor operates by executing software code that instructs the processor to perform specific operations. Appx1019. "Boot code" instructs the processor to perform certain initialization operations. *Id.* After a processor executes its boot code, it typically executes "program code" that instructs the processor to perform various operations. *Id.* For example, the program code in a baseband/modem processor may instruct it to transfer received data to the application processor so that the user can view the data in an email or other application. *Id.*

Software code is stored in two basic types of memory: non-volatile memory and volatile memory. Appx1020. Non-volatile memory, sometimes called persistent memory, is suitable for long-term storage because it can store code and data regardless of whether power is being applied to the memory. *Id.* Common types of non-volatile memory include flash memory and read-only memory ("ROM"). Appx1021; *see* Appx73(1:51-56).

Volatile memory can store code and other data only when power is being applied to the memory. Appx1020. Volatile memory is suitable for short-term storage and typically allows for code and data to be quickly retrieved from the memory, thereby increasing system performance. Appx1021. Examples of volatile memory include random access memory ("RAM"), dynamic RAM ("DRAM"), and static RAM ("SRAM"). *Id.*

Software code is often packaged and stored in memory as a software file or program called an "executable software image." Appx1022. A software image is typically stored, at least initially, in non-volatile memory before being transferred to volatile memory for execution. Appx1021. Volatile memory to which an executable software image is loaded and from which the loaded image is executed by a processor is often referred to as "system memory." Appx1022.

Executable software images may include (1) a header that contains information about the overall image or the underlying data and (2) a payload consisting of data segments that contain the code or other data used by the image. Appx1022; *see* Appx73(2:14-16); Appx74(4:34-42). For a processor to execute those images, it usually must read the information in the header and then use that information to load the data segments to the proper locations in system memory for execution. Appx1022. One well-known technique for loading an executable image is "scatter loading," which loads or scatters segments of an image into system memory. Appx1023; *see* Appx49 (Qualcomm's expert noting that "'the general concept of scatter loading was known prior to the '949 patent'").

When a multi-processor system is first powered on, one or more processors typically load and execute boot code. Appx1025-1026; Appx73(1:38-44, 51-56). Each processor can store its own boot code. Appx1025. Alternatively, a processor's boot code may be stored in a non-volatile memory coupled to a

different processor to reduce costs and save space. *See* Appx73(2:9-13); Appx1026. In that case, the boot code is retrieved from that other processor's non-volatile memory and loaded into and executed from the receiving processor's system memory. *See* Appx73(2:9-13); Appx1026-1027.

B. Prior Art

Before the '949 patent, multiple prior art references disclosed methods of scatter loading an executable software image from one processor to another processor's system memory in a multi-processor system.

1. U.S. Patent No. 7,356,680 ("Svensson")

Svensson describes a multi-processor system in which data blocks of an image are loaded from a host processor to a client processor. Appx19.

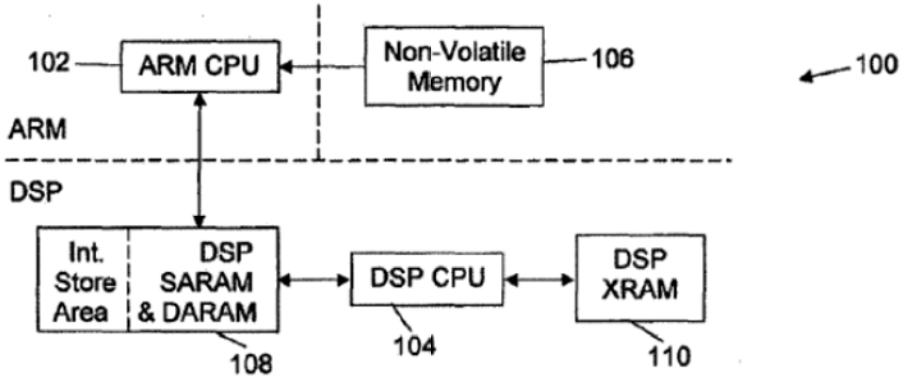


FIG. 1

Appx20; Appx1280; Appx1041.

Figures 1 discloses a device that includes a host processor (ARM CPU 102) coupled to a non-volatile memory (106) and a digital signal processor (DSP)

device. Appx1285(3:49-63, 4:3-5). The DSP device includes a client processor (DSP CPU 104) and internal volatile memory (single-access RAM and dual-access RAM 108), as well as an external RAM (XRAM 110). Appx1285(3:64-4:3); Appx20. A block of memory is reserved within the internal volatile memory (108) as an intermediate storage area. Appx1285(3:64-4:3); Appx20-21.

Svensson discloses a technique for sending data blocks from the host processor to the client processor's XRAM. Appx20. The host processor loads the data blocks from the non-volatile memory to the intermediate storage area in the shared memory, and the client processor then copies the data blocks to final destinations in XRAM. Appx1284(1:11-15, 2:6-20); Appx1285(4:22-26); Appx1286(6:12-15); Appx1042.

Svensson discloses a file format where each transfer block includes a header that indicates the destination address for the block's data. Appx1043. For each transfer block, the client processor reads the header and uses the destination address to load the data to the XRAM. Appx1044.

2. U.S. Publication No. 2006/0288019 ("Bauer")

Bauer is closely related to Svensson and names the same four inventors. Appx1044; Appx1272; Appx1280. Bauer discloses the file format depicted in Figures 1A, 1B, and 1C.

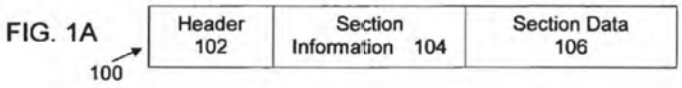


FIG. 1A

FIG. 1B

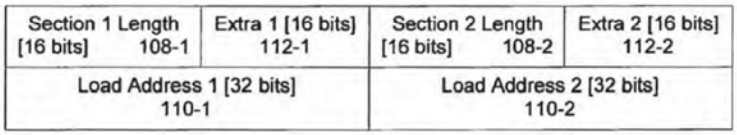


FIG. 1C

Appx1273; Appx22.

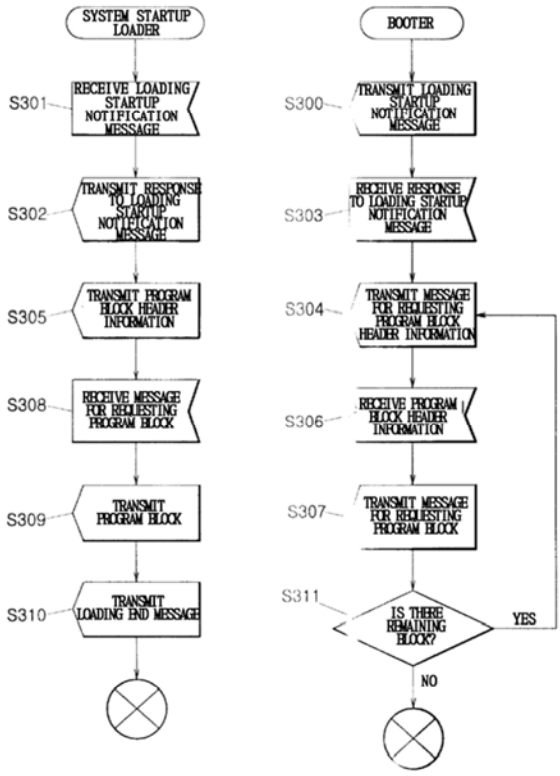
Figure 1A shows the file format for a binary data image 100, which has a header 102, section information 104, and one or more sections of data 106. Appx1277(¶ 32); Appx22. The section information includes the final destination addresses 110 for all the section data. Appx1277(¶ 34); Appx22.

Bauer teaches that this file format (including collecting destination addresses for each data section into one place) can be used in the same multi-processor system described in Svensson, and describes Svensson as an example of a program loader for loading an image with this file format in that same system. Appx23; Appx1276-1277(¶¶ 31, 35-36).

3. Korean Publication No. 10-2002-0036354 ("Kim")

Kim discloses a multi-processor system in which a processor receives program block header information separately, before receiving a corresponding program block, from another processor.

FIG. 3



Appx1318; Appx24.

In step S304, the booter of a secondary processor requests program block header information from a primary processor, which the system startup loader in the primary processor provides S305. Appx1305(5:16-21). When the secondary processor receives the header, it requests a program block S307, which the primary processor provides S309. Appx1305(5:21-24). This process is repeated if there are more blocks to be received. Appx1306(6:2-4).

C. The '949 Patent

Qualcomm owns the '949 patent, which is directed to scatter loading an executable software image from a memory connected to a primary processor (*e.g.*,

application processor) to a memory connected to a secondary processor (*e.g.*, baseband processor). Colloquially, Qualcomm has asserted that the '949 patent claims a way of doing a "flashless boot"—*i.e.*, booting up a secondary processor that does not have its boot code stored in its own flash or other non-volatile memory. Appx6260; Appx6217.

The '949 patent discloses a "primary processor" coupled to a memory that stores an "executable software image for a secondary processor," Appx73(2:63-66), and a "secondary processor" with "a system memory and a hardware buffer for receiving at least a portion of an executable software image," Appx73(2:58-61). The secondary processor also includes "a scatter loader controller for loading the executable software image directly from the hardware buffer to the system memory." Appx73(2:61-63). The only other times the patent mentions a "hardware buffer" outside the claims are in Figure 3 and the explanatory text stating "the executable software image is loaded into the system memory of the secondary processor without an entire executable software image being stored in the hardware buffer of the secondary processor." Appx77(9:37-41).

The '949 patent explains that "one way" of loading a software image from a primary processor to a secondary processor is "to allocate a temporary buffer into which each packet is received," including both "packet header information" and "the payload." Appx73(2:23-28). "From that temporary buffer, some of the

processing may be done over the payload," and the payload or data segments are "copied over to the final destination." Appx73(2:29-31); *see also* Appx73(2:14-16). The patent notes that the "temporary buffer would be some place in system memory, such as in internal random-access-memory (RAM) or double data rate (DDR) memory." Appx73(2:31-34). According to the '949 patent, the problem with this conventional method is that this "extra memory copy operation[]" deters "performance" by increasing "the time required to boot secondary processors in a multi-processor system." Appx76(7:20-30).

The '949 patent purportedly "alleviate[s]" that problem by disclosing scatter loading techniques that "avoid extra memory copy operations." Appx76(7:24-30). The specification notes that in Figure 3, which is described as "exemplary," an "executable software image is loaded into the system memory of the secondary processor without an ***entire executable software image*** being stored in the hardware buffer of the secondary processor." Appx74(4:10-11); Appx77(9:37-41).[1] Instead, the secondary processor processes ***the image header***, and the scatter loader controller on the secondary processor uses the information in the header to transfer data segments directly to their target destination in the system memory of the secondary processor. Appx77(9:21-35). The specification explains:

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[1] All emphases are added unless otherwise indicated.

Thus, conventional techniques employing a temporary buffer for ***the entire image***, and the packet header handling, etc., are bypassed in favor of a more efficient direct loading process. Thus, the exemplary load process of FIG. 3 does not require the intermediate buffer operations traditionally required for loading a software image from a primary processor to a secondary processor. Instead of scatter loading from a temporary buffer holding ***the entire image***, the exemplary load process of FIG. 3 allows for direct scatter load [sic] the image segments to their respective target destinations directly from the hardware to the system memory.

Appx77(9:43-54).

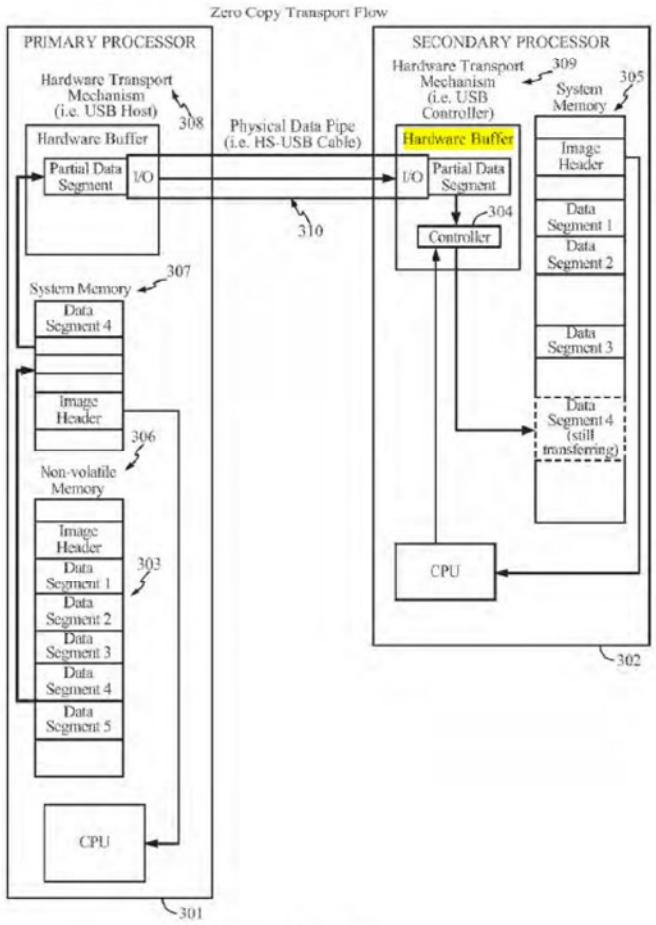

FIG. 3

Appx70 (highlight added).

As relevant to this appeal, independent claim 1 of the '949 patent recites:

> 1. A multi-processor system comprising:
>
> a secondary processor comprising:
>
> system memory and a ***hardware buffer*** for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and
>
> a scatter loader controller configured:
>
> to load the image header; and
>
> to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;
>
> a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and
>
> an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.

Appx78-79(12:60-13:10). Claims 2-9 depend from claim 1. *See* Appx79(13:11-46).

Claim 12, which is similar to claim 2 but depends from independent claim 10, comprises "loading the executable software image directly from a ***hardware buffer*** to the system memory of the secondary processor without copying data between system memory locations," Appx79(14:3-6).

Claim 16 is directed to an apparatus comprising various "means for receiving," "means for processing," and "means for scatter loading"—all "at" or

"by" the "secondary processor." Appx79(14:17-37). Claim 17 depends from claim 16. Appx79(14:38-42).

D. Intel's Sales Of Baseband Processors To Apple

Intel manufactures baseband processors (*i.e.*, modem chips). In 2016, Apple launched a smartphone with baseband processors from Intel, while continuing to purchase baseband processors from Qualcomm for other phones. *See* Appx1007; Appx6247-6251. When Apple started using Intel's baseband processors in its devices, Qualcomm responded by asserting the '949 patent against Apple in two different proceedings, accusing only those Apple devices that incorporate Intel's chips of infringement.

In July 2017, Qualcomm sued Apple for infringement of the '949 patent and other patents in the Southern District of California. Appx6240. Qualcomm also requested that the International Trade Commission ("ITC") initiate an investigation of Apple's allegedly unfair trade practice and exclude certain Apple devices that incorporate Intel's baseband processors from entering the United States, allegedly because those devices infringe the '949 patent. *See* Appx6223. The real target of Qualcomm's actions was clear: Apple explained in one of its filings that "Qualcomm is selectively asserting its patents to target only Apple products containing Intel chipsets" to "force Apple to choose Qualcomm as a supplier instead of Intel." Appx6233-6234.

Although Qualcomm eventually dropped the '949 patent from the ITC action, it proceeded to trial on that patent in the Southern District of California. To show infringement, Qualcomm's expert relied extensively on Intel components, documents, and software. *E.g.*, Appx6256-6257; Appx6261-6262; Appx6266-6267. On March 15, 2019, the jury found that the accused Apple devices containing Intel baseband processors infringed claims 1 and 2 of the '949 patent and awarded more than $9 million in damages. Appx6277; Appx6279.

In April 2019, Qualcomm and Apple reached a confidential settlement agreement that dismissed "all litigation between the two companies worldwide." Mot. to Dismiss 4 (ECF No. 21). Intel is not a party to the agreement and not privy to its details, but Qualcomm's SEC filing reported that Qualcomm "entered into a six-year global patent license agreement with Apple, effective as of April 1, 2019" and that its financial "results for the third and fourth quarters of fiscal 2019 included royalties from Apple and its contract manufacturers for sales made in such quarters." Appx6210.

In July 2019, Intel sold most of its smartphone modem business to Apple. Appx6205. But Intel has not yet exited the baseband processor market. *Id.* It has continued and will continue to supply baseband processors to Apple for prior versions of the iPhone that Apple continues to sell. *Id.* Intel also has sold and

continues to sell baseband processors to another customer that integrates those processors into components for use in cellular-enabled computers. *Id.*

E. Inter Partes Review

While Qualcomm's actions against Apple were pending, Intel initiated an IPR in July 2018, naming Intel and Apple as the real-parties-in-interest and challenging all claims of the '949 patent as obvious under 35 U.S.C. § 103 (2011).[2] As relevant to this appeal, Intel argued that claims 1-9 and 12 were obvious over Bauer, Svensson, and Kim, and that claims 16 and 17 were obvious over Bauer, Svensson, Kim, and Zhao.[3] Appx2-3. The Board determined that claims 1-9, 12, 16, and 17 were not unpatentable, but agreed with Intel that claims 10, 11, 13-15, and 18-23 were obvious in light of the prior art and therefore unpatentable. Appx63-64.

As to claims 1-9 and 12, the Board found that Intel had not proven obviousness based on the Board's construction of "hardware buffer." Appx10-17; Appx55-56. Intel argued that "hardware buffer" should be given its ordinary meaning—*i.e.*, '"a buffer implemented in hardware."' Appx11-12. The Board initially agreed with Intel in its institution decision, noting that "Svensson and

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[2] This case is governed by the pre-America Invents Act versions of 35 U.S.C. §§ 103 and 112, ¶ 6.

[3] Zhao is patent application publication US 2007/0140199 A1, published on June 21, 2007. *See* Appx1321-1343. Because the Board did not address Zhao in its final written decision, Intel does not provide background on that patent.

Bauer's intermediate storage area teaches a 'hardware buffer' because [t]he intermediate storage area of Bauer and Svensson is a buffer used to store data destined for another memory, and the intermediate storage area is in hardware." Appx11 (quotation marks omitted; brackets in original); *accord* Appx4171.

The Board changed its mind in the final written decision, concluding that "hardware buffer" does not include the use of a "temporary buffer." Appx12-17. The Board acknowledged that claim 1 "does not define what implementation the hardware buffer must take or what type of storage device the hardware buffer is." Appx12-13. The Board also acknowledged while that claim "separately recites a 'system memory,'" that recitation "does not foreclose the possibility of implementing a buffer in some other system memory." Appx13. The Board further noted that the written description mentions "'hardware buffer' only three times" and "does not provide much, if any, guidance on what [it] must be." Appx15.

Nonetheless, the Board gave two reasons for narrowing the scope of "hardware buffer." First, the Board concluded that Intel's proposed construction and the Board's preliminary determination "fail to give meaning to the term 'hardware'" because "all buffers must ultimately be implemented in hardware." Appx14-15 (quotation marks omitted).

Second, the Board noted that the patent "differentiate[s] disclosed loading techniques from known prior art techniques that use temporary buffers to receive data from a primary processor for loading." Appx15. For example, the Board cited the statement in the specification that "'[i]n one exemplary aspect a direct scatter load technique'" is disclosed, which "'avoids use of a temporary buffer.'" Appx15-16 (quoting Appx74(4:43-47)) (brackets in original). The Board also relied on the statement that in "the exemplary device of Figure 1," the patent discloses that the modem processor stores the executable image "'directly into the modem processor RAM … 112 to the final destination without copying the data into a temporary buffer in the modem processor RAM 112.'" Appx16 (quoting Appx75(5:31-35)) (emphasis omitted). The Board thus concluded that "hardware buffer" distinguishes the claims from the prior art and "should not be read so broadly as to encompass the use of a temporary buffer." Appx16-17 (quotation marks omitted).

At the same time, the Board rejected Qualcomm's primary proposed construction of "hardware buffer"—*i.e.*, "'a buffer within a hardware transport mechanism that receives data sent from the primary processor to the secondary processor.'" Appx11; Appx13-14. The Board found that interpretation "problematic," because Figure 3 of the patent, on which Qualcomm relied, is merely "exemplary"—a term the '949 patent defined as "serving as an example,

instance, or illustration" and not necessarily "preferred or advantageous over other aspects." Appx13 (quoting Appx74(4:22-25)) (quotation marks omitted). The Board also explained that "'hardware transport mechanism' itself lacks the kind of specificity that would help" a person of ordinary skill understand the term "hardware buffer." Appx13-14.

As to claims 16 and 17, the Board found them not unpatentable because the patent fails to disclose sufficient corresponding structure, making it impossible to compare the claims to the prior art. Appx62. The Board agreed with Intel that claim 16 contains means-plus-function limitations. Appx17-18; Appx62; *see* 35 U.S.C. § 112, ¶ 6 (2011). But the Board expressed concerns in its institution decision regarding whether the specification disclosed corresponding structure. Appx17. After Intel agreed that the claims fail to disclose sufficient structure to perform the recited functions, the Board turned the failure in Qualcomm's patent back on Intel by holding that Intel "has not met its burden … to show structure corresponding to the claimed function to which [the Board] can compare the prior art's disclosure," and therefore has not shown that claims 16 and 17 are unpatentable. Appx62.

F. Appeal

Intel timely appealed the Board's final written decision, and Qualcomm cross-appealed on the claims that the Board had declared unpatentable. Before

briefing on the merits began, Qualcomm moved to dismiss Intel's appeal for lack of standing. ECF No. 21. Intel opposed, arguing that it readily satisfies the requirements of Article III standing. ECF No. 30. Qualcomm filed a reply. ECF No. 37. On August 27, 2020, the Court denied Qualcomm's motion to dismiss without prejudice and directed the parties to address standing in their merits briefs. ECF No. 46.

SUMMARY OF THE ARGUMENT

The Court should reverse or vacate and remand the Board's decision as to claims 1-9, 12, and 16-17.

1. The Board erred in finding that claims 1-9 and 12 are not unpatentable by construing "hardware buffer" unduly narrowly. Although the Board initially agreed with Intel that "hardware buffer" has the ordinary meaning of a buffer implemented in hardware, the Board limited its construction in the final written decision to exclude the use of a temporary buffer. This was error, and the Board's reasoning to the contrary does not withstand scrutiny.

The Board cited the preference for avoiding surplusage on the ground that the ordinary meaning of "hardware buffer" makes "hardware" redundant (as all buffers are implemented in hardware). But that mere preference yields to the reality of commonplace redundancies where, as here, the patent does not clearly indicate a different meaning. Further, the two statements in the '949 patent

specification on which the Board relied to exclude the use of a temporary buffer do not clearly or unmistakably disavow such use, as required by this Court's precedent. Those statements appear in "exemplary" embodiments, and even if they could be read as limiting, they would disclaim, at most, the copying of an entire image into a temporary buffer.

The Board's narrow interpretation was incorrect, and it certainly was not the broadest reasonable interpretation. Under the correct construction of "hardware buffer," claims 1-9 and 12 would have been obvious over the combination of the prior art.

2. Even under the Board's erroneous construction, claims 1-9 and 12 would have been obvious. The Board determined that Intel had not shown those claims to be obvious because the intermediate storage area in Svensson and Bauer is a "temporary buffer" that does not teach a "hardware buffer." But that finding is unsupported by substantial evidence. The only reason the Board gave was that the intermediate storage area in Svensson and Bauer is allocated or reserved at runtime of the program loader to receive information to be transferred to the actual system memory for later execution. But there is no evidence—and the Board has cited none—that suggests the intermediate storage area in those prior art references is *deallocated* so that it could be used later for another purpose, which is necessary to make a buffer temporary. To the contrary, Svensson indicates that the intermediate

storage area is not deallocated and therefore is permanent. Thus, the Board's decision as to claims 1-9 and 12 cannot stand.

3. As to claims 16 and 17, the Board should have assessed their unpatentability despite the lack of a corresponding structure for certain means-plus-function limitations because as Intel and Qualcomm agreed, assessing the claims' validity does not depend on construing those means-plus-function terms. To the extent the Board found claims 16 and 17 indefinite, the Board should have declined to reach a decision on the merits, rather than find that Intel had not met its burden to show unpatentability. This Court has instructed the Board to decline to reach the merits of an unpatentability challenge where the patent fails to disclose a corresponding structure, recognizing that the inability to compare the prior art to the disclosed structure is due to the patentee's failure, not the challenger's. That approach prevents an IPR petitioner from being unfairly estopped under 35 U.S.C. § 315(e) from challenging the relevant claims in the future. The Board improperly disregarded this caselaw in holding Intel responsible for the patent's failure.

4. Intel readily satisfies the injury-in-fact requirement of Article III standing because it suffers a concrete, particularized, and sufficiently imminent injury in the form of a potential infringement allegation by Qualcomm or, at the least, Qualcomm's use of the '949 patent to constrain Intel's and its customers' actions. When Qualcomm sued Apple for using Intel's baseband processors, its

proof of infringement focused extensively on Intel components, documents, and software. That creates a sufficient threat that Qualcomm would accuse Intel of infringement. Indeed, Qualcomm's argument that it has not sued Intel, specifically, or that Apple's devices contained components other than Intel's baseband processor does not mitigate the risk because Qualcomm has already mapped the asserted claims onto Intel's processor and its functions in the case against Apple.

Further enhancing Intel's injury, Qualcomm has refused to provide a covenant not to sue to Intel despite its settlement with Apple and will likely argue that Intel is estopped from challenging the relevant claims of the '949 patent. Contrary to Qualcomm's argument, this Court does not require further proof of how Intel would infringe the relevant claims of the '949 patent. Finally, this case presents a strong basis for recognizing competitive standing because the Board's decision changed the competitive landscape by favoring Qualcomm's position in the baseband processor market over Intel's.

ARGUMENT

I. STANDARD OF REVIEW

The Board's "[c]laim construction based solely upon intrinsic evidence, as is the case here, is a matter of law reviewed de novo." *Hamilton Beach Brands, Inc. v. f'real Foods, LLC*, 908 F.3d 1328, 1339 (Fed. Cir. 2018). Because the petitions

for IPR in this case were filed before November 13, 2018, the claims are given the broadest reasonable construction in light of the specification. *Game & Tech. Co. v. Wargaming Grp. Ltd.*, 942 F.3d 1343, 1351 (Fed. Cir. 2019); Appx8-9. The Court reviews *de novo* the Board's "ultimate determination of obviousness and compliance with legal standards," and reviews "underlying factual findings for substantial evidence." *Pride Mobility Prods. Corp. v. Permobil, Inc.*, 818 F.3d 1307, 1314 (Fed. Cir. 2016). The underlying factual findings include "'the scope and content of the prior art.'" *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1039 (Fed. Cir. 2017). "'Substantial evidence is something less than the weight of the evidence but more than a mere scintilla of evidence.'" *Id.*

II. THE BOARD IMPROPERLY CONSTRUED THE TERM "HARDWARE BUFFER"

The Board determined that Intel had not shown claims 1-9 and 12 would have been obvious because the prior art references did not teach the "hardware buffer" recited in the claims. Appx10-17; Appx55-56. That ruling rested on the Board's erroneous construction of "hardware buffer." Appx55-56. Although the Board agreed with Intel in its institution decision that "hardware buffer" simply means a buffer implemented in hardware, the Board changed its mind and construed "hardware buffer" to exclude the use of a temporary buffer. Appx11-17. That narrow construction is wrong under any standard, and it is certainly not the broadest reasonable interpretation.

The ordinary meaning of "hardware buffer" should control. The patentee has not set out an alternative definition of "hardware buffer" in the patent, nor has the patentee clearly or unmistakably disavowed the scope of the claims reciting "hardware buffer" to exclude the use of a temporary buffer. The two statements on which the Board relied show, at best, only that claims 1-9 and 12 might exclude copying an *entire* executable image into a buffer before scatter loading it to its final destination in system memory. The Court should therefore vacate the Board's decision and remand for application of the proper claim construction.

A. "Hardware Buffer" Means A Buffer Implemented In Hardware

Under the broadest reasonable interpretation standard, the "words of a claim" are "'given their ordinary and customary meaning'" in the context of the claims, the specification, and the entire patent. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1374 (Fed. Cir. 2019). A patentee acts as its own lexicographer only when it sets out an alternative definition "'with reasonable clarity, deliberateness, and precision.'" *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1370-1371 (Fed. Cir. 2005). As Intel's expert explained, the ordinary meaning of "hardware buffer" is "'a buffer implemented in hardware.'" Appx1797; *see* Appx2829 (Intel's expert saying "hardware buffer has an ordinary meaning of a buffer implemented hardware"). Nothing in the patent contradicts that ordinary

meaning, let alone sets out an alternative definition clearly, deliberately, or precisely.

Claim 1, from which claims 2-9 depend, recites "system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image" and "a scatter loader controller configured" to scatter load each data segment "directly from the hardware buffer to the system memory." Appx78(12:60-13:3). As the Board recognized, those references do not "define what implementation the hardware buffer must take or what type of storage device the hardware buffer is." Appx12-13. The fact that claim 1 recites "system memory *and* a hardware buffer" (Appx78(12:60-65)) also does not "foreclose the possibility of implementing a buffer in some other system memory," Appx13.

All the claims indicate regarding a "hardware buffer" is that it can receive an image header and at least one data segment and that each received data segment is scatter loaded from the hardware buffer to the system memory. Claim 2 adds the limitation "without copying data between system memory locations on the secondary processor." Appx79(13:14-16).[4] Claim 8 adds the requirement that the loading into the system memory occurs "without an entire executable software image being stored in the hardware buffer." Appx79(13:39-41). Inclusion of those additional limitations in dependent claims does not limit the meaning of the term

[4] Claim 12, which depends from claim 10, is similar.

"hardware buffer" itself. Rather, it shows that when the claims intend a narrower meaning, they say so.

The patent's specification is no more illuminating or limiting. As the Board noted, the written description mentions "hardware buffer" only three times, none of which provides "much, if any, guidance on what a 'hardware buffer' must be." Appx15. In the "Summary" section, the patent explains that "[t]he system includes a secondary processor having a system memory and a *hardware buffer* for receiving *at a least a portion* of an executable software image." Appx73(2:58-61). It notes in the next sentence, "[t]he secondary processor includes a scatter loader controller for loading the executable software image directly from the *hardware buffer* to the system memory." Appx73(2:61-63). Finally, in the "Detailed Description," the specification notes that "[i]n one aspect" of the exemplary loading process as disclosed in Figure 3, "the executable software image is loaded into the system memory of the secondary processor without an *entire executable software image* being stored in the *hardware buffer* of the secondary processor." Appx77(9:37-41). The only things that these three statements add are examples of a "hardware buffer" that does not store an *entire* executable software image prior to scatter loading of that image.

None of this suggests that "hardware buffer" has anything other than the ordinary meaning of a buffer implemented in hardware. A buffer implemented in

hardware can, of course, receive at least a segment of an executable software image but not store the entire image before loading it to a system memory. The patentee has therefore failed to set forth an alternative definition of "hardware buffer" with any sufficient "clarity, deliberateness, and precision." *Merck*, 395 F.3d at 1370-1371. Under the broadest reasonable interpretation standard, "hardware buffer" should be given its ordinary meaning.

B. "Hardware Buffer" Does Not Exclude The Use Of A Temporary Buffer

Despite initially agreeing with Intel, the Board concluded in the final written decision that "hardware buffer" does not encompass the use of a temporary buffer for two reasons. First, the Board said the ordinary meaning of "hardware buffer" makes "hardware" superfluous. Appx14-15. Second, the Board reasoned that the patent describes the advantage of the direct scatter loading technique over the prior art as avoiding the use of a temporary buffer, and so the "hardware buffer" cannot include the use of a temporary buffer. Appx15-17. Neither conclusion has merit.

1. The preference for avoiding surplusage does not apply

Certainly, "[a] claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so." *Merck*, 395 F.3d at 1372. But the "preference for giving meaning to all terms … is not an inflexible rule." *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016); *see also Pickholtz v. Rainbow Techs., Inc.*, 284 F.3d 1365, 1373 (Fed.

Cir. 2002). This Court has acknowledged that "surplusage may exist in some claims," *Decisioning.com, Inc. v. Federated Dep't Stores, Inc.*, 527 F.3d 1300, 1312 n.6 (Fed. Cir. 2008), particularly "where neither the plain meaning nor the patent itself commands" a different result, *Power Mosfet Techs., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1410 (Fed. Cir. 2004). Thus, even if all buffers must ultimately be implemented in hardware, that does not warrant departing from the ordinary meaning of the claim. *See supra* pp. 28-30; *see infra* pp. 32-39.

Indeed, the patent repeatedly uses the term "hardware" in a manner that shows no aversion to redundancy. For example, it refers to "the hardware boot ROM 126 (small read-only on-chip memory)" even though such a boot ROM would have to be implemented in hardware. Appx75(5:20-22); *see also* Appx76(8:55-56) (referring to "extra hardware" that would allow "external control of the secondary processor's controller"). In the context of this routine use of the term "hardware," it is untenable to assume that "hardware buffer" must be construed narrowly to avoid use of a temporary buffer merely to avoid surplusage.

Further, in the analogous context of statutory interpretation, the rule against surplusage "'assists only where a competing interpretation gives effect to every clause and word of a statute.'" *Marx v. General Revenue Corp.*, 568 U.S. 371, 385 (2013); *cf. Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 987 (Fed. Cir. 1995) (en banc) (statutory interpretation is an "appropriate analogy for interpreting

patent claims"). Yet the construction adopted by the Board—that "hardware buffer" does not encompass the use of a temporary buffer—does not rid the claim of surplusage because a "hardware buffer" that does not encompass the use of a "temporary buffer" would still be a buffer implemented in hardware (just narrower in scope). In reality, the Board was not giving meaning to the word "hardware" at all, but engrafting an entirely new limitation onto Qualcomm's claims.

2. The '949 patent does not disavow the use of a temporary buffer with any clarity

Contrary to the Board's decision, the patent also does not indicate that "hardware buffer" excludes the use of a temporary buffer by distinguishing the claims from the prior art on that basis. Although a patentee can disavow claim scope, the patentee must do so explicitly in the patent, by including "a clear and unmistakable disclaimer" that contains "expressions of manifest exclusion or restriction." *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019), *cert. denied*, 140 S. Ct. 648 (2019) (quotation marks omitted). "Mere criticism of a particular embodiment encompassed in the plain meaning of a claim term is not sufficient to rise to the level of clear disavowal," nor is it enough that "the only embodiments, or all of the embodiments, contain a particular limitation," for the Court does "not read limitations from the specification into claims." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012).

The '949 patent does not clearly or unmistakably disavow the use of a temporary buffer. The Board essentially acknowledged as much, noting that the claims do not "define what implementation the hardware buffer must take or what type of storage device the hardware buffer is," Appx13, and that the references to "hardware buffer" in the written description provide little, "if any, guidance on what a 'hardware buffer' must be," Appx15.

All that the Board pointed to were two statements in the specification regarding the prior art's use of a temporary buffer. *See* Appx15-16. The specification notes that "***[i]n one exemplary aspect***[,] …. the direct scatter load technique avoids use of a temporary buffer." Appx74(4:43-47). With reference to another "***exemplary***" device of Figure 1, Appx74(4:6-7, 55), the patent discloses that the modem processor stores the executable image directly into that processor's RAM to the final destination "without copying the data into a temporary buffer in the modem processor RAM," Appx75(5:31-35).

Those "exemplary" embodiments do not limit the meaning of "hardware buffer." Indeed, the patent warns that an "exemplary" device "serv[es] as an example, instance, or illustration," and "is not necessarily to be construed as preferred or advantageous over other aspects." Appx74(4:22-25)) (quotation marks omitted); *accord* Appx13.

At most, the statements on which the Board relied "simply describe" one way in which the exemplary embodiments may work that is "different from the prior art process," *Continental Circuits*, 915 F.3d at 797. This Court has held that such "general descriptions of the characteristics of embodiments do not suffice to limit the claims." *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1331 (Fed. Cir. 2012); *see Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1358-1359 (Fed. Cir. 2016) (although "the specification discusses voice channels in many places," they do not amount to "'manifest exclusion or restriction' of the claim scope" in context). In other words, "nothing in the specification indicates" that the avoidance of a temporary buffer is "an essential feature of the claimed" technique. *Aventis Pharma*, 675 F.3d at 1330.

In this way, this case is much like *Continental Circuits* where the patent specification contained "'[m]ere criticism of a particular embodiment'" without clearly disclaiming it. 915 F.3d at 797-798. The district court in that case had limited the claim scope because "the specification not only repeatedly distinguishe[d] the process covered by the patent from the prior art and its use of a single desmear process, but also characterized the present invention as using a repeated desmear process." *Id.* at 794 (quotation marks omitted). This Court also acknowledged that the patent distinguished the double desmear process as "'contrary to'" or "'in stark contrast' with" the single desmear process. *Id.* at 797-

798. But the Court held that these statements "comparing and contrasting the present technique to that of the prior art" are still not, without more, "clear and unmistakable limiting statements." *Id.* The two statements on which the Board relied here easily fall short of a clear disavowal under *Continental Circuits* because they do not even use language like "'contrary to'" or "'in stark contrast' with," let alone contain other indicia of a disavowal. *See also AstraZeneca LP v. Breath Ltd.*, 542 F. App'x 971, 976 (Fed. Cir. 2013), *as amended on reh'g in part* (Dec. 12, 2013) (no clear disavowal where the specification is "[a]t most … confusing" regarding claim scope).

The Board's reliance on *SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc.*, 242 F.3d 1337 (Fed. Cir. 2001), does not change the analysis. Appx16. In *SciMed*, the Court addressed whether the common specification of the patents at issue limited the scope of the asserted claims to catheters with coaxial lumens, rather than also covering dual lumens. 242 F.3d at 1340. Lumens or passageways could be arranged in two ways: (1) in the dual lumen configuration, "the two lumens are positioned side-by-side within the catheter"; and (2) in the coaxial configuration, one of the lumens ("guide wire lumen") runs inside the other lumen ("inflation lumen"), and the "inflation lumen, viewed in cross-section, is annular in shape." *Id.* at 1339. This Court held that the

asserted claims read only on catheters having coaxial lumens because the specification expressly indicated so in numerous ways. *Id.* at 1340-1345.

For example, the abstract of the patents in *SciMed* identified the inflation lumen as being "annular" shape. *SciMed*, 242 F.3d at 1342. Thus, "from the outset the specification identifie[d] the inflation lumen … as 'coaxial rather than dual in structure.'" *Id.* The specification explained that certain prior art structures had a distinct "disadvantage" because they had "dual lumen configurations," while "point[ing] out the advantages of the coaxial lumens used in the catheters that are the subjects of the" patents. *Id.* at 1342-1343. Moreover, "the 'Summary of the Invention' portion of the patents describe[d] 'the present invention'" as having an "'annular inflation lumen,'" and the "characterization of the 'present invention' include[d] several more references to the 'annular inflation lumen.'" *Id.* at 1343.

"The most compelling portion of the specification" was the passage describing the inflation lumen as annular in structure and stating that that is the basic structure for "'*all embodiments of the present invention contemplated and disclosed herein*.'" *SciMed*, 242 F.3d at 1343 (emphasis in original). That language, the Court noted, defined the invention "in a way that excludes the dual … lumen arrangement." *Id.* "It [wa]s difficult to imagine how the patents could have been clearer in making the point that the coaxial lumen configuration was a necessary element of every variant of the claimed invention." *Id.* at 1344.

As explained above, the '949 patent does not evince any such clarity. Although the Board focused on a single aspect of *SciMed*—namely that the '949 patent purportedly distinguishes prior art that uses a temporary buffer, Appx16—"[m]ere criticism," by itself, does not amount to clear disavowal. *Thorner*, 669 F.3d at 1366; *see also Continental Circuits*, 915 F.3d at 797-798 (disavowal requires a "clear and unmistakable limiting statements"). Moreover, criticism of the prior art was only one factor in the analysis in *SciMed*. 242 F.3d at 1342-1344. In contrast to *SciMed*, the '949 patent does not characterize "the present invention" as avoiding the use of a temporary buffer. Its references to the avoidance of a "temporary buffer" appear in exemplary embodiments and are far "less direct, clear, and defining than the phrase '[the] structure … is the basic … structure for all embodiments,'" *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1121 (Fed. Cir. 2004). Nor does the '949 patent contain anything close to the "broad and unequivocal" statement in the *SciMed* patents that clearly limited the invention to coaxial lumens. *Id.* at 1343-1344.

3. Even if the patent could be read as disavowing prior art techniques, the patent would disclaim storing an entire image before scatter loading, not using a temporary buffer

Even if statements in the '949 patent could be read as limiting, the specification does not dictate avoidance of a temporary buffer. Rather, it focuses on scatter loading segments of an executable software image *without first copying*

the entire image into a temporary buffer. *E.g.*, Appx76(7:20-30). The specification states that the '949 patent purportedly solved problems with the conventional system by "avoid[ing] extra memory copy operations." Appx76(7:24-30). But that does not necessarily mean entirely avoiding the use of a "temporary buffer." Indeed, the specification explains that a hardware buffer performs similar functions as a prior art temporary buffer—*i.e.*, both receive data from the primary processor and store it for loading into a memory of a secondary processor. *See* Appx75(5:31-35) (temporary buffer); Appx73(2:58-3:2) (hardware buffer); *see also* Appx2828 (Intel's expert stating that "[a] buffer is a storage – something that can store data"). The purported difference between the "conventional" techniques and the alleged invention is how much image data is stored in the buffer before scatter loading into target locations. The specification states that "conventional techniques employing a temporary buffer for ***the entire image*** … are bypassed in favor of a more efficient direct loading process." Appx77(9:42-46) (discussing Figure 3); *see also* Appx77(9:37-41, 50-54).

The two statements on which the Board relied are consistent with that reading. Viewed in the context of the specification's description of conventional techniques using a temporary buffer "for the entire image," Appx77(9:42-46), statements that the modem processor does not "copy[] the data into a temporary buffer," Appx75(5:31-35), and a "direct scatter load technique avoids use of a

temporary buffer," Appx74(4:43-47), are likewise best read as referring to bypassing use of a temporary buffer to store the *entire* software image.

To the extent some embodiments purport to distinguish the prior art based on copying an entire image into a temporary buffer, the fact that other statements about exemplary embodiments might be read to refer to bypassing a temporary buffer entirely would not justify limiting a general term like "hardware buffer" to the narrower embodiment. *Cf. Trustees of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1368 (Fed. Cir. 2016) ("fleeting references cannot overcome the overwhelming evidence in the specification"). Indeed, the distinction the specification is drawing does not concern the meaning of "hardware buffer" at all. Rather, the patent channels that distinction to claim 8, which adds the requirement that "the portion of the executable software image is loaded into the system memory of the secondary processor without an entire executable software mage being stored in the hardware buffer." Appx79(13:37-41).

The Board improperly narrowed the scope of the claims. Its construction of "hardware buffer" is incorrect under any standard, and all the more so under the broadest reasonable interpretation standard that applies here. This Court should reverse and instead give "hardware buffer" its plain and ordinary meaning—a buffer implemented in hardware.

III. EVEN UNDER THE BOARD'S CLAIM CONSTRUCTION, THE BOARD'S DECISION AS TO CLAIMS 1-9 AND 12 CANNOT STAND BECAUSE IT LACKS SUBSTANTIAL EVIDENCE

Even if the Court were to accept the Board's erroneous construction, the Board's decision regarding claims 1-9 and 12 still cannot stand. The Board determined that Intel had not proven obviousness of claims 1-9 and 12 under the Board's construction of "hardware buffer," because "the intermediate storage area of Bauer and Svensson is a temporary buffer." Appx56. That finding is unsupported by substantial evidence.

A "temporary buffer" has to be, as the term indicates, temporary—*i.e.*, if the buffer is allocated or reserved at runtime of the program loader to receive image sections, then the buffer would have to be deallocated to be used for another purpose later. Yet there is no evidence that the intermediate storage area in Svensson and Bauer is deallocated to be used for another purpose. Svensson discloses that a block of memory at the client processor is reserved as an intermediate storage area for storage of information to be transferred to the actual system memory (DSP XRAM 110) for later execution. Appx1286(5:21-28). As Qualcomm's expert agreed, the client processor in Svensson does not execute code directly from that intermediate storage area, Appx6407, which indicates that the intermediate storage area is not used for other purposes such as executing code later (as a temporary buffer would). Instead, the intermediate storage area is

permanently allocated for storing information to be transferred to the system memory. Bauer discloses the same intermediate storage area. Appx1276-1277(¶¶ 31, 35-36); *see* Appx27 (Bauer's Figure 2 "depicts the same multi-processor system as Svensson's Figure 1"). Thus, Svensson and Bauer make plain that the intermediate storage area is allocated for the purpose of receiving information to be transferred to the actual system memory for later execution.

Nothing suggests that this intermediate storage area is deallocated to be used for another purpose. To the contrary, Svensson discloses that the intermediate storage area is reserved at boot up of the client processor. *See* Appx1283 (Fig. 2, blocks 208-212). It is then used whenever the host processor is running, including during normal operation to change the software running on the client processors, which means the intermediate storage area is permanent. *See* Appx1287(8:29-32) ("With the OS-friendly bootloader described here, one can load and execute new software in the [client processor] virtually any time the host processor is running."); Appx1287(8:17-19) ("It will therefore be understood that the OS-friendly boot loader described here also makes it possible to change software executing in the [client processor]"). That indicates that the intermediate storage area is not deallocated for later use for other purposes, and it is therefore permanent instead of temporary.

The Board found that the intermediate storage area of Bauer and Svensson is a temporary buffer because "Svensson discloses that the intermediate storage area is reserved at runtime of the program loader." Appx55-56. But again, being "reserved at runtime of the program loader" does not make a buffer "temporary" unless the buffer is also deallocated. The Board cited no evidence that the intermediate storage area of Svensson and Bauer is deallocated. The Court should therefore vacate the Board's unsupported decision. *See Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043-1044 (Fed. Cir. 2017); *cf. Takeda Pharm. Co. Ltd. v. Array Biopharma Inc.*, 720 F. App'x 620, 622-623 (Fed. Cir. 2017).

IV. THE BOARD DID NOT NEED TO CONSTRUE THE MEANS-PLUS-FUNCTION LIMITATIONS IN CLAIMS 16 AND 17 OR, ALTERNATIVELY, SHOULD HAVE DECLINED TO REACH A DECISION ON THE MERITS IN LIGHT OF THEIR INDEFINITENESS

Claim 16 (from which claim 17 depends) identifies a "means for receiving at a secondary processor…an image header…"; a "means for processing…"; a "means for receiving at the secondary processor … each data segment"; and a "means for scatter loading…" Appx79(14:17-37). The Board agreed with Intel that each of these is a means-plus-function limitation subject to 35 U.S.C. § 112, ¶ 6 (2011). Appx17.

"Construction of a means-plus-function limitation involves two steps. First, the court must identify the claimed function." *Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1113 (Fed. Cir. 2002). "After identifying the

claimed function, the court must then determine what structure, if any, disclosed in the specification corresponds to the claimed function." *Id.* "In order to qualify as corresponding, the structure must not only perform the claimed function, but the specification must clearly associate the structure with performance of the function." *Id.*

Intel's petition identified corresponding structure for each term, consistent with the ruling by the Chief Administrative Law Judge in Qualcomm's ITC case against Apple phones using Intel's baseband processors. Appx5026-5030; Appx5156-5159. In its institution decision, however, the Board questioned the sufficiency of the identified structures. Appx5160-5162. It invited the parties to address "the impact that a determination that the specification of the '949 patent does not provide adequate corresponding structure for the recited functions should have on this proceeding and any final written decision." Appx5162.

After institution, Qualcomm argued that the means-plus-function terms did not need to be construed, but that if they were, they should be construed as they were in the ITC investigation. Appx4227-4230; *see also* Appx4325. Intel acknowledged that upon consideration of the Board's concerns, the "specification fails to disclose sufficient structure to perform the recited functions." Appx4325. But Intel argued that the claims could be deemed obvious without construing them,

Appx4325-4326, because "the Patent Owner concedes that none of its arguments turn on the means-plus-function terms," Appx4326 n.6

The Board's final written decision concluded that because Intel had acknowledged that the '949 patent fails to disclose a corresponding structure for the means-plus-function limitations, it had failed to show the unpatentability of claims 16 and 17. Appx17-18. Noting that an IPR petitioner bears the burden to identify such structure under 37 C.F.R. § 42.104(b), the Board concluded that Intel "ha[d] not met its burden" and that claims 16 and 17 are therefore not unpatentable. Appx17-18; Appx62.

The Board's decision to rule against Intel on the merits suffers from multiple defects. *First*, the Board never addressed Intel's argument that it was unnecessary to construe the means-plus-function terms because Qualcomm did not defend the patentability of its claims on that basis. *See* Appx4226; Appx4325. Elsewhere in its final written decision the Board invoked the principle that claims need to be construed only insofar as "necessary to resolve the obviousness inquiry." Appx17 (citing *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017)); *Nidec*, 868 F.3d at 1017 ("we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'"). The Board should have heeded that principle and resolved the

disputed points before it—and thus the patentability of claims 16 and 17—without needing to reach a definitive construction of the means-plus-function terms.

Second, to the extent the Board considered the means-plus-function terms indefinite, it should not have ruled against Intel on the merits, and Intel should not be estopped under 35 U.S.C. § 315(e). In *Samsung Electronics America, Inc. v. Prisua Engineering Corp.*, 948 F.3d 1342 (Fed. Cir. 2020), this Court explained that when the Board "cannot ascertain the scope of a claim with reasonable certainty for purposes of assessing patentability," the claim is indefinite. *Id.* at 1353. The Court noted, however, that indefiniteness is outside the scope of an IPR inquiry. *Id.* Thus, the Court held that "the proper course for the Board to follow" in such situations is "to decline to institute the IPR or, if the indefiniteness issue affects only certain claims, to conclude that it could not reach a decision on the merits with respect to whether petitioner had established the unpatentability of those claims under sections 102 or 103." *Id.* The Court further clarified that "in cases in which the Board cannot reach a final decision as to the patentability of certain claims because it cannot ascertain the scope of those claims with reasonable certainty, the petitioner would not be estopped by 35 U.S.C. § 315(e) from

challenging those claims under sections 102 or 103 in other proceedings." *Id.* at 1353 n.3.[5]

Under that standard, the Board erred in finding that Intel "ha[d] not met its burden" to show corresponding structure. Appx62. Intel could not have failed to show something that does not exist due to the *patentee's* failure to disclose it. Thus, the Board should have declined to reach an unpatentability decision, to ensure that Intel is not estopped from challenging claims 16 and 17 for obviousness later. The Board's rule, 37 C.F.R. § 42.104(b), on which the Board relied (Appx17-18, Appx62), does not suggest otherwise. That section governs the "[c]ontent of petition" and provides that "[w]here the claim to be construed contains a means-plus-function or step-plus-function limitation as permitted under 35 U.S.C. 112(f), the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function." 37 C.F.R. § 42.104(b)(3). But that merely begs the question as to what the Board must do when the *patent* fails to disclose the

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[5] This Court reiterated that principle in *Cochlear Bone Anchored Solutions AB v. Oticon Medical AB*, 958 F.3d 1348 (Fed. Cir. 2020). Citing *Samsung*, the Court noted that the Board should "'conclude that it could not reach a decision on the merits with respect to whether petitioner had established the unpatentability of those claims.'" *Id.* (quoting *Samsung*, 948 F.3d at 1353). Further, because any "rejection of the petitioner's prior-art challenge rests on a deficiency of the *patentee's* making, not the *petitioner's*," the Court emphasized in *Cochlear*, as it did in *Samsung*, that "'the petitioner would not be estopped by 35 U.S.C. § 315(e) from challenging those claims'" in the future. *Id.*

necessary "structure." This Court answered that question in *Samsung* by requiring the Board to decline to decide whether the petitioner had established the unpatentability of the challenged claims.

V. INTEL HAS STANDING TO PURSUE THIS APPEAL

Intel has standing to appeal the Board's final written decision because it suffers a concrete, particularized, and sufficiently imminent injury in the form of a potential infringement accusation or, at a minimum, the use of the '949 patent to constrain the actions of Intel and its customers.

Article III standing has three elements: the party invoking federal jurisdiction "must have (1) suffered an injury in fact, (2) that is fairly traceable to the challenged conduct of the defendant, and (3) that is likely to be redressed by a favorable judicial decision." *Spokeo, Inc. v. Robins*, 136 S. Ct. 1540, 1547 (2016). To establish an injury in fact, an appellant "must typically show an invasion of a legally protected interest that is concrete, particularized, and actual or imminent, as opposed to merely conjectural or hypothetical." *Grit Energy Sols., LLC v. Oren Techs., LLC*, 957 F.3d 1309, 1319 (Fed. Cir. 2020). But because Congress authorized an appeal of the Board's final written decision in an IPR, *see* 35 U.S.C. § 141(c), the appellant in such circumstances "need not 'meet all the normal standards for redressability and immediacy.'" *JTEKT Corp. v. GKN Auto. LTD.*, 898 F.3d 1217, 1219-1220 (Fed. Cir. 2018). The Supreme Court has explained, for

example, that a party with a procedural right provided by Congress may satisfy Article III standing, even though the object of contention may not occur "for many years." *Lujan v. Defenders of Wildlife*, 504 U.S. 555, 572 n.7 (1992). Intel readily satisfies these criteria.

A. Intel Suffers Injury In Fact

"In order to demonstrate the requisite injury in an appeal from a final written decision in an inter partes review, … it is generally *sufficient* for the appellant to show that it has engaged in, is engaging in, or will likely engage in 'activity that would give rise to a *possible* infringement suit.'" *Grit Energy*, 957 F.3d at 1319. To show such a risk, the appellant need not have already been sued, nor does it need to show that it actually infringes the patent at issue. Indeed, this Court has explained that the injury-in-fact element of Article III standing does not require an appellant to "'bet the farm, or … risk … damages … before seeking a declaration of its actively contested legal rights.'" *JTEKT*, 898 F.3d at 1220 (quoting *MedImmune, Inc. v. Genentech, Inc.*, 549 U.S. 118, 134 (2007)). The Supreme Court has explained, moreover, that Article III's case-or-controversy requirement may be met even in the absence of the risk of an infringement suit. *MedImmune*, 549 U.S. at 132 n.11.

1. Intel faces the risk of a possible infringement allegation by Qualcomm based on Qualcomm's actions against Apple

Intel faces a concrete, particularized, and sufficiently imminent risk of an infringement accusation based on Qualcomm's prior actions against Apple for using Intel baseband processors. *See Grit Energy*, 957 F.3d at 1319-1320. Qualcomm has already asserted the '949 patent against Apple, Intel's biggest customer for baseband processors, in both the Southern District of California and the ITC. *See* Appx6240; Appx6216. In both actions, Qualcomm targeted only those Apple devices with Intel's baseband processors, in a clear effort to drive Intel from the market. As Apple explained, it was "no coincidence that Qualcomm has brought this action only after Apple began buying chipsets from Intel." Appx6233; *accord* Appx6247-6251 (Qualcomm's Chief Technology Officer acknowledging that only those iPhones containing an Intel chipset are accused).

Moreover, Qualcomm's proof at trial in the Southern District of California focused extensively on Intel components, documents, and software. As Qualcomm's expert explained, his "first assignment was to analyze the '949 patent and several phones, the iPhone 7, 7 plus, 8, 8 plus and iPhone X, all with the Intel chipset … to determine whether those phones did, in fact, infringe the '949 patent." Appx6256-6257. Qualcomm "identified the Intel modem package as the secondary processor" in claim 1 of the '949 patent. Appx6272-6273. And "for a lot of" the elements of claim 1 in the '949 patent that Qualcomm's expert

considered "undisputed[ly] … infringed," the expert looked at Intel's design documents because those documents "describe how the Intel baseband processors are integrated into the iPhones." Appx6261-6262. Indeed, Qualcomm's expert emphasized the Intel components in his infringement opinion, noting: "Intel is a supplier to Apple, and even though it's the Apple iPhones that infringe, part of the reason they infringe is because they incorporate these Intel baseband processors." Appx6262.[6]

These theories of infringement that Qualcomm asserted against Apple create a substantial risk that Intel will be accused of direct infringement—either in connection with product testing or claim 16—or for indirect infringement when Intel's baseband processors are used with a customer's primary processor. Qualcomm denies the injury by arguing that it "has not sued Intel for infringement

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[6] Qualcomm's infringement theories focused on claims 1 and 2, but there is a risk that Qualcomm will allege that Intel infringes the other claims challenged on appeal because Qualcomm identified Intel's baseband processor as the "secondary processor." Claims 3, 8, and 12 are directed to the way data is received by the *secondary processor*. Claims 4 and 5 are directed to the way the *secondary processor* is configured. Claims 6 and 7 are directed to the location or components of the *secondary processor*. And claims 9 and 17 merely add a generic list of electronic devices. *See* Appx79(13:18-14:42).

Moreover, claim 16 is an apparatus claim directed to "means" for "receiving," "processing," and "scatter loading"—all "at" or "by" the "secondary processor." Appx79(14:16-37). Although claim 16 is indefinite because the specification fails to disclose corresponding structure, Appx62, there is a substantial risk that, given its arguments at trial, Qualcomm would assert direct infringement of claim 16 focusing solely on Intel components and software.

of the '949 patent" or "threatened Intel with [such] litigation." Mot. to Dismiss 7-8; *accord* Reply 2 (ECF No. 37). But as explained above, the question is not whether Intel has already been sued for infringement; it is whether Intel "has engaged in, is engaging in, or will likely engage in 'activity that would give rise to a *possible* infringement suit.'" *Grit Energy*, 957 F.3d at 1319; *see also E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1005 (Fed. Cir. 2018) (DuPont has standing based on its actions that "'would implicate'" the patent at issue); *Altaire Pharms., Inc. v. Paragon Bioteck, Inc.*, 889 F.3d 1274, 1282-1283 (Fed. Cir. 2018), *remand order modified by stipulation*, 738 F. App'x 1017 (Fed. Cir. 2018) (Altaire has standing based on its future plans to market a product that would prompt an infringement suit).[7]

Moreover, an appellant seeking review of the Board's decision "need not face a *specific* threat of infringement litigation by the patentee to establish jurisdiction, but rather need only generally show a controversy of sufficient immediacy and reality to warrant the requested judicial relief." *Grit Energy*, 957 F.3d at 1319 (quotation marks omitted); *accord Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1357 (Fed. Cir. 2020). Qualcomm's actions against Apple plainly pose a

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[7] Although Qualcomm attempts to distinguish the cases Intel cites based on their facts (Reply 5-7), this Court's holdings are not limited to the precise facts of a case, and Intel meets the injury-in-fact standard for all the reasons stated in Section V.

sufficiently real and immediate controversy, since Qualcomm's arguments in prior infringement actions were predicated on Apple's use of Intel's baseband processors.

Qualcomm also argues that the claims it asserted against Apple "required some components made by Apple" (in addition to Intel), so there was no "product made entirely by Intel … infringing" the '949 patent. Mot. to Dismiss 8; *see also* Reply 2. That does not mitigate the threat of Qualcomm asserting direct or indirect infringement against Intel. *See* 35 U.S.C. § 271(b), (c). Indeed, Qualcomm mapped the asserted claims of the '949 patent primarily onto Intel's baseband processor and its functions. *See* Appx6283-6287 (¶¶ 104-118). For example, claim 1 recites: (1) a secondary processor comprising (a) system memory and a hardware buffer for receiving an executable software image and (b) a scatter loader controller that is configured a certain way; (2) a primary processor coupled with a memory storing the executable software image for the secondary processor; and (3) an interface that allows for the secondary processor to receive the executable software image from the primary processor. Appx78-79(12:60-13:10). Intel's baseband processor allegedly constitutes the secondary processor along with all its claimed components ("(1)" above), and Intel's software is the alleged "executable software image" that is stored on the memory coupled to the primary processor (in "(2)" above). *E.g.*, Appx6264-6265 (Qualcomm's expert examining Intel

documents for the secondary processor's system memory and hardware buffer in claim 1). Thus, the risk that the '949 patent poses to Intel is far from speculative.

2. Intel's past, current, and future sales of its baseband processors further demonstrate the risk of a possible infringement allegation

The threat of an infringement allegation by Qualcomm is especially concrete, particularized, and imminent because of Intel's past, present, and future sales to Apple. "Past activities, like present and potential future activities, can create a controversy between two parties." *Grit Energy*, 957 F.3d at 1320. Intel has supplied baseband processors to Apple for years. *See* Appx6204-6205.

Qualcomm incorrectly argues (Mot. to Dismiss 9) that its settlement with Apple makes an infringement action against Intel "speculative." Qualcomm admitted (*id.*), however, that Intel is not a signatory to the settlement agreement. And although Qualcomm has not put the agreement into the record, Qualcomm notably does not say in its motion that it has released any claims against Intel. Thus, Intel still faces risk based on its past supply to Apple. Indeed, in *Exelis Inc. v. Cellco Partnership*, 2012 WL 5289709, at *3-5 (D. Del. Oct. 9, 2012), the district court held that claims of both direct and indirect infringement could proceed against manufacturers of mobile devices even though the patentee had

covenanted not to sue the direct infringers (the network provider and its customers) for infringement.[8]

Further exacerbating the risk, Qualcomm has refused to provide a covenant not to sue to Intel. Appx6183; *see Grit Energy*, 957 F.3d at 1320 n.3 (patentee's failure to stipulate it will not sue for infringement supports injury); *Altaire*, 889 F.3d at 1283 (same); *Adidas*, 963 F.3d at 1357 (patentee's refusal to grant a covenant not to sue confirms injury); *E.I. DuPont*, 904 F.3d at 1005 (same). Qualcomm tries to minimize this failure by arguing that its refusal to covenant not to sue Intel "does nothing to confer standing," Reply 5; but the point here is that such refusal *supports* standing even if it may not, by itself, establish standing. Given that all the relevant information is in Qualcomm's hands, and Qualcomm has refused to covenant not to sue Intel, Qualcomm's settlement with Apple does not diminish Intel's risk of an infringement allegation. Moreover, Qualcomm will likely argue that Intel is estopped from challenging the relevant claims of the '949 patent as obvious in any subsequent proceedings under 35 U.S.C. § 315(e), which "compound[s]" Intel's injury. *Altaire*, 889 F.3d at 1283.[9]

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[8] Intel disagrees with the holding in *Exelis*, but that issue would have to be litigated and does not diminish the risk that Intel would face an infringement allegation.

[9] The Court has not decided, however, whether estoppel under § 315(e) would apply if an IPR petitioner lacked standing to appeal the Board's decision to this Court. *See AVX Corp. v. Presidio Components, Inc.*, 923 F.3d 1357, 1363 (Fed.

Besides past sales, Intel has continued to sell its baseband processors to Apple. It is true, as Qualcomm notes, that Intel has sold part of its baseband processor business to Apple recently, but Intel has not yet exited the market entirely. Appx6205. It is continuing to supply Apple with baseband processors for legacy versions of Apple's products, and Intel expects to make sales outside of the smartphone modem market. Appx6205-6206; *see Altaire*, 889 F.3d at 1282-1283 (likelihood of future events supports a "'real and imminent'" threat of injury).

Further, as a real-party-in-interest, Apple continues to be affected in its use of Intel baseband processors. As noted, Qualcomm's securities filing reported that Apple is paying Qualcomm royalties as part of the settlement that followed the infringement verdict on the '949 patent, and that the license will expire after six years. Appx6210. Dismissing this appeal would leave Apple subject to the same estoppel arguments as Intel, continuing its harm from the '949 patent in both the short and long term.

Cir. 2019). Thus, although the possibility of § 315(e) estoppel supports Intel's injury here, Intel reserves the right to argue that estoppel does not apply where the petitioner lacked standing to appeal. *See Penda Corp. v. United States*, 44 F.3d 967, 973 (Fed. Cir. 1994) ("It is axiomatic that a judgment is without preclusive effect against a party which lacks a right to appeal that judgment."); Restatement (Second) Judgments § 28 (1982) ("relitigation of the issue in a subsequent action between the parties is not precluded" if "[t]he party against whom preclusion is sought could not, as a matter of law, have obtained review of the judgment in the initial action."); 18A Fed. Prac. & Proc. Juris. § 4433 (3d ed.) (issue preclusion might not apply where party lacked opportunity to appeal due to lack of standing).

3. Intel suffers competitive injury from the Board's decision

In prior cases, this Court has declined to find standing based on competitive injury in an appeal from the Board's decision, because the Board's "upholding of specific patent claims" did not "nonspeculatively threaten[] economic injury to the challenger by the ordinary operation of economic forces." *AVX Corp. v. Presidio Components, Inc.*, 923 F.3d 1357, 1364-1365 (Fed. Cir. 2019). Nonetheless, the Court indicated that competitive standing may apply to an appeal from the Board's decision where the Board's upholding of claims "change[s] the competitive landscape for" the product at issue. *General Elec. Co. v. United Techs. Corp.*, 928 F.3d 1349, 1354 (Fed. Cir. 2019); *cf. AVX Corp.*, 923 F.3d at 1365 ("patent claim *could* have a harmful competitive effect on a would-be challenger … if the claim would block the challenger's own current or nonspeculative actions").

This is precisely such a case. Qualcomm has already used infringement allegations against Apple to try to drive Intel out of the baseband processor market. *See* Appx6233-6234 ("Qualcomm is ruthlessly using this Investigation to … attempt[] to drive out its only remaining premium LTE chipset competitor (Intel)"); *accord* Appx6228-6229. The Board's patentability decision, coupled with the possibility of estoppel against Intel in a potential infringement action, entrenches Qualcomm's position in the market to Intel's detriment.

For example, without the ability to challenge the Board's patentability finding, Intel may lose future customers due to concerns regarding the '949 patent. Appx6206. Intel may also need to design its baseband processors differently to prevent any infringement claim. *Id.* By contrast, if Intel were to prevail in this Court, that could change the competitive landscape by allowing Intel to compete with Qualcomm without artificial constraints. The Board's decision, in other words, "nonspeculatively threaten[s] economic injury" to Intel. *AVX Corp.*, 923 F.3d at 1364-1365; *see General Elec.*, 928 F.3d at 1354.

If an agency had decided to keep in place a regulation that restricted Intel from working with potential customers in the same way as Qualcomm's patent claims, there would be no question that, as a member of the affected industry, Intel would be able to sue based solely on the way that the regulation had skewed the competitive dynamic. The result should not be different because the case involves patentability.

4. Qualcomm's remaining argument is meritless

Qualcomm's only remaining response to Intel's standing arguments is that Intel has not substantiated the risk that Qualcomm would allege infringement. Qualcomm contends, for example, that Intel "never articulate[d] how it believes its baseband processors risk meeting all of the limitations of any claim of the '949 patent" and that Intel provided "no claim charts or any other attempt to map any

claims of the '949 patent onto Intel's products." Reply 3. Qualcomm similarly complains, as to competitive standing, that Intel was "required to provide significantly more detail" as to how the '949 patent's claims would block Intel's actions in the competition for sales. Reply 10.

Intel has explained, however, that Qualcomm mapped the asserted claims of the '949 patent onto Intel's baseband processor in prior proceedings. *See supra* pp. 49-50, 52-53. Intel also showed through a declaration from Intel personnel how the patent claims would affect Intel's competitive behavior. *See supra* pp. 56-57; Appx6203-6206. Insofar as Qualcomm believes (Reply 3) that Intel needs to show further "evidentiary support," that is incorrect. In *MedImmune*, the Supreme Court held that Article III's case-or-controversy requirement is met even without the risk of an infringement suit. 549 U.S. at 132 n.11. There, a patent licensee had paid royalties to the patent assignee before challenging the patent as invalid, which made imminent threat "at least remote, if not nonexistent." *Id.* at 121-122, 128. Nonetheless, the Supreme Court upheld federal jurisdiction under Article III, rejecting this Court's "'reasonable apprehension of imminent suit' test." *Id.* at 132 & n.11. As the Supreme Court explained, the requirement that a patent challenger show a reasonable apprehension of suit "conflict[ed] with [its] decisions," including *Cardinal Chemical Co. v. Morton International, Inc.*, 508 U.S. 83, 98 (1993), "which held that appellate affirmance of a judgment of noninfringement,

eliminating any apprehension of suit, does not moot a declaratory judgment counterclaim of patent invalidity." *MedImmune*, 549 U.S. at 132 n.11. It makes little sense to require Intel to *prove* infringement in detail (as Qualcomm demands), when the risk of an infringement suit itself is not required to satisfy Article III.

B. Intel Satisfies The Remaining Requirements Of Article III Standing

Qualcomm challenges only Intel's injury in fact and does not argue that Intel lacks any of the other elements of Article III standing. At any rate, it is clear that Intel satisfies the remaining requirements of Article III standing because Intel's injury—the risk of an infringement allegation or the threat that Qualcomm would use the '949 patent to constrain Intel's and its customers' actions—is fairly traceable to the '949 patent and is likely redressed by this Court's favorable decision holding certain claims unpatentable. *See E.I. DuPont*, 904 F.3d at 1005 (finding standing because appellant faces a substantial risk of infringement or infringement action and "there is no dispute that the risk of infringement liability is attributable to [the challenged patent], and that the risk could be redressed by our review of the Board's decision").

* * *

For all of these reasons, Intel clearly has standing to pursue this appeal. In the alternative, to the extent the Court were to conclude that Intel lacks standing (which it should not), Intel requests that the Court join the other real-party-in-

interest Apple as a party. *See, e.g.*, *Mullaney v. Anderson*, 342 U.S. 415, 416-17 (1952) (joining additional parties to resolve alleged lack of standing); *see also* Fed. R. Civ. P. 21 ("On motion or on its own, the court may at any time, on just terms, add or drop a party.").

CONCLUSION

The Court should reverse or vacate and remand the Board's final written decision as to claims 1-9, 12, 16, and 17.

Respectfully submitted,

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