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Transcript of Martin Rinard, Ph.D.

Date: June 3, 2022
Case: Intel Corporation -v- Qualcomm Incorporated (PTAB) (INTEL)

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IPR2018-01334
Intel v. Qualcomm
INTEL 1028

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

QUALCOMM INCORPORATED,

Patent Owner.

IPR2018-01334

U.S. Patent No. 8,838,949

Deposition of MARTIN RINARD, Ph.D.

Conducted Virtually

Friday, June 3, 2022

7:03 a.m.

Job No.: 451226

Pages: 1 - 88

Reported by: Renee J. Ogden, CSR-3455, RPR

APPEARANCES:

ON BEHALF OF THE PETITIONER:

WILMER CUTLER PICKERING HALE AND DORR, LLP
BY: JOSEPH F. HAAG
1875 Pennsylvania Avenue, NW
Washington, DC 20006
(202) 663-6000
Joseph.haag@wilmerhale.com

ON BEHALF OF THE PATENT OWNER:

JONES DAY
BY: JOSHUA R. NIGHTINGALE
500 Grant Street
Suite 4500
Pittsburgh, Pennsylvania 15219
(412) 394-7950
Jrnightingale@jonesday.com

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(Exhibits not offered.)

Friday, June 3, 2022
7:03 a.m.

PLANET DEPOS TECH: Thank you to everyone for attending this proceeding remotely which we anticipate will run smoothly. Please remember to speak slowly and do your best not to talk over one another, and please be aware that we are recording this proceeding for backup purposes. Any off-the-record discussions should be had away from your computer, and please remember to mute your mic for those conversations.

Please have your video enabled to help the reporter identify who is speaking. If you're unable to connect with video and connect via phone, please identify yourself each time before speaking. And I apologize in advance for any technical-related interruptions. Thank you.

COURT REPORTER: The attorneys participating in this deposition acknowledge that I'm not physically present in the deposition room and that I will be reporting this deposition and

administering the oath remotely.

The parties and their counsel consent to this arrangement and waive any objections to this manner of reporting.

Counsel, please indicate your agreement on the record.

MR. HAAG: This is Joseph Haag. We agree.

MR. NIGHTINGALE: This is Josh Nightingale of Jones Day. We agree.

MARTIN RINARD, Ph.D.,

was thereupon called as a witness herein, and after having first been duly sworn or affirmed to testify to the truth, the whole truth and nothing but the truth, was examined and testified as follows:

EXAMINATION

BY MR. HAAG:

Q. Good morning.

A. Good morning.

Q. Can you please state your full name for the record?

A. Martin Conway Rinard.

Q. And what is your current address?

A. 48 Robbins Road, Arlington, Massachusetts 02416.
Q. And where are you currently located?
A. At that address.
Q. So is that your home address?
A. Yes, it is.
Q. Do you understand that you're under oath today?
A. Yes, I do.
Q. And do you understand that you must answer truthfully and fully just as if you were in the court?
A. Yes, I do.
Q. Is there any reason you cannot provide your best and honest testimony here today?
A. Not that I'm aware of.
Q. Approximately how many times have you been deposed before?
A. It's hard for me to give you an exact answer. I would say in the ballpark of 10, maybe 12; maybe a little bit more than that, maybe a little less.
Q. So you understand that I'll be asking you a series of questions here today?
A. Yes, I do.

Q. And you'll be providing answers as best you can?
A. That's my understanding.
Q. And I would appreciate it if you don't interrupt me when I'm trying to ask a question. Can we agree on that?
A. I'll do my best.
Q. And I'll also do my best to try not to interrupt your answers, okay?
A. Okay.
Q. Have you been deposed by -- over a video link before?
A. Yes, I have.
Q. Okay. Do you have any documents in front of you? Physical documents?
A. I have Gupta; this is the '949 Patent. I've got Svensson U.S. Patent 7,356,680. I've also got Bauer, which is -- yeah, I think we know what I'm talking about.
Q. Okay. Do you have any notes on those documents?
A. No, I don't. They should be clean copies.
Q. And is the '949 Patent exhibit marked 1001?
A. Let me see.

It says Intel 1001, and it appears to be a copy of the -- well, we'll see it if loads. Yeah. It appears it be a copy of the '949 Patent. I haven't examined every page, but it looks familiar.

Q. Okay. And then physical copy of Svensson that you have, is that marked Exhibit 10- -- 1010?

A. No. It's just -- it's not marked at all.

Q. Okay.

A. It doesn't have an exhibit marker on it.

Q. And then is Bauer, is that marked 1009?

A. No markings on it whatsoever.

Q. Okay.

A. No exhibit markings.

Q. You don't have any handwritten notes on any of those physical documents?

A. No, I don't.

Q. And just before the deposition started, I believe you downloaded copies of Exhibit 1001, 2015, and 2014; is that right?

A. That's correct.

Q. Do you have any other electronic documents open?

A. No, I do not.
Q. So I'd like to turn first to --
A. Just for clarification?
Q. Sure.
A. So I'm looking at -- okay. You know, I'm just looking for the exhibit numbers on the documents and I see them, so I think we're good.
Q. It should be lower right of the first page.
A. Yeah, I see them.
Q. Do you see that, sir?
A. I do.
Q. Okay. So I'd like to first turn to Exhibit 2015.
A. Okay. Which one's that again? Oh, that's my declar- -- that's the remanded declaration of Dr. Martin Rinard, correct?
Q. Yes.
Do you have that in front of you?
A. Give me a second.
Yes, I have it in front of me.
Q. And do you recognize this document?
A. Let me take a look.
Yeah, again, without examining it, it

appears to the remanded declaration of -- filed in this case.

Q. And do you see your signature on the last page?

A. Yes, I do.

Q. That is your signature, right?

A. It appears to be, yes.

Q. And approximately how much time did you spend on this declaration?

A. Difficult for me to give you an exact answer. I would say, again, ballpark some tens of hours. I would say certainly less than 100; probably less than 50. It would be difficult for me to be more exact than that.

Q. And I think you've spent a decent amount of time on the '949 Patent over the past few years, right?

A. I don't know whether I would characterize it as "decent" or not, but, yes, I've been involved with this patent in several litigations.

Q. And you have been deposed on it at least a couple times; if not a few times, right?

A. I'd say that's accurate, yes.

Q. Pardon me?

A. I've been deposed several times on matters involving the '949 Patent.
Q. So I'd like to turn first to paragraph -- if I can find it -- paragraph 45 of your declaration of Exhibit 2015. It should be on page 22.
A. Yes.
Q. Do you have that in front of you, sir?
A. Paragraph 45 you said?
Q. Yes.
A. Yes, I have paragraph 45 in front of me.
Q. And in paragraph 45, you address claims 1 and 2, right?
A. I believe that's correct, yes.
Q. This is claims 1 and 2 of the '949 Patent, right?
A. That's my understanding.
Q. And you say that claims 1 and 2 have a different scope under your proposed construction, right?
A. Well, I believe it said "different scopes under my proposed construction."
Q. And there's a sentence that begins with "Claim 2 further limits."
Do you see that?

A. Yes, next to last sentence in the paragraph. Is that what you're referring to?
Q. Yes.
Can you read that out loud for us, please?
A. Do you want me to read the whole paragraph? Just that one sentence.
Q. Just that one sentence.
A. Yeah. So just for context, I think -- I'm happy to read that one sentence, but I want -- but I'll just remark that that one sentence occurs in the context of paragraph 45, and it's a single sentence in the middle of paragraph 45. The context would include the sentences before it and the sentences after it. So having that, the sentence that you've asked me to read reads: "Claim 2 further limits the scatter loader controller element by adding limitations on how it 'directly' loads into system memory - specifically, expressly excluding 'copying data between system memory locations on the secondary processor.'"
I note that there's more sentences in

that paragraph and in the declaration in general that provide additional context to the sentence that I just read.

Q. So in that sentence am I right that you're saying that claim 2 further limits claim 1 in that claim 2 excludes copying between system memory locations on the secondary processor?

MR. NIGHTINGALE: Objection to form.

A. Let me take a quick like here. You're asking me about -- I'm understanding your question to be asking me specifically about the text of claim 2. I have claim 2 here, and it says -- it includes the limitation of "without copying data between system memory locations on the secondary processor."

BY MR. HAAG:

Q. So in that sentence, you're saying that claim 2 further limits claim 1, right?

A. I believe claim 2 does further limit claim 1, yes. It's a --

Q. And you're --

A. It's a defendant claim. I'm sorry. It's a defendant claim. From claim 1 it further limits

claim 1.

Q. And you're saying that claim 2 excludes copying data between system memory locations on the secondary processor, right?

A. I think that's accurate because claim 2 says "without copying data between system memory locations on the secondary processor."

Q. And you're saying that claim 2 further limits the scatter loader controller of claim 1, right?

A. That's one of the things I'm saying here because it says -- I mean, claim 2 starts "The multi-processor system of claim 1 in which the system" -- "the scatter loader control is configured," and then it goes on. So one of the things it's doing is it's limiting the configuration of the scatter loader controller from claim 1.

Q. And so in claim 1, it allows copying data between system memory locations on the secondary processor, but claim 2 does not; is that right?

A. I would not agree with that characterization because claim 1 -- there's certain important things that claim 1 does limit. If you look at the

variety of limitations in claim 1, claim 1 includes a limitation "to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory." And that limits -- that -- in fact, that excludes copying between system memory locations for the received data segments.

Q. So how do you think claim 2 further limits claim 1?

A. As I say in my expert report, and here I am reading the very last sentence of paragraph 45, I say: "I note that claim 1 recites the term 'data segment,' and claim 2 recites the term 'data.'"

I'll also note additionally that claim 2 says -- includes the limitation where "the software loader controller is configure" -- "configured to load the executable software image directly from the hardware buffer to the system memory of the secondary processor"; whereas, claim 1 says "to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory."

Q. So what is it about claim 2 that you think further

limits claim 1?
A. The use of the term "data segment" in claim 1 and "data" in claim 2 as well as, again, the use of the term "data segment" in claim 1 and the use of the term "software image" in claim 2. Those are two differences between --
Q. Do you agree with --
A. I'm sorry. Those are two differences between claim 1 and claim 2.
Q. Do you agree with me that "data" is a broader term than "data segment"?
A. I would say that often depends on context, and you would have to consider the context carefully. In this situation, I think that there are things that you could potentially consider to be data that are not necessarily data segments in the context of this patent and these two claims.
Q. Do you agree with me that a data segment is data, right?
A. I would say the data segment contains data, but there's -- I will also point out that the term data segment has been litigated extensively in this

case. There's a lot of nuance here and conditions here that we're going to have to go through if we're going to get deep into it. I'm going to have to ask you to show me various documents and trial testimony to get deep into it.

Q. So you have got a sentence here that reads: "Claim 2 further limits the data loader controller element by adding limitations on how it directly loads into system memory, specifically expressly excluding copying data between system memory locations on the secondary processor."

You see that sentence, right?

A. Just to keep the record clean, I believe you read that sentence inaccurately. I think you said "data loader controller" instead of "scatter loader controller."

Q. Okay. Now, you say there "Claim 2 further limits." What do you mean by "further limits"?

A. All I'm saying is that I'm referring here to the first sentence of the claim 2 where it says "The multiprocessor system of claim 1 in which the scatter loader controller is configured to," and

then the claim goes on. So that's what I'm referring to. I'm referring to the first part of the sentence of claim 2.

Q. What do you mean by "further limits"?

A. It just says, "further limits the scatter controller." The configuration of the scatter controller, set scatter loader controller. If you look at claim 1 --

Q. I'm sorry.

A. -- you will see that claim 1 includes a scatter loader controller configured and then there are several claim elements, and further to -- and in claim 2 further limits the configuration of the scatter loader controller as laid out in the following text in claim 2.

Q. So by "further limits," you mean adds an additional feature to it?

MR. NIGHTINGALE: Objection to form.

A. I wouldn't put it that way at all.

BY MR. HAAG:

Q. Sir, I'm just trying to understand what you think "further limits" means in your sentence. What does

that mean?

MR. NIGHTINGALE: Objection to the form.

A. I would say that it imposes -- I'm sorry. I didn't -- can I hear the question again to be sure we're on the same page?

BY MR. HAAG:

Q. What does "further limits" mean in your paragraph 45?

MR. NIGHTINGALE: Same objection.

A. I understand you to be asking me about the next to last sentence in claim 45. I think I'm saying that it adds an additional requirement to the configuration of the scatter loader controller as laid out in claim 2. I'm finding it difficult to give you a more precise answer than simply reading back the language of claim 2 because I think that the language of claim 2 is clear on how it further limits the configuration.

BY MR. HAAG:

Q. And you say "specifically expressly excluding copying data between system memory locations on the secondary processor," right?

A. I believe -- I believe that sentence directly copies the language from claim 2.
Q. So are you saying that claim 1 allows copying data between system memory locations on the secondary processor and claim 2 does not?
A. Let me be precise here. What I'm saying is, claim 1 expressly says in the claim element to "scatter load each received data segment based at least in part on the loaded image header directly from the hardware buffer to the system memory."
That claim element rules out any copying of data segments between system memory locations on the -- in between system memory locations and I suppose I should say on the secondary processor in claim 1.
Q. So then, in your view, how does claim 2 further limit claim 1?
A. Claim 2 uses the term "data" instead of "data segment," and it uses the term "executable software image" directly from the hardware buffer instead of using each received data segment based at least in part on the loaded image shutter directly from the

hardware buffer to the system memory. Those are two of the differences between claim 1 and claim 2.

Q. If you could turn to paragraph 21 of your declaration.

A. Sure. I'm there.

Q. Right about in the middle of that paragraph, you refer to final locations in system memory. Do you see that?

A. Please give me a chance to read the paragraph.

Here you are referring to, again, the next to last sentence in that paragraph where the sentence refers to Figure 3?

Q. Yes. It refers to final locations in system memory. Do you see that?

A. I do see that. That's, again, referring to final locations in system memory 305 referencing Figure 3.

Q. What do you mean by "final locations"?

A. It means in this case the locations where they are -- that means they're final locations. That means they're not copied to any other location.

Q. If you turn to your declaration to paragraph 9 --

A. Okay. I'm there.
Q. On this page you referred to a couple -- I think they're books by Hennessy and Patterson.
A. Yeah. You are referring here to Hennessy and Patterson, "Computer Architecture-A Quantitative Approach," the fourth and fifth editions.
Q. And are those books?
A. Yes, they are.
Q. And I think you have portions of at least one of those in Exhibit 2014, right?
A. Let me check that. Let me see what we have here. It's a long book. I'm not going to try on what is and isn't present in Exhibit 2014. I think we can go on here if you have got some specific part of the book you are interested in.
Q. I just have a couple questions. I mean, this is your exhibit that you attached to your declaration, right, Exhibit 14?
A. I referenced the book, I attached it to -- I presume it's been filed with my declaration. Whether what I'm seeing on the screen before me or not is the full book or not, I'm not going to try

to take a position on that issue without doing a lot of examination, and I don't think we need to do that right here.

Q. The full book is longer than 77 pages, though, right?

A. Yes.

Q. I think this exhibit is 77 pages, right?

A. Let me see. That's what the PDF reader says.

Q. Okay. So we can agree that Exhibit 2014 is at least some excerpts from a Hennessy and Patterson book, right?

A. I think that's a logical conclusion based on what you told me. Yeah, I think it goes directly from the table of contents to chapter 5. Presumably in the book there's chapters 1 through 4 as listed in the table of contents.

Q. So you selected the portions you thought were the most relevant to include this Exhibit 2014; is that fair?

A. I selected the portions of these books I thought were most relevant and cited them in my declaration.

Q. And it looks like Exhibit 2014 is the fourth edition of the Hennessy and Patterson book; is that right?
A. That's what it says.
Q. And why did you cite the Hennessy and Patterson books?
A. Just for background. They are known books in computer architecture. I'm familiar with them. I'm familiar with the series from various other editions, and I thought it was useful background.
Q. Are you saying that the Hennessy and Patterson books are well-known books in architecture?
A. Yes, they are very well known.
MR. NIGHTINGALE: Objection, foundation.
A. Let me clarify. I would say they're very well known to people in computer architecture that I know and, of course, myself and people in computing work generally tend to be very aware of this book. It's a standard textbook used throughout, you know, many computer architecture courses.
BY MR. HAAG:
Q. So you refer to Figure 5.2 on page 289 of

Exhibit 2014. Do you see that?
A. Are you asking do you see where I refer to it or do I see Figure 5.2?
Q. Well, do you see where you refer to it?
A. Yeah. It's about the middle of the paragraph 9, I believe.
Q. Okay. Now, can you find that Figure 5.2 on page 289 of Exhibit 2014?
A. Sure. I see Figure 5.2.
Q. The first sentence with the caption of Figure 5.2 says "Starting with 1980, performance as a baseline, the gap in performance between memory and processors is plotted over time."
Do you see that?
A. I do see that sentence.
Q. And then it goes on and in the next sentence it refers to DRAM.
A. Mm-hmm.
Q. Right. So am I right that Figure 5.2 is comparing processor to DRAM memory?
A. I'm not sure I understand your question. It's comparing the performance gap between a processor

and DRAM.
Q. So Figure 5.2 is comparing the performance gap between a processor and DRAM?
A. It's presenting a performance gap between processors and DRAM.
Q. Am I right that DRAM is a typical type of external memory?
A. I would say that DRAM is often used as a form of memory in many computer systems. In fact, the majority of computer systems that you would see in a laptop or a desktop, and it has been for several decades.
Q. And typically that DRAM is external to the processor chip, right?
A. Can you clarify what you mean by "external"?
Q. A separate chip.
A. It is often a separate chip or -- a separate chip or in some cases chips.
Q. From the processor, right?
A. That's my understanding, yes.
Q. And am I right that DRAM is typically made using a separate process technology from a processor chip?

A. Can you be more specific by what you mean by "process technology"?
Q. Yeah, I'm talking about the manufacturing technology in a fab?
A. You mean fabrication technology?
MR. NIGHTINGALE: Objection to scope, relevance.
BY MR. HAAG:
Q. Correct.
A. Often that can be the case, yes.
Q. So DRAM is typically made from a different fabrication technology than the processor chip; is that fair?
MR. NIGHTINGALE: Objection, scope, relevance.
A. It would help me answer the question if you could give me some idea of what you're trying to figure out here.
BY MR. HAAG:
Q. I'm just trying to figure out if the fabrication technology is typically different for DRAM compared to a processor chip.

A. It can be, yes. And what you refer to here as -- and, you know, I don't know how deep you want to get into this, but in a fab, you have a sequence of steps that you use to manufacture various computer chips, and those have different technologies, and, you know, you can make processors in a whole wide range of technologies. You can make DRAMs and other kinds of RAMs as well in a whole range of technologies. And often you'll mix different kinds of technologies together into a computer system for a variety of reasons, including costs and other kinds of -- costs, density, other kinds of constraints. So in general, you would expect to see a computer system, say, over the last several decades, incorporating multiple chips and, you know, these chips may have been manufactured on fab lines that use kinds of technologies, sure.

Q. I'd like you to turn to the previous page of Exhibit 2014.

A. Okay.

Q. And there's a Figure 5.1 shown there, right?

A. Yes.

Q. And it shows the levels of a typical memory architecture, right?
A. The first sentence of Figure 5.1 says "The levels in a typical memory hierarchy in embedded, desktop, and server computers."
Q. And on the -- on Figure 5.2, this comparison between performance of processor and memory, there's a memory listed. Is that memory shown in Figure 5.1?
A. That specific memory.
Q. The memory referred to in Figure 5.2.
A. Well, if you like at 5.2, it is -- the X axis covers a range of times from 1980 to 2010, so, of course, there's not any one specific memory. And in Figure 5.2, it's plotting the performance of a range of memories over time.
Q. Yeah. And what type of memory is that shown in Figure 5.2? Is it also shown in Figure 5.1?
MR. NIGHTINGALE: Objection, form.
A. In general, I would expect 5.2 to be talking -- the line that says "Memory" to be referring to DRAM memory. And I would say Figure 5.1 is more general

than that potentially, but in practice, the figure labeled "Memory" -- the box labeled "Memory" in 5.1 could be and often is implemented in DRAM, but it doesn't have to be implemented in DRAM.

BY MR. HAAG:

Q. So the box labeled "Memory" in Figure 5.1 often would be implemented in DRAM. Is that fair to say?

A. It could be. I mean, many computer systems -- but, again, you've got to realize 5.1 is an abstraction of the actual architecture that occurs in many computer systems. If you look at the corresponding figure from the next edition of the machine, you'll see a slightly different architecture. This is a conceptual architecture that's intended for -- to give you an idea of what's going on. There have been systems that have been built with this specific -- with an architecture that is captured accurately, 5- -- Figure 5.1, but there are other architectures as well. This is intended to be a conceptual overview of the kinds of levels that you see in a memory hierarchy.

Q. Now it shows a CPU, and it's got registers in it,

right?
A. You're referring here to the circle in Figure 5.1 labeled "CPU" and inside has a box called "Registers." That's correct.
Q. And it's got a size and speed listed below that circle.
Do you see that?
A. I do.
Q. And what does that speed indicate?
A. Okay. So let's see if we can --
MR. NIGHTINGALE: Objection, relevance and scope.
A. So what I'll -- so if you look at the very first paragraph under 5.1 Introduction, the very last line says "Figure 5.1 shows a multilevel memory hierarchy, including typical sizes and speeds of access." And I'll note that these numbers have changed over time, so this is something that would be typical as of the time that this book was written, and things may have changed later on.
BY MR. HAAG:
Q. Yeah. So the speed there refers to speed of

access?
A. Again, speeds of access, and I think that's what is explicitly stated in the last sentence of the first paragraph of Section 5.1 Introduction.
Q. Figure 5.1 of Exhibit 2014 shows that the speed of access of the CPU and its registers is about 250 picoseconds, right?
A. I don't think that's an accurate characterization of how I would interpret this. I would say the accurate characterization is this is a typically speed of access for the registers. And I'll just, you know, remark here that registers are -- I mean, I don't know how deeply you want to get into this, but registrars are distinct from the memory hierarchy in the way that they're accessed by the instructions of architecture. I can go as far as you want to into that.
Q. So Figure 5.1 shows that the typical speed of access for registers is about 250 picoseconds?
MR. NIGHTINGALE: Objection, scope.
A. Again, let's bear in mind that this is written as of a certain date, and that is -- that time's going

to be -- is going to be typical as of that date according to the authors of the paper, but on any machine and in particular as machines change over time, that speed's going to change. And, in fact, I don't know that 250 picoseconds specifically is going to be the exact access time for any machine. It's going to be a typical range. That's how this is --

BY MR. HAAG:

Q. Okay. I understand. It's typical range of typical speed, right?

A. It's intended to give -- you know, again, a range or a ballpark of where you might be at for these systems at this point in time.

Q. I mean, is it what it's intended to do is compare a speed of access of CPU registers versus cache versus memory versus I/O devices? Is that what Figure 5.1 is trying to do?

MR. NIGHTINGALE: Objection, form, scope, relevance.

A. I would hesitate to characterize a figure as having an intention. I'll just say the information in the

figure provides, again, ballpark indications of what the speeds of access of the various components labeled in the figure would be, so that would be, for example, registers, cache, memory, and I/O devices as the components of the figure labeled in the figure.

And, again, I'll just -- I'll just remark that these things change over time, and this is intended to be a typical and it isn't -- I would not expect it to be the case that if you looked at any specific system, you would find exactly these numbers in that system.

BY MR. HAAG:

Q. So for the cache Figure 5.1 lists the typical speed of access of 1 nanosecond, right?

A. If you look at the Speed column at the bottom of Figure 5.1, it says "1 ns," and that's nanoseconds. And if you look at the size, it's 64 kilobytes. And, again, I just want to emphasize that these numbers change over time, and they're intended to be -- give you a typical idea of what's going on. They're not intended to -- to capture the

characteristics of any specific system.
Q. And so in Figure 5.1, the cache speed of access is on the order but slightly larger or slightly higher than the register access time; is that right?
A. Why don't I --
MR. NIGHTINGALE: Objection to scope, relevance.
A. Why don't I just read the numbers off the figure? Figure 1 says speed of 250 picoseconds for "Register reference" and 1 nanosecond for "Cache reference." Again, those are typical numbers as of that time, not any specific system, and it will change over time.
BY MR. HAAG:
Q. And in the label for Figure 5.1, it says:
"As we move further away from the processor, the memory in the level below becomes slower and larger."
Do you see that?
A. I believe you read that sentence correctly from the caption of Figure 5.1.
Q. And what does that sentence mean in Exhibit 2014?

MR. NIGHTINGALE: Objection, form.
A. So this is a standard concept in computer architecture, the concept of a memory hierarchy, and that in computing more generally, and what you'll see is it's referring to something called a hierarchy which is an ordering of the memories according typically to size, and as you go away from the CPU to the right toward's the I/O devices passing through the cache and memory, as those things are labelled, you'll see that these -- the cache is larger than the registers, the memory is larger than the cache, I/O devices are larger than the memory. And as the sizes of the cache, memory, and I/O devices get larger and larger as you go out there, the access time or the speed of -- I think they call it speed of access gets slower.
Q. I'd like you to turn --
MR. HAAG: Does someone have a phone on or something that's beeping?
BY MR. HAAG:
Q. I'd like you to turn now to page 311 of Exhibit 2014. This is the Hennessy Patterson book.

A. Sure. Let me see. Take me a little while to get there. Okay.
Q. And there's a section on page 311 that relates to "SRAM Technology."
Do you see that?
A. I do.
Q. Do you know what SRAM means?
A. So as it says, the first letter of SRAM stands for static, so SRAM typically stands for static RAM.
Q. And right above the title "SRAM Technology" on 311, there's a sentence that reads "Virtually all desktop or server computers since 1975 use DRAMs for main memory, and virtually all use SRAMs for cache."
Do you see that?
A. I do see that sentence.
Q. And do you agree that virtually all computers use SRAM for cache?
A. There's a couple caveats there. First of all, this is referring to the time frame in which this book was written, and I think we've gone past that time frame now. Second, I believe not all desktop or

server computers since 1975 did have any cache at all.

Q. But you agree that SRAM typically is used for cache, right?

A. In this time frame, SRAM is a typical way to implement that cache.

THE REPORTER: I'm sorry. SRAM is a typical way to?

A. Implement that cache.

THE REPORTER: Implement. Thank you.

A. And that -- and, again, this is the main processor cache that sits between the processor and the main memory as of the publication time of this book, as I think laid out in -- as illustrated in -- what page is this? What figure is this? I'm going to back to -- yeah, 5.1.

Again, I'm going to say that, in actuality, many machines have more involved and complicated cache hierarchies than you see in Figure 5.1, although Figure 5.1 could be seen as an accurate representation of many machines.

But, again, let's be sure we have that

caveat in there. If it becomes important to talk about the details of caches and all the specific architectures, we have got to get into that.

Q. You do agree that virtually all computers use SRAM for cache, right?

A. Again, there's a time frame involved. There's a caveat that as of 1975 -- 1975 to 1980 time frame, not all computers had a cache at all, and even today you may find computers without a cache.

So I would say more to the point that desktop computers, server computers in the time frame covered by this book in this sentence, I think it's accurate to the extent that they have a cache, they would use SRAM, they would implement that cache in SRAM.

Q. And then under the section on SRAM technology, there's a sentence that says "S-RAMs don't need to refresh, and so the access time is very close to the cycle time."

Do you see that?

A. I do see that sentence.

Q. What does it mean for "the access time to be very

close to the cycle time"?
A. Okay.
MR. NIGHTINGALE: Objection, compound.
A. Now I've got to go back and talk about the cycle time. Let's see where we are here. Let's go -- see -- okay. So, for example, can you go to page 291 of Hennessy and Patterson?
BY MR. HAAG:
Q. Okay.
A. Okay. See there is a bullet there called 4?
Q. Okay.
A. Do you see where it's talking about "multilevel caches to reduce miss penalty"?
Q. Okay.
A. In figure -- I believe it's 5.1, there is a single level cache. You will recall that earlier I was speaking about different cache architectures. So in different cache architectures, you may have multiple levels. So instead of having a single level cache, you would have a cache that compromises multiple levels.
And I think if you go to the fifth

edition of this book, you will see in the figure corresponding, Figure 5.1, they have a more elaborate multilevel cache hierarchy there, although we have to go to that figure to be sure that's illustrated there.

Now, so what we're talking about here is, you will see about midway down, that paragraph, it says, "The first level cache can be small enough to match a fast clock cycle time."

So what they're talking about here, and then they say "yet the second level cache can be large enough to capture many accesses that would go to the main memory." Now they're talking about a more complicated cache architecture that has two levels in it. And when you see "match a fast clock cycle time," now we need to get into what clock cycle time is.

It turns out that modern processors are something called synchronous circuits where the operation of the circuit is driven by something called a clock. It ticks every now and then. That ticks on a regular basis and drives the operation

of the processor.

So in this time frame, what they're referring to is in some computers, you can make the access time of the cache fast enough to match the clock cycle time, and the clock cycle time here is the clock, the cycle time of the clock. It drives the operation of the machine -- of the processor and that part of the machine.

It doesn't actually obviously drive the operation of thing likes the I/O, the I/O devices, those components.

Q. So the time cycle time is the clock speed of the processor?

A. No, no, no, no. It's not the clock speed of the processor. Cycle time is -- so the processor has a clock. That's what they're talking about here. Again, it's an abstract. If you get into the architecture, you can have architectures that have multiple cycle -- it can get very, very complicated because these machines have been engineered extensively over time to extract the most performance out of them.

What they're talking about here is a conceptual system where you have a clock that drives the execution of the processor, which was typical several decades ago. Every time the clock ticks, the processor takes an action because it's a synchronous circuit.

Q. So then if the access time is very close to the cycle time for SRAM, that's saying that the SRAM access time is close to the cycle time of the clock of the processor?

A. Are you back on page 311 now?

Q. I was referring to the cycle time on 311, yes.

A. Okay. Let me see here. Yeah, let me -- again, let me go through this and be sure that we're on the same page. I'm reading through here just to be sure I have all the context in my mind as I answer your question.

I'm still going to make sure we have got all the context. So in this part of Hennessy and Patterson, they define cycle time above where it says, "Cycle time is the minimum time between request to memory." You will see that at the

bottom of page 310 and the top of page 311.

I will note that cycle time is also used in the field to talk about the clock cycle time with processing. Here they are defining it to be the minimum time between request to memory, which is often related to the processor cycle time.

Q. My computer is just a bit slow, so bear with me. I'm just trying to get back to page 311.

A. Okay.

Q. Are you back at page 311?

A. Yes, I am.

Q. The second full paragraph the first sentence reads, "SRAM designs are concerned with speed and capacity while in DRAM designs emphasis on cost per bit and capacity."

Do you see that?

A. I do see that sentence.

Q. Do you agree with that?

A. I think in the context of this book, that's broadly accurate. I don't disagree with it in this context. Obviously in another context, there may be other considerations, and every individual

design has different considerations that drive different -- different concerns. But in general across computers in this time frame, I would agree that in the context of this book it's roughly accurate.

Q. Do you agree that the cycle time of SRAM is faster than DRAM?

A. As defined in this book, in the context of this book and this page, it says "The cycle time of SRAMs is 8 to 16 times faster than DRAMs," and that is the first part of the last sentence of the SRAM technology section on page 311. So I think 8 to 16 times faster is indeed faster.

Q. Do you agree that SRAM is faster than DRAM?

A. Again, in the context of this book, the systems they're talking about at the level at which they're talking about, that's typically true, yes.

Q. Do you agree that SRAM is typically implemented on a chip with the processor?

A. That is one, but not the only way to do it.

Q. Do you agree that that's typical?

A. It's often done that way. I would hesitate to

characterize it as typical or not.
Q. Do you teach using the Hennessy and Patterson books?
A. I don't recall if I recommended those over the years. I typically teach from materials that I have prepared myself, and we have textbooks that are recommended. I don't recall if I recommended that textbook or not. Yeah, I just don't recall.
Q. I'd like you to pull up your copy of the Patent '949.
A. Okay. It's going to take me a bit to get there.
MR. NIGHTINGALE: Counsel, we have been going for about an hour. Would now be a good time to take a quick break?
MR. HAAG: That's fine. Sure.
(Off the record at 7:58 a.m.)
(Back on the record at 8:10 a.m.)
BY MR. HAAG:
Q. Am I right that the data segment is copied from the hardware buffer and written to the system memory in the claim 1 of the '949 patent?
A. Let's take a look at claim 1. I wouldn't

characterize it necessarily as being copied from the hardware buffer to system memory. I would say that it is scatter -- again, we're referring to the claim element to scatter load each received data segment based at least in part on loaded image header directly from the hardware buffer to the system memory. So the claim language talks about scatter loading from the hardware buffer to the system memory.

Q. To get from the hardware buffer to the system memory, the data segment needs to be copied from the hardware buffer, right?

A. I think you need to interpret what is going on here precisely. I would hesitate to use the word copy in the context of this patent in this claim.

Q. To get from --

A. I'm sorry. So just to clarify, what's going on is the pieces -- as the data segment in figure -- for example, let's take a look at Figure 3. Maybe that will clarify things.

So here we are in Figure 3 of the '949 patent, and it's illustrating the flow by which the

data segments are scatter loaded into the system of the secondary processor. It goes through the hardware buffer to get there. So I would say it's transferred through the hardware buffer and scatter loaded from the hardware buffer into the system memory.

Given the way that the copying -- the term copying has been used in this case, I don't think that's -- you know, I would hesitate to use the word copying to describe that operation. I think it's more precise to say it's transferred or loaded from.

Q. To get from the hardware buffer to the system memory, doesn't the data segment need to be read from the hardware buffer and then written to the system memory?

A. Again, we have got to be careful here because in the kind of transfers that we're talking about here, it's a flow. So you don't -- it's not as if you take the entire data segment, put it in the hardware buffer, and then copy the hardware buffer into the system memory. Instead the data segment

flows through conceptually the hardware buffer.
Q. But somehow it has to get out of the hardware buffer, right?
A. Yes. I believe claim 1 says it's scatter loaded from the hardware buffer to the system memory.
Q. Doesn't that mean that the scatter loader controller needs to access the hardware buffer to read the data segment?
A. Again, I think we're getting beyond what the claim specifically requires. It is true that as the pieces of the -- see, most -- most modern computer systems, when they -- when it flows like this, transfer the flow in chunks or pieces. As those pieces flow through the system, they are transferred from, in this case, the hardware buffer into the system.
Q. And doesn't the scatter loader controller need to access these chunks of the data segment in order to get them to the system memory?
A. I would say that it has to -- that it has to orchestrate or coordinate the movement of the data.
Q. So the hardware buffer has to orchestrate the

movement of data from the hardware buffer to the system memory?

A. I believe you asked me about the scatter loader controller. If you look at claim 1, it is the secondary processor comprising, and then it says "a scatter loader controller configured to scatter load." So I believe it's the scatter -- I would say, again, speaking roughly about what's going on in claim 1, it's the scatter loader controller that is causing the data segment to get transferred directly in -- from the hardware buffer to the system memory.

Q. So the scatter loader controller orchestrates the movement of data segments from the hardware buffer out of the hardware buffer and into the system memory, correct?

A. Yeah. And just to be precise, it's configured -- again, I'm reading from the claim language. It says "a scatter loader controller configured" -- and then I'm skipping -- it says "the scatter loader controller configured to load the image header and to scatter load each received data

segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory." And what that is referring to is it's configured to make that happen, and the way I described that is orchestrated or coordinated. But I think you need to look at the claim language to be precise about exactly what's going on here.

Q. The scatter loader controller in the '949 Patent orchestrates the movement of data segments from the hardware buffer out of that hardware buffer and into the system memory, correct?

A. Let's be precise here. The claim language says it's configured. The scatter loader controller is configured "to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory." And as part of that scatter loading, the data moves through hardware buffer and into the system memory.

Q. And how does the data segment get out of the hardware buffer?

A. I'm not sure I understand the question.

Q. So in claim 1, the hardware buffer receives data segments, right?
A. You're referring here to the claim element "system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image"?
Q. Yes.
A. Okay. So it says there the hardware buffer -- I'm read that to say the hardware buffer receives at least one data segment. And, again, you have to understand this in the context of the patent where it isn't as if the entire data segment hits the hardware buffer all at once; it flows through the hardware buffer, so the hardware buffer is receiving the elements of the data segment.
Q. So if hardware buffer receives the elements of the data segment, and then the data segment needs to get out of that hardware buffer, right?
A. It's -- I mean, I prefer to stick with the claim language where it says it's scatter loaded from the hardware buffer directly to the system memory. And it is true --

Q. Something --
A. And it is true that the data moves from the hardware buffer into the system memory as part of the flow.
Q. So does the scatter loader controller read the data from the hardware buffer?
A. I'm not seeing any requirement that states in claim 1 that the scatter loader controller has to read it.
Q. Well, look, it's not magic. Somehow the data has to get out of the hardware buffer, right? I'm just trying to figure out how that happens, okay?
A. Yeah, sure. I mean, if you look at Figure 3, you'll see a line, you know, going from the controller to data segment 4 still transferring so the controller causes something to happen to the data in the hardware buffer so that it gets into the system memory.
Q. How does that work? Is that a -- is that a read of the hardware buffer?
A. That would completely depend on the way in which the hardware buffer and more generally whatever the

system components the hardware buffer's part of is implemented.

Q. But how would a hardware buffer be accessed by a scatter loader controller so that it can orchestrate movement of data out of the hardware buffer?

MR. NIGHTINGALE: Objection, form.

A. Yeah, again, why don't you ask -- I mean, I think if we stick to the claim language, life would be more precise and we'll understand each other better here.

BY MR. HAAG:

Q. Sir, I know what the claim says. I'm not asking you exactly what the claim says; I'm asking you how it would work, okay?

A. And --

Q. I can read the claim, and I see what it says.

A. Okay. Good. So then I think I would say that would depend on the specific system that you're talking about.

Q. But we agree that it's not magic how the data gets out of the hardware buffer, right?

A. I think I shouldn't --

MR. NIGHTINGALE: Objection, form, asked and answered.

A. Look, there's -- there's a variety of ways of implementing this -- this particular thing that we're talking about here, and I don't want to -- I'd have to hypothesize a system and then tell you how that system works to answer that question that you're asking me.

BY MR. HAAG:

Q. Well, can we agree that the scatter loader controller needs to access the hardware buffer to access a data segment in order to orchestrate the movement of that data segment to the system memory?

A. No.

MR. NIGHTINGALE: Objection, form, asked and answered.

BY MR. HAAG:

Q. Why -- why is that?

A. Because there may be other ways of doing it.

Q. How?

A. You are asking me to hypothesize a system that

would do it in some other way.
Q. I'm asking you to tell me some way that's not magic that -- that could get of the hardware buffer by using the scatter loader controller.
A. The scatter loader controller could -- and, again, I'm being very general here at a high level. There's a variety of ways a scatter loader controller could do it, and some of those ways do not involve the scatter loader controller itself, accessing the hardware buffer, but merely causing the system to transfer the data directly from the hardware -- from the hardware buffer directly into the system memory. The scatter loader controller itself doesn't need to access the hardware buffer to make that happen.
Q. Doesn't something need to access the hardware buffer to get the data segment out of it and into the system memory?
A. I wouldn't characterize it as access. It is true that the data does need to flow from the hardware buffer into the system memory, and one of the ways of doing that is to have wires that connect the

hardware buffer to the system and via some number of other system components. There's a lot of ways you can make that happen. I wouldn't say that the scatter loader controller itself has to access the hardware buffer to make that happen.

Q. But you agree that something has to access the hardware buffer to get data segments out of the hardware buffer that's orchestrated by the scatter loader controller.

A. I don't like the term "access" because it contains connotations that I don't necessarily agree with in all -- in all possible systems that could -- that could do what claim 1 is saying they should do.

I agree that the data does need to get somehow from the hardware buffer into the system memory.

Q. Under the control of the scatter loader controller, right?

A. Yeah. It says that -- let me read claim 1 again. And I'm not going to quote it back to you, but I think that's what we're talking about. And the way I'm reading scatter -- claim 1 is that the scatter

loader controller has to configured -- again, you can read the relevant section -- all it has to do is be configured to scatter load it, and I don't agree that given all of the connotations that the term "access" has in this context that the scatter loader controller or itself has to access the hardware buffer to make that scatter load happen.

Q. But one way to implement claim 1 would be to have the scatter loader controller access the hardware buffer to get a data segment out of that hardware buffer and into system memory, right?

A. Could you give me a more specific system -- system configuration that you're thinking about here?

Q. No.

A. So you're asking me is there some hypothetical system that I could manufacturer up on the -- on the spot here that would do that?

Q. Yes.

A. Let me think about that a little bit.

MR. NIGHTINGALE: I'm going to object to form. It calls for speculation.

A. You know, I don't want to get too far outside the

bounds of my expert report. Clearly, there are some systems where you would read the data, read portions of the segment -- read portions of the image -- let me just make sure I'm using the right words here.

Yeah. There are systems where you would read the -- read some portions of the data segment as part of flow out of the hardware buffer and in that way scatter load it into the system memory.

BY MR. HAAG:

Q. So one way to implement claim 1 would be to read portions of the data segment from the hardware buffer --

A. Let me --

Q. -- and then load them into system memory, right?

A. Let me verify. So there's a flow going on here. One way -- I mean, one way of doing this is to have a flow going on where the image segments flow through the hardware buffer, and as part of that flow, they might be read from the hardware buffer and then placed into the system memory via some mechanism. That's a possible way that that

implementation could be part of one way to do claim 1.

Q. Can you tell me any other way to do claim 1?

MR. NIGHTINGALE: Objection, form, scope.

A. You know, any way where the data moves from the hardware buffer into system memory where the -- where the transfer is direct, I think would be satisfy the limitations of the claim. I don't know that you'd necessarily -- I could imagine there would be systems where you wouldn't describe what's happening as the data being read out of the hardware buffer.

BY MR. HAAG:

Q. Can you tell me any specific ways to do that?

MR. NIGHTINGALE: Same objection.

BY MR. HAAG:

Q. So just so we're clear right now, you told me one way to do that, which is to read the data from the hardware buffer. I'm trying to figure out if there's any other way to move the data from the hardware buffer to the system memory in your view?

A. Yeah. I mean, you could set certain switches. You could build a system where you'd set switches that would cause it to move. I'm reluctant to get very deeply into this because I don't see how it's relevant, and I certainly didn't go this deep into -- yeah, so I think I said I'm reluctant to get this far into it without understanding what the -- what the purpose of the question is and where we're going.

Q. So aside from reading data out of the hardware buffer, can you tell me any other way to get the data out of the hardware buffer to the system memory for claim 1?

A. I believe I --

MR. NIGHTINGALE: Objection, form, scope.

A. Again, you're asking me to come up with hypothetical systems here on the fly. I'm sure there are other ways to do it. It depends on how long you want me to try to come up with such ways of doing it.

Q. Right now you can't tell me any other way aside

from reading the data from the hardware buffer; is that right?
A. No, that's not right.
Q. Tell me any other way then.
A. I believe I mentioned the system where you would set certain switches that would cause that to happen.
Q. What would set those switches?
A. Well, potentially the scatter loader controller or some other -- you know, presumably, the scatter loader controller would be configured to set those switches in a way that would cause this to happen.
Q. That would be setting switches to access the hardware buffer to get data out of the hardware buffer?
A. No, I wouldn't describe it that way. I think in this context the term access has connotations that I would be reluctant to apply to the hypothetical system that we're talking about.
Q. How would it work then?
A. It would set the switches.
Q. How would setting switches -- describe for me in

detail how setting switches gets data out of the hardware buffer.

A. One of the things --

MR. NIGHTINGALE: Objection, form, scope.

A. One of the things that you can do when you set switches is you can affect the way the data flows. So it would affect the flow of data through the hardware buffer.

BY MR. HAAG:

Q. How?

A. Because it would determine where the data flows.

Q. What are these switches that you are talking about, these switches that you have mentioned?

A. They are switches that affect the data flow of the machine.

Q. How?

A. They switch and change how the data flows.

Q. Can you tell me how they would be implemented?

A. Sure. You have -- again, we are getting very deep into the architecture here. This is not, I think, a relevant part of the patent, but they can be

implemented in hardware.

Q. How?

A. Again, this is just one way that we're talking about here, and, you know, I can probably -- that's one way that we're talking about here.

How would they be implemented? There are a variety of ways of implementing hardware switches, the switches in hardware, and, you know, we can talk about that if you would like.

Q. So I'm just trying to understand your switches in hardware. Are you saying that the scatter loader controller would cause these switches to switch in a way that would cause data to move out of the hardware buffer? Is that what you are saying?

MR. NIGHTINGALE: Objection, form, scope.

A. Again, we're talking about a hypothetical, which is just one way of doing this. I'm not talking about any limitation that the patent is imposing on how this happens.

You asked me how could this happen. I'm discussing a hypothetical at some level. It's not

the only way. It's not a limitation of the claim. I want to make that very clear. Again, it could affect what I would call the flow of data through the hardware.

BY MR. HAAG:

Q. So I don't think you actually answered my question. So this is your hypothetical about how a system could implement claim 1, right?

A. You asked me about a variety of ways, and I'm trying to give you my best answer about different ways it could do it.

Q. But it's your hypothetical. It's the switch's hypothetical. That's not mine. It's yours, right?

A. It's a hypothetical.

Q. From you? You're saying that switches --

A. I wouldn't say --

Q. You said the switches could be used to somehow get data out of the hardware buffer. You said that, right?

A. I said it could affect the flow of data. I'm not saying the switches themselves actually get the data out of the hardware buffer.

Q. I'm just trying to figure out how, in your view, these switches could affect the flow of data out of the hardware buffer.
A. By changing where the data flows.
Q. How?
A. By switching it from one place to another.
Q. And what causes the switches to be switched?
A. In this hypothetical we're talking about here, which is very far away from any claim limitation, it's just one way of doing the claim that we're talking about. I want to make that clear.

They would change the flow of data. They would cause the data to flow into the right part of the system memory directly.
Q. The switch hypothetically you are talking about, it's not described in the '949 patent, is it?
A. That's right. You asked me about ways in which you could implement it. We're discussing multiple different ways. It's not discussed in the '949 patent. The '949 patent has a set of limitations. I want to be very clear here that we're not -- we're getting way down below the level of detail

that the patent discloses because the patent is claiming a certain way, a certain configuration at some level, and it's not limited to any of the things that I'm talking about right here necessarily.

Q. Claim 1 does not require any particular level of performance for scatter loading, correct?

A. Let me read claim 1. I would say it doesn't explicitly mention performance. On the other hand, the purpose of the entire purpose of the invention is to provide increased performance. One of the primary ways it does that is by limiting extraneous copy operations and eliminating use of various temporary or intermediate buffering operations used in previous prior art systems.

Q. But you agree with me that claim 1 doesn't explicitly require any level of performance, right?

A. I agree that claim 1 does not mention performance explicitly, but the purpose of the patent is to deliver, to enable increased performance in part by the elimination of temporary and intermediate buffering operations and additional copy operations

on the secondary processor characteristic of prior art systems.

Q. Claim 1 does not require any particular level of efficiency in scatter loading, correct?

A. Claim 1 does not explicitly mention efficiency, any efficiency measure, but the point of the patent is to enable efficient loading of images by eliminating copying, excess copying operations and excess temporary -- and use of temporary or intermediate buffers as in prior art systems --

(Reporter clarification.)

A. -- or intermediate buffering as in prior art systems over which the patent gets designed and approved.

BY MR. HAAG:

Q. We agree that claim 1 does not require any particular level of speed and scatter loading, correct? That's a yes/no question.

A. I'm not going to give you -- what I'm going to say is claim 1 does not mention speed explicitly. The purpose of the invention is to improve the performance of image loading in part by eliminating

the use of temporary and intermediate buffers as in prior art systems and eliminating excess copying operations between system memory locations as in prior art systems.

Q. So you know that the scope of the patent is limited by claims, right?

A. The claim and scope of the invention is limited by claims, by the claims. That's my understanding, yes.

Q. So the scope of the claims is not limited by some purpose of the patent? You agree with me on that, right?

MR. NIGHTINGALE: Objection, scope.

A. That's getting into a legal question, but I can tell you my understanding. My understanding is, if a system in this case because -- if a system satisfies every limitation, then it satisfies the claim. Otherwise, it doesn't.

And, again, that's my understanding as a technical expert. I'm not trying to put forth any legal opinion here.

BY MR. HAAG:

Q. Let's look at claim 22 of your declaration. That's Exhibit 2015.
A. Are you asking me about my declaration? Are you asking me to look at my declaration?
Q. Yes.
A. Okay. Where do you want when me to look?
Q. Paragraph 22.
A. I thought you said claim 22. I was not -- okay. Good. Yes, I see paragraph 22.
Q. So we're on paragraph 22 of Exhibit 2015, right?
A. Exhibit -- yes.
Q. And you say that hardware buffer is distinct from system memory, right?
A. Yes.
Q. So you mean that the hardware buffer cannot be the same as the system memory in claim 1 of the '949 patent; is that right?
MR. NIGHTINGALE: Objection to form.
A. I think it has to be distinct from system memory, for example, the system memory in claim 1.
BY MR. HAAG:
Q. You refer to a permanent dedicated buffer.

A. Uh-hum.
Q. Is a permanent buffer the same thing as a buffer that is not a temporary buffer?
A. I would say that a permanent buffer is not a temporary buffer. I wouldn't say it's the same thing as not a temporary buffer.
Q. A permanent buffer is not a temporary buffer; is that right?
A. The intention here is that permanent and temporary be different kinds of buffers. I'm sorry. The intention here is that a permanent buffer -- yeah, a permanent buffer isn't a temporary buffer because it's not temporary, it's permanent.
Q. Now, I'd like you to turn to paragraph 8 of your declaration.
A. Okay.
Q. And at the end of that paragraph, you refer to main or system memory of the computer often implemented in DRAM.
A. And it says, "storing data during the execution of a program is also part of that paragraph." It occurs right after the word DRAM.

Q. Do you use the terms "main memory" and "system memory" synonymously?
A. Certainly, there are people who could use -- who would use the term main memory when they're talking about system memory and system memory when they're talking about main memory. I would hesitate to say that they're exact synonyms.
Q. What's the difference?
A. I don't think -- one potential difference is the connotations of system memory where people often talk about system memories where, you know, you may have, you know, some other specialized memory, such as a GPU memory in the system, whereas main memory typically refers to the main memory of the, you know, main CPU, and I think system memory often refers to the main memory of the CPU as well. But they tend to use -- people tend to use system memory in slightly different context often to mean the same thing.
Q. DRAM is a common implementation of system memory; is that right?
A. Common, I would say -- we went through this earlier

in the deposition when we are talking about this Hennessy and Patterson, but, yeah, it's often -- but main or system memory is often implemented in DRAM.

Q. If you'd go to paragraph 10 of your declaration.

A. Sure.

Q. You refer to a write buffer.

Do you see that?

A. I do.

Q. Is a write buffer part of a cache?

A. That depends on your perspective. Some people would say it is, and other people would say it isn't. I think it's -- for me, it is part of the cache memory system and part of the memory system more generally, but it is not -- I mean, I think -- I think people would say -- I think many people would say that the write buffer is distinct from the cache, even though it's part of it, and it operates pretty closely with the cache.

Again, I could -- I could see other people saying colloquially that it's just -- that it's part of the cache or referring to it as part

of the cache when they're speaking about the system in a more abstract level.

Q. So a write buffer is typically part of the cache?

A. No, I didn't say that. It depends on how you're talking about the cache and the level of abstraction you're talking about. If you want to be precise, a cache -- a write buffer is a component that is part of -- is a component that makes the -- that is -- that interoperates with the cache, that works with the cache.

Q. So you earlier said, when I asked you about a write buffer you said, "I think for me it is part of a cache memory system." Is that true?

A. If you understand what I mean by cache memory system, here I'm referring to the entire memory system of the computer as seen, for example, in Figure 5.1 of the Hennessy and Patterson book that we were talking about earlier. There's a difference between the cache memory, which is just the cache itself, and the memory system, which can include a cache. And I said cache memory system in that answer. I believe I was referring to the

entire memory system.

Q. So where would a write buffer reside in this overall memory system?

A. You're -- logically, I think -- why don't we go to Hennessy and Patterson at 289. Maybe that'll clear things up here. Yeah, let's go to 289. They may even have a diagram. I don't know.

Okay. I'm still getting to 289.

Q. I think you meant page 288.

A. Could be. I mean, I'm still -- still trying to get there.

Oh, yeah. So let's look a little bit lower down where they may have a more detailed figure. Typically -- and, again, we're talking about a logical operation here. People would say as -- it would sit between -- again, logically, at this level of abstraction and different systems would have very -- could have different architectures when you bore down and look at the different level of detail, but in general, it would sit between the cache and the main -- and the main memory.

Q. So let's look at Figure 5.1 of Exhibit 2014, okay?
A. Sure.
Q. Where would a write buffer reside in Figure 5.1 in your view?
A. Again, logically somewhere between the cache and --
Q. And on the level of speed shown in Figure 5.1, at what level of speed would a write buffer operate?
A. That would vary substantially depending on the architecture, but it would have to be fast enough, as Hennessy and Patterson says: "to allow the cache to proceed as soon as the data are placed in the buffer rather than wait the full latency to write the data into memory." And that's, again, from Hennessy and Patterson, I believe fourth edition, and I'm quoting page 289. Let me see if I can find page 289. Yeah, it's the bottom of page 289.
Q. What -- what were you referring to at the bottom of page 289?
A. Look at the bottom of page 289. You asked me how fast or the speed of the write buffer. And it says the very last sentence on page 289: "Both write

strategies can use a write buffer to allow the cache to proceed as soon as the data is placed in the buffer rather than wait the full latency to write the data into memory."

It would be half the write buffer would be implemented efficiently enough to provide that particular characteristic to the -- to the machine.

Q. Could the hardware buffer in the '949 Patent be implemented as RAM?

A. Let's go take a look at the -- at my expert -- the remand declaration, paragraph -- I believe it's 22.

Wait. Come on. Okay. 16. Okay. 22.

So "'hardware buffer' should be construed as 'a permanent, dedicated buffer that is distinct from system memory,'" so that proposed construction focuses on one particular aspect of it. It doesn't focus on any specific technology for implementing it. I would say in some situations, depending on the kind of RAM that you're talking about, it could potentially be implemented as RAM, but, again, you'd have to take a look at the specific system and see that in the

context of the claim, that it makes sense for the hardware buffer to be implemented in that particular whatever technology you're talking about.

And, again, I'd point out that RAM here is not limited to DRAM. DRAM is a kind of RAM. And we also talked earlier about SRAM, which is static RAM.

Q. So a hardware buffer could be, in theory, implemented as SRAM?

A. Correct. In general, the construction that I'm putting forward here doesn't focus on the particular technology that it would be implemented in; it focuses on whether it's a permanent, dedicated buffer distinct from system memory. I would say that depending on the system and how well and -- and depending on the rest of claim 1, it could be implemented in certain kinds of RAM.

Q. Including SRAM?

A. And, again, I'm talking about there are many kinds of RAM as you see in Hennessy and Patterson Figure 1. Then these kind of RAMs have very many

different kind of access patterns. Static RAM is a kind of a RAM that has a certain kind of access patterns.

Q. So I'm just not quite sure I got the answer to my question, so I'll try it again.

A. Sure.

Q. Do you agree that the hardware buffer in the '949 Patent could be implemented in SRAM?

A. I see. So referring to paragraph 22 of my expert declaration, that focuses on -- on the -- that presents the proposed construction of the term "hardware buffer." The hardware buffer construction doesn't reference any specific memory technology or technology for implementing the buffer. I'll point out that if it satisfies all the other limitations of claim 1, then I don't see any reason why it couldn't be implemented in certain kinds of RAM, assuming that it satisfies the remainder of the requirements of claim 1.

And whether it made sense to implement it in any particular kind of RAM, in static RAM, dynamic RAM, any other kind of RAM, would depend on

the system that it had.
Q. So let's look at claim 1 of the '949 Patent again.
A. Sure.
Any particular aspect of it you want me to look at?
Q. Yes. I'm trying to find it here.
Yeah. The part of claim 1 that says "the image header and each data segment being received separately."
A. I see that.
Q. What does that mean?
MR. NIGHTINGALE: Objection, form.
A. This hasn't come up -- this certainly hasn't come up in my declaration. I would say that it just means that they have to be received separately, as the claim says.
BY MR. HAAG:
Q. So that means that the entire executable image is not received together in claim 1; is that right, by the hardware buffer?
A. Again, we're getting into parts of the interpretation of the claim. I would just say that

they have to be received separately, as the claim says. And I don't -- I would hesitate to go -- to characterize that as together or apart. I mean, I think we should focus on and stick with the language of the claim as best we can to be sure that we don't -- that we're understanding each other.

Q. So in the claims, the hardware buffer needs to receive the image header and the data segments separately; is that right?

A. Well, I mean, again, just to be precise, you have a system memory and a hardware buffer for receiving, and it's certainly those things together somehow have to receive the image header, in each case segment, and the image header and the data segment have to be received separately. And -- and certainly, the data segment are scanned, though, directly from the hardware buffer to the system memory. I wouldn't say the whole image is received necessarily by the hardware buffer itself in claim 1. I don't think claim 1 necessarily imposes that particular restriction that you just asked me

about on a hardware buffer.
Q. So the hardware buffer in claim 1 is not allowed to receive the image header and each data segment together, right?
A. I think it says they have to be received separately, and if you're using together as somehow not separately, then I think I would agree, but I think the more important thing is if they're not received separately, they're not -- if the system doesn't receive the image header and each data segment -- the image header and each data segment separately, then it doesn't fall within the claims -- the scope of the claimant. And, again, I'm just doing a logical transformation on the language of the claim.
Q. Are there permanent buffers that are less efficient than temporary buffers?
A. What's the scope of your question? Are you asking me in all of computer science?
Q. Sure.
A. Okay. So buffers are present in various different -- in fact, let me go to my expert

declaration here, and I think I can point you to something that's useful to you.

So let's see.

Okay. See paragraph 7 of my expert declaration.

Q. Just give me a moment please. And then --

A. So what I'm seeing here is that "Buffers that support the transfer of data are ubiquitous in computing generally." They "can appear in a wide variety of contexts, implemented in a wide variety of storage technologies, with the specific characteristics of the buffer specialized as appropriate for the context in which they appear." So you can have in some context -- not necessarily the context of the -- of claim 1 or the context of the '949 Patent -- in some contexts, you can have permanent buffers that have various access characteristics because of the context in which they appear.

Okay. And in the context of the '949 Patent and the context of claim 1, the temporary buffers that are described and -- as prior art to

the '949 Patent cause less efficient data -- they cause less efficient image transfers than the use of the hardware buffer as part of the direct transfer mechanism.

So you wouldn't achieve the benefit of the '949 Patent if the permanent buffer that you were using for that purpose was -- was slower or significantly slower than some temporary buffer of the kind referred to in the '949 Patent.

Okay. Outside the context of the '949 Patent, you can imagine permanent buffers being implemented in a wide range of technologies for a wide range of purposes. And I'm not going to tell you that outside the context of the '949 Patent in the broad scope of computing every permanent buffer is more efficient than every temporary buffer, again, in the broad scope of computing outside the context of the '949 Patent.

Q. You agree with me that it's possible to have a permanent buffer that is less efficient than a temporary buffer, correct?

A. Not in a --

MR. NIGHTINGALE: Asked and answered.

A. So, again, outside the context of the '949 Patent and, again, referring back to paragraph 7 of my expert declaration where I talk about the ubiquity of buffers in computing generally, throughout all of computing, you can find permanent buffers that have certain performance characteristics because of the context in which they're being used. You can find other temporary buffers in different contexts that have difficult performance characteristics because of the context in which they're being used. And I'm not going to tell you that every permanent buffer in every context is faster than any other temporary buffer that occurs in any other context.

But what I will tell you is that the permanent buffers and the -- or the hardware buffers in the '949 Patent are designed to provide performance characteristics that are -- improve on the performance characteristics that you'd get by using temporary buffers or intermediate buffers described in the prior art of the '949 Patent.

MR. HAAG: No more questions. Thank

you.

MR. NIGHTINGALE: Counselor, give us a few minutes and we'll see if we have any redirect.

Can we take a 15-minute break?

MR. HAAG: Yeah, I mean, if you need 15; I'll be back in 5.

MR. NIGHTINGALE: Sure. And I'll be back if we have a decision one way or the other ahead of time.

MR. HAAG: Okay. Off the record.

(Off the record at 9:00 a.m.)

(Back on the record at 9:00 a.m.)

MR. NIGHTINGALE: The patent owner has no questions.

MR. HAAG: Thank you, Dr. Rinard.

THE WITNESS: Thank you.

(The deposition was concluded at 9:00 a.m.)

CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

I, RENEE J. OGDEN, Certified Reporter and Notary Public within and for the State of Michigan do hereby certify:

That MARTIN RINARD, Ph.D., the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken before me and is a true record of the testimony given by such witness.

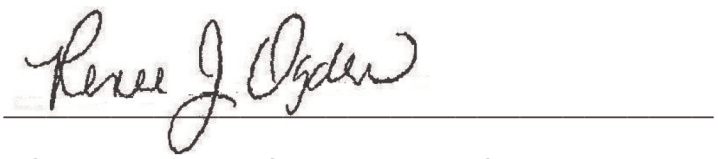
I further certify that the adverse party, QUALCOMM INCORPORATED, was represented by counsel at the deposition.

I further certify that the deposition of MARTIN RINARD, Ph.D., was conducted virtually via zoom on Friday, June 3, 2022, commencing at 7:03 a.m. to 9:00 a.m.

I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 10th day of June, 2022.

My commission expires:
June 21, 2025



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