UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01334[1]
Patent 8,838,949

REMAND DECLARATION OF DR. MARTIN RINARD

I, Martin Rinard, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorporated ("Qualcomm" or "Patent Owner") in the matter of the *Inter Partes* Review of U.S. Patent No. 8,838,949 ("the '949 patent"). I previously prepared and submitted my Declaration in support of Qualcomm's Patent Owner Response (Ex. 2007). I submit this Declaration in support of Qualcomm's Response Brief on Remand.

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding. All citations are to IPR2018-01334 unless otherwise noted.

2. Since preparing my Declaration in support of Qualcomm's Patent Owner Response, I have also reviewed the following materials:

a. Qualcomm's Sur-Reply (Paper 25);
b. Final Written Decision (Paper 30);
c. Federal Circuit Opinion (*Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801 (Fed. Cir. 2021) (the "Opinion"));
d. Intel's Opening Brief on Remand (Paper 35);
e. Remand Declaration of Bill Lin, Ph.D. (Ex. 1026);
f. Lin Deposition Transcript (May 5, 2022) (Ex. 2010);
g. Oxford University Press, "A Dictionary of Computing" (6th ed.) (Ex. 2011);
h. "Computer Architecture—A Quantitative Approach (5th Edition)" by John L. Hennessy and David A. Patterson (Ex. 2012);
i. "Computer Architecture—A Quantitative Approach (4th Edition)" by John L. Hennessy and David A. Patterson (Ex. 2014);
j. "FIFO Architecture, Functions, and Applications" (Texas Instruments, 1999) (Ex. 2013); and
k. Any other materials referenced herein.

3. I am being compensated for my work in this matter at my standard hourly rate of $975 for consulting services. My compensation in no way depends on the outcome of this proceeding.

I. PROFESSIONAL BACKGROUND

4. I described my qualifications in my Declaration in support of Qualcomm's Patent Owner Response. Ex. 2007 at ¶4-17.

II. RELEVANT LEGAL STANDARDS

5. In my Declaration in support of Qualcomm's Patent Owner Response, I set forth the applicable principles of patent law that were provided to me by counsel. Ex. 2007 at ¶18-24. As appropriate, I have continued to apply those principles in providing my opinions in this Declaration.

III. BACKGROUND ON BUFFERS

6. Computer systems often need to transfer data (such as instructions that comprise software) between devices and/or components. A common problem that arises in this context is matching the timing at which the sender sends the data with the timing at which the receiver receives the data. A common solution to this problem is to insert a buffer between the sender and the receiver. In this context a buffer accumulates and stores transferred data, typically for a short period of time, until the receiver retrieves the data. For efficiency reasons, it is often important that the buffer support fast retrieval by the receiver. Oxford University Press's "A Dictionary of Computing," Sixth Edition (2008), defines "buffer" as follows:

buffer **1.** A temporary memory for data, normally used to accommodate the difference in the rate at which two devices can handle data during a transfer. The buffer may be built into a peripheral device, such as a printer or disk drive, or may be part of the system's main memory. *See* BUFFERING. **2.** A means of maintaining a short but varying length of magnetic tape between the reels and the *capstan and head area of a tape transport, in order that the acceleration of the tape at the reels need not be as great as that of the tape at the capstan. Streaming tape transports and many types of cartridge drives do not use buffers and are therefore limited to lower accelerations of the tape in the area of the head and (if there is one) capstan. **3.** Any circuit or device that is put between two others to smooth changes in rate or level or allow asynchronous operation. For example, line *drivers can be used to isolate (or buffer) two sets of data lines.

Ex. 2012 at 58.

7. Buffers that support the transfer of data are ubiquitous in computing generally and can appear in a wide variety of contexts, implemented in a wide variety of storage technologies, with the specific characteristics of the buffer specialized as appropriate for the context in which they appear.

8. There is an important conceptual difference between *buffers* that store data for short periods of time as it is transferred between components or devices, and *memories* that store data for longer periods of time (or even indefinitely) for future access, often as the primary storage mechanism for data over the lifetime of a

program or computer system. Examples of such memories include the main or system memory of the computer, often implemented in DRAM (storing data during the execution of a program), disks (storing data for a computer attached to the disk), or tape (storing archived data indefinitely).

Examples of Buffers in Modern Computer Systems

9. In modern computers, the DRAM memory access time is too slow to keep up with processor memory reads and writes. *See*, *e.g.*, Ex. 2012, "Computer Architecture—A Quantitative Approach (5th Edition)" by John L. Hennessy and David A. Patterson (hereinafter "Hennessy/Patterson 5") at Figure 2.2, page 73 and Ex. 2014, "Computer Architecture—A Quantitative Approach (4th Edition)" by John L. Hennessy and David A. Patterson (hereinafter "Hennessy/Patterson 4") at Figure 5.2, page 289. This fact motivates the development of caches – smaller, faster memories designed to hold accessed memory locations. *See* Hennessy/Patterson 5 at Figure 2.1, page 72 and Hennessy/Patterson 4 at Figure 5.1, page 288. Instead of inefficiently accessing data from DRAM memory, the processor accesses data from faster caches, with data transferred between the DRAM memory and caches as required to satisfy the processor's memory access requests. A goal is to improve the overall efficiency and performance of the system by storing frequently accessed data in the cache.

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