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(54) **Title**: MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

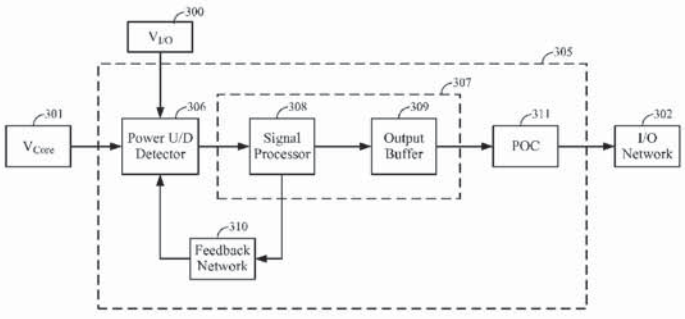

FIG. 3B

(57) **Abstract**: A multiple supply voltage device includes an input/output (I/O) network operative at a first supply voltage, a core network coupled to the I/O network and operative at a second supply voltage, and a power-on-control (POC) network coupled to the I/O network and the core network. The POC network is configured to transmit a POC signal to the I/O network and includes an adjustable current power up/down detector configured to detect a power state of the core network. The POC network also includes processing circuitry coupled to the adjustable current power up/down detector and configured to process the power state into the POC signal, and one or more feedback circuits. For reducing the leakage current while also improving the power-up/down detection speed, the feedback circuit(s) are coupled to the adjustable current power up/down detector and configured to

MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

TECHNICAL FIELD

[0001] The present disclosure is related, in general, to integrated circuit devices and, more particularly, to power up/down detectors for multiple supply voltages devices.

BACKGROUND

[0002] As technology has advanced there has been an increased ability to include more and more devices and components within integrated circuits. Semiconductor fabrication techniques have allowed these embedded devices to become smaller and have lower voltage requirements, while still operating at high-speeds. However, because these new integrated devices often interface with older technology devices or legacy products, input/output (I/O) circuits within the integrated circuit have remained at higher operating voltages to interface with the higher voltage requirements of these older systems. Therefore, many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.

[0003] Core devices and applications communicate with operations outside of the integrated component through the I/O devices. In order to facilitate communication between the core and I/O devices, level shifters are employed. Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down. Powering down or power collapsing is a common technique used to save power when no device operations are pending or in progress. For example, if the core network is power collapsed, it is possible that the level shifters, whether through stray currents or the like, could send a signal to the I/O devices for transmission. The I/O devices assume that the core devices have initiated this communication, and will, therefore, transmit the erroneous signal into the external environment.

[0004] It has been found useful to have the I/O devices in a known state when the core networks are powered down. In order to guarantee these known states,

solutions have included the addition of hardware or software for managing additional external signals to control the I/O circuitry. By using these external signals, the I/O circuitry can be controlled (e.g., placed in a known state) whenever the core power is collapsed. However, whether implementing this external signal management system using hardware or software, a considerable amount of delay is added to the operation of the integrated device. Although hardware is slightly faster than software controls, , hardware solutions may have problems caused by significant additional power leakage on the I/O device side.

[0005] One hardware solution currently in use provides power-up/down detectors to generate a power-on/off-control (POC) signal internally. The POC signal instructs the I/O devices when the core devices are shut down. FIGURE 1 is a circuit diagram illustrating standard POC system 10 for multiple supply voltage devices. POC system 10 is made up of three functional blocks: power-up/down detector 100, signal amplifier 101, and output stage 102. Power-up/down detector 100 has PMOS transistor M1 and NMOS transistors M2 – M3. The gate terminals for each of M1-M3 are connected to core power supply 103, V_{core}. When core power supply 103 is power collapsed, M2 and M3 are switched off while M1 is switched on, pulling up the input node to amplifier 105 to $V_{I/O}$, i.e., I/O power supply 104. A "high" signal is input into amplifier 105 which inverts the output to a "low" signal. In output stage 102, the low signal from amplifier 105 is processed in output buffer 106 and again inverted to a high signal for POC 107. The high signal for POC 107 is transmitted to the I/O circuitry indicating that core power supply 103 has been shut down.

[0006] When core power supply 103, V_{core}, is on, M1 becomes very weak and M2 and M3 both switch strongly on, pulling the input node to amplifier 105 to V_{SS}, i.e., core power supply 103. V_{SS} is considered the logical low signal. Therefore, amplifier 105 inverts it to a high signal which is then processed in output buffer 106 and inverted again to a low signal. This signal detection process operates acceptably when either I/O power supply 104 is on and core power supply 103 is power collapsed or when core power supply 103 is powered-up before I/O power supply 104 is powered-up. However, when I/O power supply 104 is powered-up before core power supply 103 powers-up, substantial current leakage may occur in the power up/down detector 100 or in the POC 10.

[0007] In the situation where I/O power supply 104 is on and core power supply 103 is off, M1 is switched on with M2 and M3 switched off. When core power supply 103 is then powered up, M2 and M3 switch on, and M1 becomes very weak. However, before M1 can switch completely off, there is a period in which all three transistors within power up/down detector 100 are on. Thus, a virtual short is created to ground causing a significant amount of current to flow from I/O power supply 104 to ground. This "glitch" current consumes unnecessary power.

[0008] In order to reduce this stray power consumption, one solution may be adopted to decrease the sizes of transistors M1-M3. By reducing the size of M1-M3, the actual amount of current that can pass through the transistors is physically limited. However, because the transistors are now smaller, their switching speeds are also reduced. The reduced switching speed translates into less sensitivity in detecting power-up/down of core supply voltage 103 or longer processing time for power-up/down events.

[0009] FIGURE 2 is an illustration of diagram 20 presenting the signal interactions in POC circuit 10 of FIGURE 1. Diagram 20 includes power supply diagram 21 and POC diagram 22. As I/O power supply 104 is powered up, there is a steady increase until it reaches $V_{I/O}$. POC 107 follows I/O power supply 104 as it powers up to reach the high level. Similarly, when I/O power supply 104 maintains steady at $V_{I/O}$ at time 200, POC 107 remains steady at the high signal. When core power supply 103 begins to power on at time 201 power up/down detector 100 (FIGURE 1) takes a little time to actually detect this new power level. Once detected, at time 202, POC 107 is switched to the low value. POC 107 should, thereafter, remain at the low level until core power supply 103 is power collapsed, between times 203 and 205. Again, because power up/down detector 100 (FIGURE 1) takes a little time to actually detect the new power level, POC 107 remains in the low state until time 204, when the powering down is actually detected by power up/down detector 100. This low state time, between time 202 and 204 is referred to as the normal operation region. Once core power supply 103 is completely off or power collapsed at time 205, the input to amplifier 105 (FIGURE 1) is again pulled up to the high signal. POC 107 will then follow I/O power supply 104 as it also powers down between times 206 and 207.

[0010] The leakage current between I/O power supply 104 and ground can be lessened because of the smaller transistor size. Thus, during the time between times 201 and 205 any leakage that occurs is reduced. However, this reduced leakage comes at the price of faster detection. If POC circuit 10 may include the lower-threshold or bigger transistors, switching/detecting times would be faster. For example, as core power supply 103 begins to power up at time 201, the lower-threshold or bigger transistors of power up/down detector 100 would detect the power-up at time 208, instead of time 202. Moreover when core power supply 103 begins powering down at time 203, the power up/down detector 100 would detect the power-down at time 209, instead of time 204. This increase may be represented by the difference between the time periods of time 202 to 204 vs. time 208 to 209. Therefore, the conventional solutions still have problems with leakage and switching times.

SUMMARY

[0011] Various representative embodiments of the disclosure relate to integrated devices having multiple supply voltages. Further representative embodiments of the present disclosure relate to methods for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device. Additional representative embodiments of the present disclosure relate to systems for reducing power consumption in a POC network of a multiple supply voltage device.

[0012] A multiple supply voltage device includes a core network operative at a first supply voltage and a control network coupled to the core network. The control network is configured to transmit a control signal. The control network includes an up/down (up/down) detector configured to detect a power state of the core network. The control network further includes processing circuitry coupled to the up/down detector and is configured to generate the control signal based on the power state. The control network further includes one or more feedback circuits coupled to the up/down detector. The one or more feedback circuits are configured to provide feedback signals to adjust a current capacity of said up/down detector.

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