Apple Inc. (Petitioner)
v.
Qualcomm Incorporated (Patent Owner)

Demonstratives
Trial Nos. IPR2018-01315 and -01316
U.S. Patent No. 8,063,674

Before Hon. Trevor M. Jefferson, Daniel J. Galligan, and Scott B. Howard, Administrative Patent Judges

Exhibit 1026
Apple v. Qualcomm
IPR2018-01316

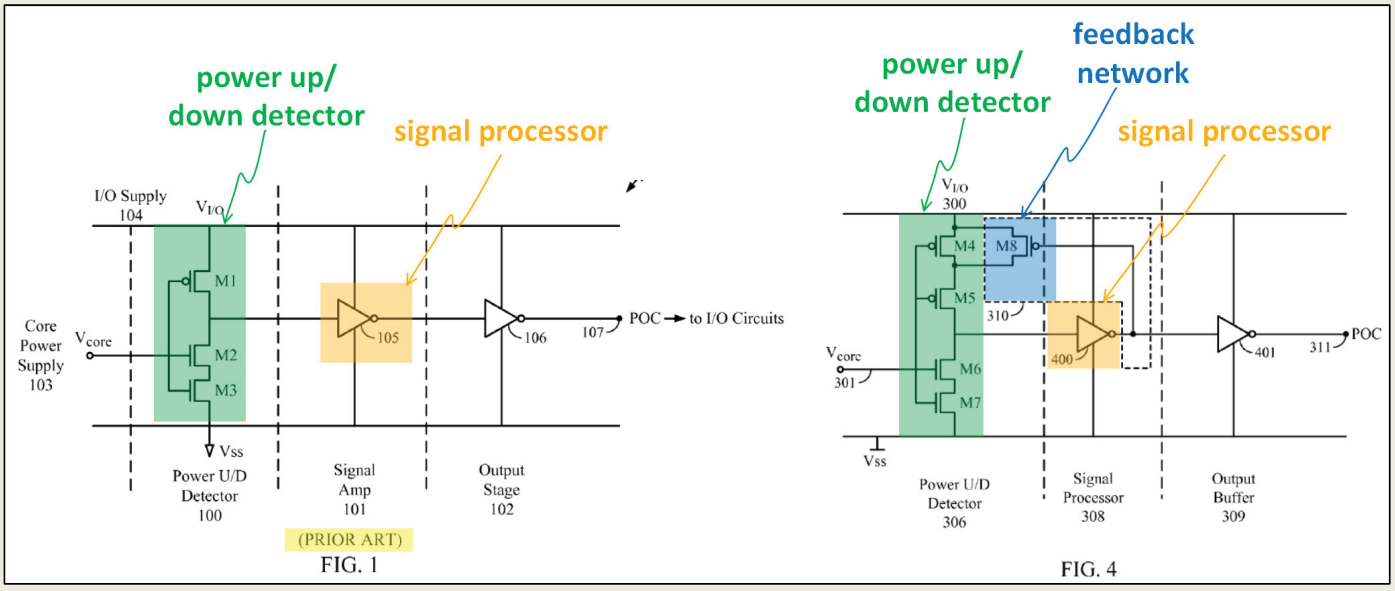
- **Background and Summary of Issues**

- Issue 1: AAPA + Majcherczak
  - Explicit and Art-Specific Motivation to Combine
  - No Teaching Away
  - AAPA Is Eligible

- Issue 2: Steinacker, Doyle, and Park
  - Explicit and Art-Specific Motivation to Combine
  - No Teaching Away

Alleged Innovation of the ’674 Patent

1:57-62. The main difference between this prior art POC system 10 and the purported invention of the ’674 Patent is the addition of a feedback network 310. APPLE-1003, ¶ 60. A comparison of FIG. 1 and FIG. 4 illuminates this straightforward difference. *Id.*



Excerpt from Paper 2 (Petition), pp. 5-6

Independent Claim 1 of the ’674 Patent

1. A multiple supply voltage device comprising:

a core network operative at a first supply voltage; and

a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;

one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;

at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

APPLE-1001, 8:44-9:3
(cited at Paper 7, pp. 6-7).

Figure 4 of the ’674 Patent

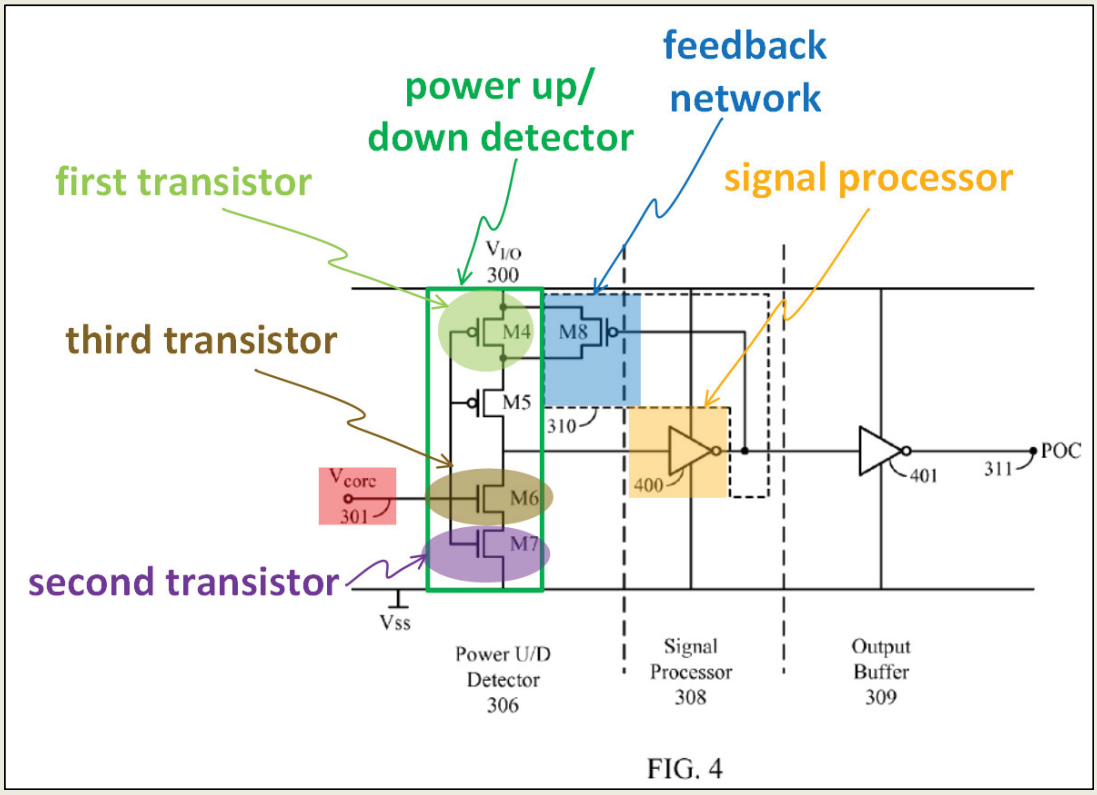


FIG. 4

See **Paper 2, pp. 6, 56.**

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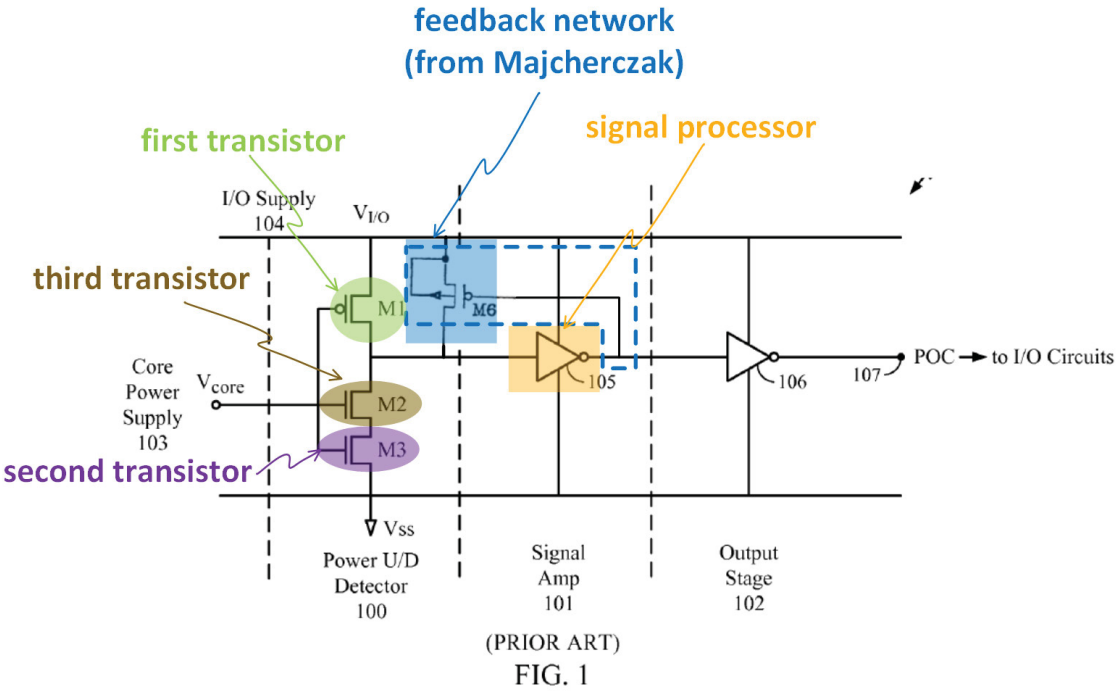
AAPA in view of Majcherczak



(PRIOR ART)

FIG. 1

AAPA + Majcherczak POC System

Paper 2, p. 56.

No Dispute AAPA + Majcherczak Meets Limitations of Claim 1

1. A multiple supply voltage device comprising:

✓ a core network operative at a first supply voltage; and

✓ a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing

✓ circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;

✓ one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

✓ at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;

✓ at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

✓ at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

APPLE-1001, 8:44-9:3
(cited at Paper 2, pp. 46-56; Paper 7, pp. 6-7).

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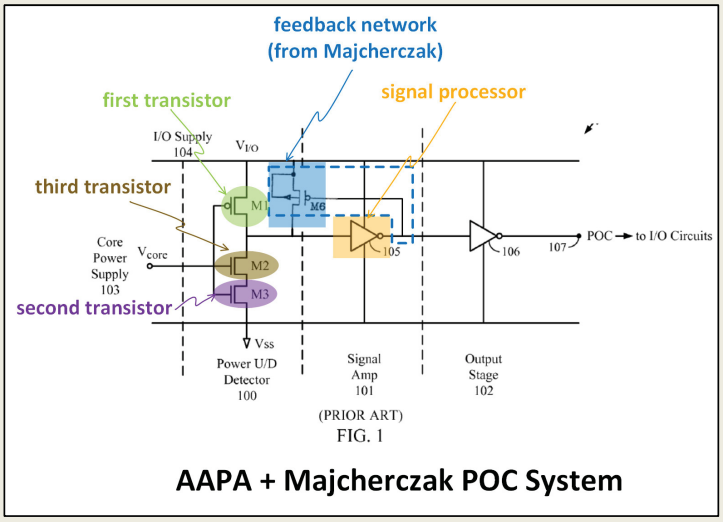
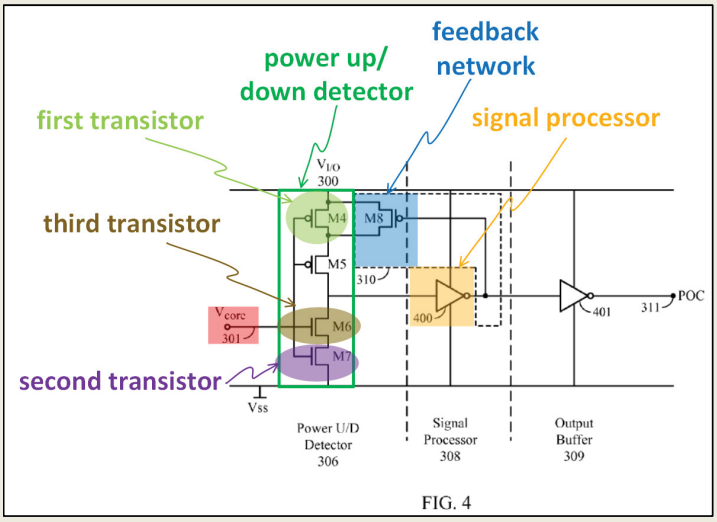
No Dispute AAPA + Majcherczak Meets Limitations of Claim 1



AAPA + Majcherczak POC System



AAPA + Majcherczak

'674 Patent's FIG. 4

Paper 2, pp. 6, 56.

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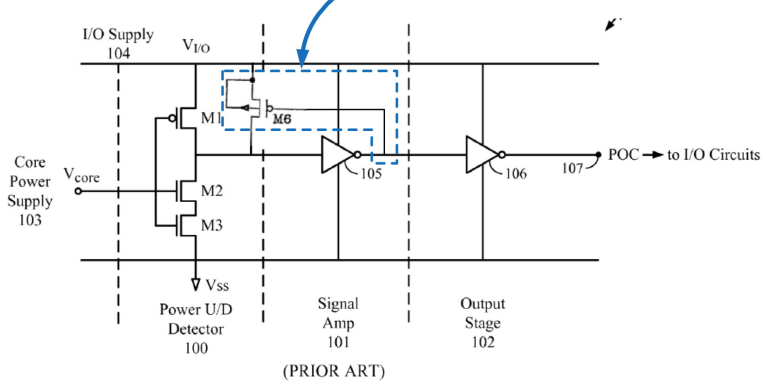
Motivation to Combine AAPA and Majcherczak

Integrate feedback transistor M6 to gain "proper stabilizing"
(gate connected to output of inverter, source connected to $V_{I/O}$, and drain connected to output of power up/down detector—just as in Majcherczak)



(PRIOR ART)
FIG. 1

AAPA POC System

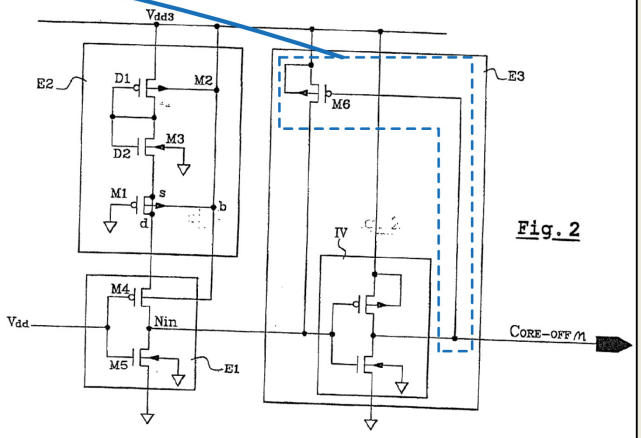


Fig. 2

Majcherczak Voltage Detector

Paper 2, p. 44.

Motivation to Combine AAPA and Majcherczak

One hardware solution currently in use provides power-up/down detectors to generate a power-on/off-control (POC) signal internally. The POC signal instructs the I/O devices when the core devices are shut down. FIG. **1** is a circuit diagram illustrating standard POC system **10** for multiple supply voltage devices. POC system **10** is made up of three

APPLE-1001 ('674 Patent), 1:57-60.
Cited at Paper 2, pp. 37, 43.

[0013] The invention therefore relates to a device for the detection of the level of the core supply voltage of an integrated circuit with respect to the level of an interface power supply voltage at a higher nominal level, applied as a power supply voltage to interface circuits of the integrated circuit. For the transmission of input/output signals, the

APPLE-1008 (Majcherczak), ¶ 0013.
Cited at Paper 16, p. 4.

AAPA and Majcherczak
In Exact Same Field

Motivation to Combine AAPA and Majcherczak

Majcherczak Teaches Explicit Motivation for Feedback in a Power Supply Voltage Detection Circuit

power supply voltage Vdd**3**. This pull-down transistor **M6** is typically a P-type MOS transistor, controlled at its gate by the inverse detection signal $C_{ORE-OFFn}$ given by the inverter IV of the output stage **E3**. This positive pull-down transistor **M6** enables the proper stabilizing of the detection device. It maintains the node Nin at Vdd**3**, by feedback.

[**0038**] With the output stage E**3**, a hysteresis detection is obtained with a low threshold of switching from a state of the presence of a core power supply to a state of the absence of a core power supply, and a high threshold of switching of the detection circuit from a state of absence of the core supply to a state of presence of the core supply. In particular,

Cited at Paper 2, p. 42; Paper 16, p. 4.

QC and Its Expert Agree with Advantages of Adding Feedback to AAPA

Q. Dr. Pedram, we've been talking about noise immunity.

If someone told you to solve a noise immunity problem by adding hysteresis to the prior art Figure 1 circuit in the '674 patent, in 2001, how would you have gone about adding hysteresis to that circuit?

A. So normally, to add hysteresis to a circuit, you have to make the circuit behave differently for different input transitions. Whether low-to-high or high-to-low, you have to behave differently. And then one could potentially use feedback to create that kind of different response to different transitions that you have.

APPLE-1017, 46:20-47:8 (cited at Paper 16, p. 5).

stability of its detection device. *See, e.g.*, Ex. 1008 at ¶37. Facing Majcherczak's problem of adding stability, *i.e.*, avoiding false detection such as by adding a noise margin, the intuitive solution would be to add hysteresis, and that is what Majcherczak describes. But the POSA faced with the switching speed problem of

QC's Sur-Reply (Paper 19), p. 5.

Hysteresis Had Known Benefits to a POSITA

To demonstrate the usefulness of hysteresis, Figure 3-48(a) shows an input signal with long rise and fall times and about 0.5 V of noise on it. An ordinary inverter, without hysteresis, has the same switching threshold for both positive-going and negative-going transitions, $V_T \approx 2.5$ V. Thus, the ordinary inverter responds to the noise as shown in (b), producing multiple output changes each time the noisy input voltage crosses the switching threshold. However, as shown in (c), a Schmitt-trigger inverter does not respond to the noise, because its hysteresis is greater than the noise amplitude.

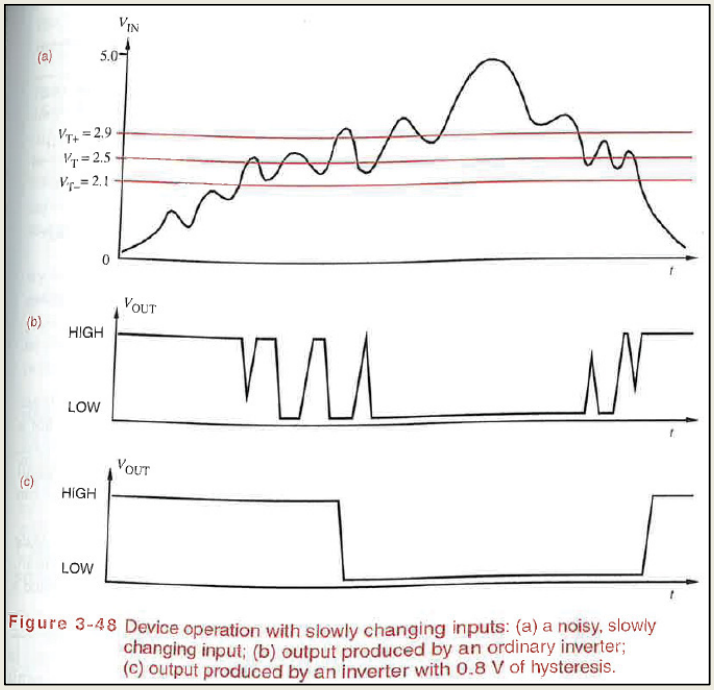


Figure 3-48 Device operation with slowly changing inputs: (a) a noisy, slowly changing input; (b) output produced by an ordinary inverter; (c) output produced by an inverter with 0.8 V of hysteresis.

APPLE-1024, pp. 87-88
(cited at Paper 16, p. 4).

POSITA Presumed to Know All Relevant Prior Art

In re GPAC Inc., 57 F. 3d 1573, 1579 (Fed. Cir. 1995).

"The person of ordinary skill in the art is a hypothetical person who is presumed to know the relevant prior art."

Cited at Paper 16, p. 22, n. 4.

Advantage of Adding Hysteresis Need Not Be Among Advantages Sought by '674 Patent

Manual of Patent Examining Procedure (MPEP) § 2144(IV)

"The reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. *See, e.g.*, *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (motivation question arises in the context of the general problem confronting the inventor rather than the specific problem solved by the invention); *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1323, 76 USPQ2d 1662, 1685 (Fed. Cir. 2005) ("One of ordinary skill in the art need not see the identical problem addressed in a prior art reference to be motivated to apply its teachings.") . . . "

Cited at Paper 16, p. 6.

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QC Advances Three Alleged Disadvantages of Combination

1. The Addition of Majcherczak's Transistor M6 to the AAPA Results in Increased Leakage Current, and the POSA Would Therefore Not Make This Combination

2. The Proposed Combination of the AAPA and Majcherczak Also Results in Increased Leakage Current Compared to Majcherczak.

3. The Combination of AAPA and Majcherczak Proposed by Petitioner Would Result in a DC Fighting Condition and Increased Glitch Current During Turn-On Transitions.

Paper 12, pp. 21, 25, 27.

QC's Expert Testified That Mitigation of Disadvantages Within Skill of POSITA

Q. Dr. Pedram, if you handed one of your graduate students prior art Figure 1 from the '674 patent and asked them to propose a method of reducing power consumption by any amount, so a small amount or a large amount, would your student have been able to, in February of 2009, propose ways of reducing power consumption?

Adjusting Transistor Size & Threshold Voltage (VT) Mitigates Leakage

If I told them the technology in which the transistors are implemented in 2009, maybe it's a 65-nanometer CMOS technology, so you have the IV characteristics of these transistors at different operating voltages and so on. And now take this design, make sure you can reduce the leakage. But at the same time, your detection speed should not exceed, say, a nanosecond. I'm just making up numbers. So within one nanosecond, make sure you can detect it. But then subject to that constraint, minimize the leakage through this.

And the student would say what optimization knobs do I have? I'd say you can size it and you can do VT adjustment. He would say, can I also change the VIO value? No. Can I change the V-core value? No. Can I change the slope of the V-core as I wanted to? No, the slope of the incision is whatever it is.

APPLE-1017, 63:22-65:20 (cited at Paper 16, p. 10).

QC's Expert Testified That Mitigation of Disadvantages Within Skill of POSITA

Selecting Transistor Sizes Within Skill of POSITA

> Okay. So subject to these things, go ahead and optimize. He would go and probably do some splice simulations, maybe do an exhaustive enumeration of the different transistor sizes that you see in M1, M2, M3 there. Try hundred different values for M1, ten different values for M2, ten different values for M3, see what the performance characteristics are in terms of the leakage.
>
> Any solution that would have violated the performance constraint, the detection latency without being thrown out, everything that meets it, was admissible among those, pick the best one, come back and give it to me, yeah, he could have done that.

APPLE-1017, 65:7-20
(cited at Paper 16, p. 10).

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Apple's Expert Agrees That Mitigation of Disadvantages Within Skill of POSITA

Adjusting Transistor Size & Threshold Voltage (VT) Mitigates Leakage

V. Summary

74. In running the SPICE simulations in this report, it was clear that the setting of the MOSFET thresholds is key to making the circuits function as intended. The FET thresholds determine the input level where POC (power on control) signal is asserted and the levels also affect the leakage once that input level is reached. A key difference in the AAPA circuit and the circuits with feedback is in the setting of the thresholds for the P channel FETs. In all circuits,

76. Circuits with feedback, including the '674 Figure 4 circuit and prior art combinations, do not have the same problem because the gate of the feedback transistor is driven all the way to the high (5 V) rail by the inverter, and that completely turns off the P-channel feedback FET. The other P-channel FETs can have thresholds far below the maximum input voltage to keep them off as well. With a -2.3V threshold and the input at 3.3V, the P-channel FET(s) do not start conducting until the input voltage drops below 5-2.3=2.7V, keeping the P channel strongly off during normal operation when the input voltage is a 3V or higher. Glitch current is reduced to a very low value by setting this threshold near the inverter threshold where the feedback transistor turns off. Thus, with proper thresholds, none of these circuits have high glitch current or high leakage.

APPLE-1018, ¶¶ 74, 76 (cited at Paper 16, p. 9).

Apple's Expert Agrees That Mitigation of Disadvantages Within Skill of POSITA

Selecting Transistor Sizes Within Skill of POSITA

41. The '674 Patent does not specify V_{th} or R_{on} for the transistors in the circuits in the drawings and specification. The fact that the '674 Patent does not give guidance in the selection of these key parameters indicates that a POSITA should be assumed to have sufficient skill in circuit design to understand and modify circuits in a way that a POSITA would be able to select the appropriate parameters, or to construct stacks of transistors to obtain the desired and useful power detection functionality described in the '674 Patent.

APPLE-1003, ¶ 41
(cited at Paper 16, p. 10).

Mitigation of Alleged Disadvantages Was Within Skill of POSITA

1. The Addition of Majcherczak's Transistor M6 to the AAPA Results in Increased Leakage Current, and the POSA Would Therefore Not Make This Combination

2. The Proposed Combination of the AAPA and Majcherczak Also Results in Increased Leakage Current Compared to Majcherczak.

3. The Combination of AAPA and Majcherczak Proposed by Petitioner Would Result in a DC Fighting Condition and Increased Glitch Current During Turn-On Transitions.

See Paper 16, p. 12.

QC's Expert Testified That Mitigation of Disadvantages Within Skill of POSITA

Adjusting Transistor Size & Threshold Voltage (VT) Mitigates "Rare" DC Fighting Condition

Q. You haven't calculated how frequently or under what conditions you believe the AAPA Majcherczak combination would result in this failure that you described?

A. It's a situation that could easily arise if you don't do the right sizing and the right facial voltage assignment. But -- of transistors -- various transistor. Not just one transistor. All of the transistors you see this design, and that's why it's a complicated task.

But it's a situation on rare occasions could happen. And -- and rare at the speeds that

APPLE-1017, 181:10-21
(cited at Paper 16, p. 11).

Apple's Expert Agrees That Mitigation of Disadvantages Within Skill of POSITA

Adjusting Transistor Size & Threshold Voltage (VT) Mitigates Glitch

V. Summary

74. In running the SPICE simulations in this report, it was clear that the setting of the MOSFET thresholds is key to making the circuits function as intended. The FET thresholds determine the input level where POC (power on control) signal is asserted and the levels also affect the leakage once that input level is reached. A key difference in the AAPA circuit and the circuits with feedback is in the setting of the thresholds for the P channel FETs. In all circuits,

76. Circuits with feedback, including the '674 Figure 4 circuit and prior art combinations, do not have the same problem because the gate of the feedback transistor is driven all the way to the high (5 V) rail by the inverter, and that completely turns off the P-channel feedback FET. The other P-channel FETs can have thresholds far below the maximum input voltage to keep them off as well. With a -2.3V threshold and the input at 3.3V, the P-channel FET(s) do not start conducting until the input voltage drops below 5-2.3=2.7V, keeping the P channel strongly off during normal operation when the input voltage is a 3V or higher. Glitch current is reduced to a very low value by setting this threshold near the inverter threshold where the feedback transistor turns off. Thus, with proper thresholds, none of these circuits have high glitch current or high leakage.

APPLE-1018, ¶¶ 74, 76 (cited at Paper 16, p. 9).

Mitigation of Alleged Disadvantages Was Within Skill of POSITA

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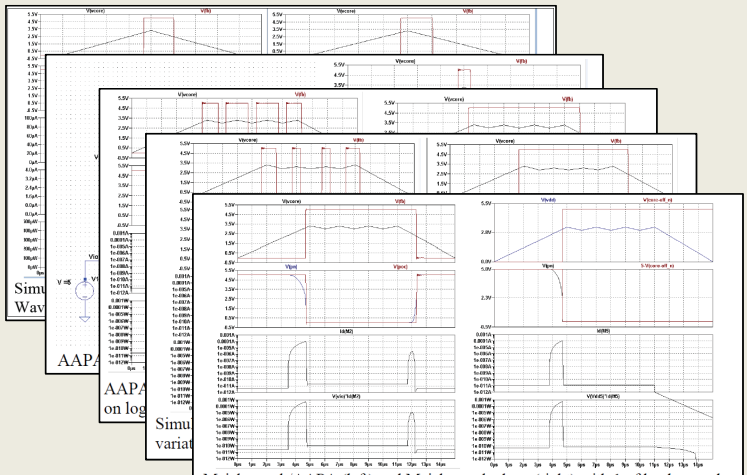
3. The Combination of AAPA and Majcherczak Proposed by Petitioner Would Result in a DC Fighting Condition and Increased Glitch Current During Turn-On Transitions.

See Paper 16, p. 12.

Dr. Horst Confirmed Through SPICE Simulations that the Alleged "Disadvantages" Did Not Exist



Majcherczak/AAPA (left) and Majcherczak alone (right) with 1 pf load on node PN. With Majcherczak alone, the loss of input power is not detected.

29. The simulations show results that are almost identical. There are small differences in the stack and feedback currents, but the magnitude of these differences is small, and the resulting power graphs are nearly indistinguishable. *See* Ex. 1017, 162:6-163:2 (Dr. Pedram agreeing that small differences in milliwatt microwatt range make the results in FIG. 17(b) of Park no better or worse than one another).

64. Based on these results, it is clear to see that when the input voltage only slightly exceeds the threshold and is subject to normal variations due to load and noise, the AAPA/Majcherczak combination would have resulted in significant decreases in power consumption over the AAPA. This is motivation to choose the AAPA/Majcherczak combination.

71. These simulation results indicate that Majcherczak alone functions in a quite similar manner to the AAPA/Majcherczak combination. Both have hysteresis and nearly identical switching current as the input voltage rises. Both have extremely low leakage during normal operation. The AAPA/Majcherczak combination has a small current pulse when the input voltage is falling, but Majcherczak alone draws almost no current when the input voltage is falling. This might look like a benefit, but in fact it means that the circuit does not actively pull down the PN node when the input is falling. Simulation showed that a tiny

APPLE-1018, ¶¶ 29, 64, 71
(cited at Paper 16, pp. 9-12).

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Motivation Exists on Balance

Medichem, S.A. v. Rolabo, S.L., 437 F.3d 1157, 1165 (Fed. Cir. 2006).

"[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine. *See Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n. 8 (Fed. Cir. 2000) ("The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another.")."

Cited at Paper 16, p 8.

QC Cites No Corroborating Evidence Beyond Unsupported Expert Opinion

Ericsson Inc. v. Intellectual Ventures I LLC, 890 F. 3d 1336, 1346 (Fed. Cir. 2018).

"To contradict a reference, an unsupported opinion is not substantial evidence."

TABLE OF EXHIBITS

Exhibit	Description
2001	International (PCT) Application Publication No. WO 2010/091105
2002	Declaration of Dr. Massoud Pedram
2003	Transcript of the Deposition of Dr. Robert Horst
2004	Patent Owner's Request for Rehearing in IPR2017-00126.
2005	Patent Owner's Response in IPR2017-00126
2006	Transcript of Second Deposition of Dr. Robert Horst
2007	Exhibit 1 to Second Deposition of Dr. Robert Horst (Corrective Declaration)

QC Cites No Corroborating Evidence Beyond Expert

EXHIBITS

APPLE-1001	U.S. Patent No. 8,063,674 to Kwon *et al.* ("the '674 patent")
APPLE-1002	Excerpts from the Prosecution History of the '674 Patent ("the Prosecution History")
APPLE-1003	Declarati
APPLE-1004	Curriculu
APPLE-1005	U.S. Pate
APPLE-1006	U.S. Pate
APPLE-1007	Jun Cheo *Reductior* Integratio
APPLE-1008	U.S. Pat. ("Majche
APPLE-1009	U.S. Pate
APPLE-1010	G.-W. Ch Its Role i Internatio Technolo
APPLE-1011	Wang-Ch Handsets Circuit S
APPLE-1012	Kaushik reduction 91 Proce
APPLE-1013	Yangyang Ye *et al.*, "A new technique for standby leakage reduction in high-performance circuits," 1998 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No.98CH36215), Honolulu, HI, USA, 1998, pp. 40-41
APPLE-1014	U.S.
APPLE-1015	Qade Research Circuit for Submicron Voltage Systems," 2006 IEEE International Symposium on Circuits and Systems (Sep. 2006)
APPLE-1016	Declaration of Jacob Munford (with attachments)
APPLE-1017	Transcript of Deposition of Dr. Massoud Pedram
APPLE-1018	Supplemental Declaration of Dr. Robert Horst
APPLE-1019	U. Daya Perera, *Reliability of Mobile Phones*, 1995 IEEE Proceedings Annual Reliability and Maintainability Symposium (Jan. 1995)
APPLE-1020	*One World Technologies, Inc. v. The Chamberlain Group, Inc.*, IPR2017-00126, Paper 56 (Final Written Decision) (PTAB Oct. 24, 2018)
APPLE-1021	*One World Technologies, Inc. v. The Chamberlain Group, Inc.*, IPR2017-00126, Paper 67 (Denial of Rehearing Request), 14-21 (PTAB Apr. 4, 2019)
APPLE-1022	U.S. Patent No. 5,386,153 to Peer H. Voss et al. ("Voss")
APPLE-1023	Wikipedia Entry for "LTspice" available at https://en.wikipedia.org/wiki/LTspice (accessed on July 17, 2019)
APPLE-1024	John F. Wakerly, DIGITAL DESIGN PRINCIPLES AND PRACTICES (4th Ed.) (2006)
APPLE-1025	Bruce Jacob, *ENEE 359a Digital VLSI Design - Transistor Sizing & Logical Effort*, available at https://ece.umd.edu/courses/enee359a.S2007/ (Internet Archive cached version of this address demonstrating presentation was available at least as early as July 4, 2008)

Apple Cites Extensive Corroborating Evidence

Paper 16, p 8; *compare* Paper 19, p. 33 *to* Paper 16, pp. ii-iv.

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AAPA Is Eligible Prior Art

"(a) IN GENERAL.—Any person at any time may cite to the Office in writing—(1) ***prior art consisting of patents or printed publications*** which that person believes to have a bearing on the patentability of any claim of a particular patent;"

35 U.S.C. § 301 (1980) (emphasis added)

"(b) Scope.—A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of ***prior art consisting of patents or printed publications***."

35 U.S.C. § 311(b) (emphasis added)

Cited at Paper 16, pp 1-2.

AAPA Is Eligible Prior Art

One World Technologies, Inc. v. The Chamberlain Group, Inc., IPR2017-00126, Paper 56, 38 (PTAB Oct. 24, 2018).

"Significantly, despite this restriction on the prior art that could be cited in pre-AIA reexamination proceedings, the Federal Circuit nonetheless found that AAPA could be cited and relied upon to support the Board's findings in such proceedings. *See In re NTP, Inc.*, 654 F.3d 1279, 1304 (Fed. Cir. 2011) ("We agree with the PTO that substantial evidence supports the Board's finding. Specifically, the AAPA states that . . . ," and this evidence supports "the Board's conclusion that . . . .")."

Cited at Paper 16, pp. 1-2.

AAPA Is Eligible Prior Art

In re Nomiya, 509 F.2d 566, 570–71 (CCPA 1975) (emphasis added).

"We see no reason why [the patentee's] representations in their [specification] should not be accepted at face value as admissions that . . . may be considered 'prior art' for any purpose, including ***use as evidence of obviousness*** under § 103."

"[A] statement by an applicant, whether in the application or in other papers submitted during prosecution, that certain matter is 'prior art' to him, is an admission that that matter is prior art for all purposes, whether or not a basis in § 102 can be found for its use as prior art."

APPLE-1020, p. 37 (cited at Paper 16, p. 1).

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  - Explicit and Art-Specific Motivation to Combine
  - No Teaching Away
  - AAPA Is Eligible
- **Issue 2: Steinacker, Doyle, and Park**
  - Explicit and Art-Specific Motivation to Combine
  - No Teaching Away

Steinacker in view of Doyle and Park

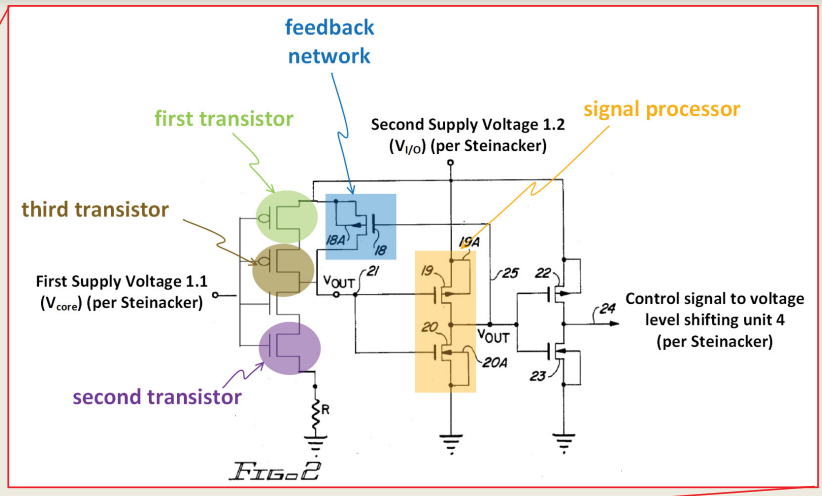
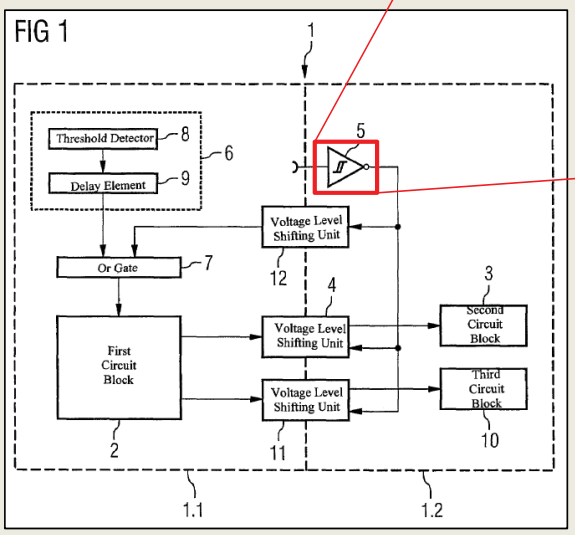


FIG 2



Paper 2, pp.12-13, 17, 33.

No Dispute Steinacker + Doyle + Park Meets Limitations of Claim 1

1. A multiple supply voltage device comprising:

✓ a core network operative at a first supply voltage; and

✓ a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing

✓ circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;

✓ one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

✓ at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;

✓ at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

✓ at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

APPLE-1001, 8:44-9:3
(cited at Paper 2, pp. 22-33; Paper 7, pp. 6-7).

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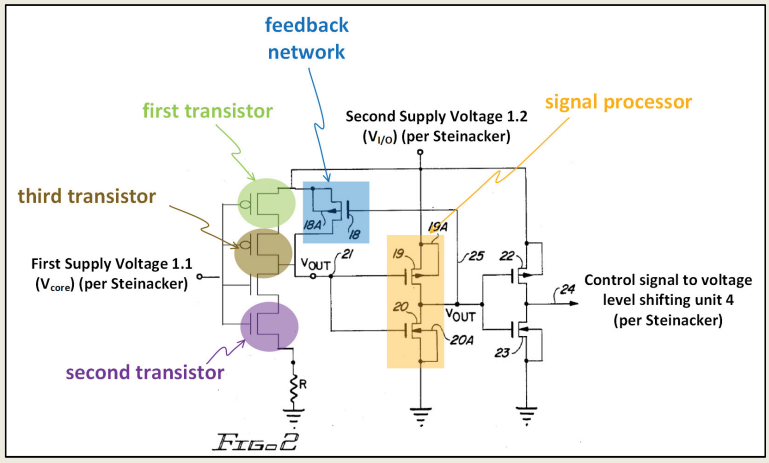
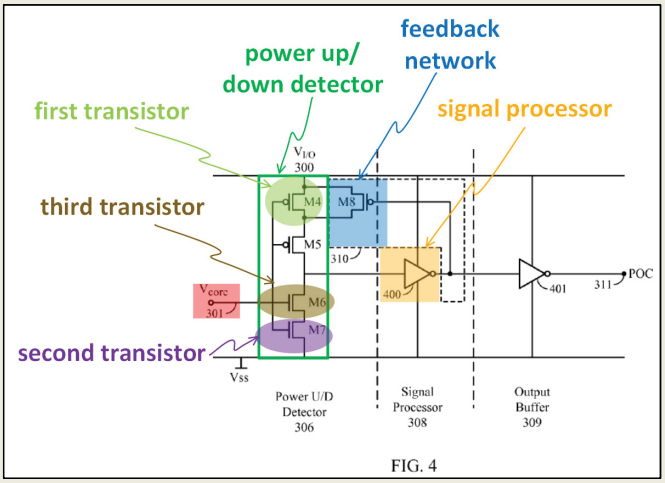
No Dispute Steinacker + Doyle + Park Meets Limitations of Claim 1



Steinacker + Doyle + Park



'674 Patent's FIG. 4

Paper 2, pp. 6, 56.

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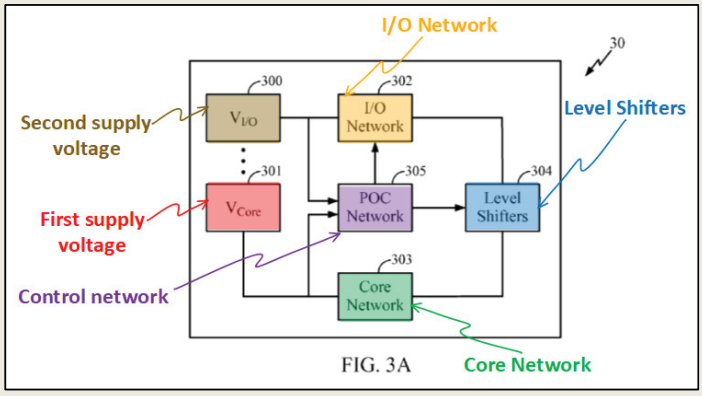
  - No Teaching Away

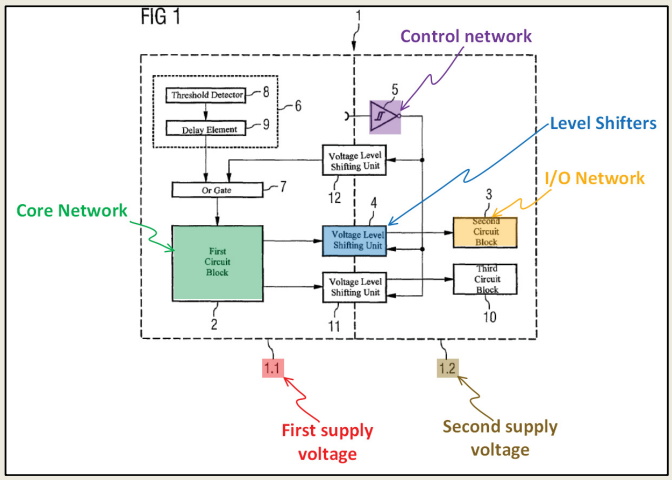
Board Requested Further Clarification

> achieve the claimed invention. However, we request the parties to brief this issue further during the trial, and in particular to focus on the following issues: (1) whether impermissible hindsight was used in the selection and combination of the prior art, (2) whether the reasons given in the Petition are generic statements divorced from the prior art elements or focus on the specific references used, and (3) whether a person of ordinary skill in the art would have selected the forced stack technique over the sleepy stack technique.

Paper 7 (Institution Decision), p. 40.

’674 Patent and Steinacker Are Analogous Art

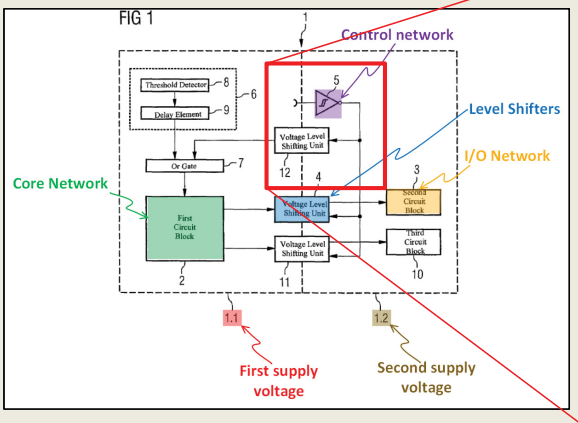


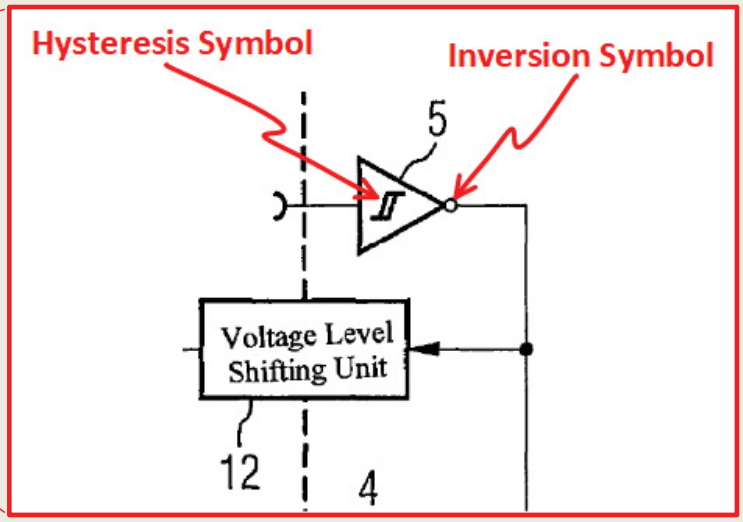


As described in the Petition, Steinacker and the ’674 Patent both address systems having at least two circuit blocks operating at different supply voltages, and both describe using a power detection circuit to ensure reliable operation when the different supply voltages are turned on and off independently of one another. *Compare* APPLE-1005, 1:49-52, 2:14-43, 4:45-64 *to* APPLE-1001, 1:12-54, 1:55-58; *see also* Pet., 11-12.

Paper 16, pp. 14-15.

Explicit Motivation to Combine Steinacker and Doyle





supplied to it via a first input. In the illustration, the voltage level detector **5** is in the form of a Schmitt trigger with an inverting output. However, it is likewise conceivable for the voltage level detector **5** to be in the form of an inverter circuit, a comparator circuit or comparable circuits. The inverting output of the voltage level detector **5** is coupled to the voltage level shifting unit **4**.

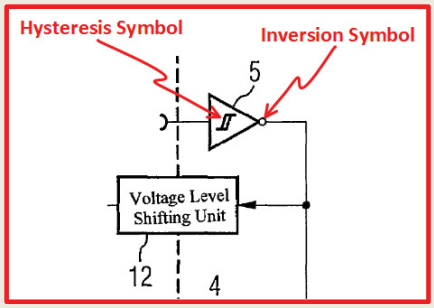
APPLE-1005 (Steinacker), 4:49-55.

Paper 16, pp. 16-17.

Explicit Motivation to Combine Steinacker and Doyle

QC's Expert Agrees That Steinacker's FIG. 1 Teaches POSITA to Use Inverter with Hysteresis

Q. Do you see there is a component labelled 5 in the shape of a triangle?
A. Yes.
Q. Do you see there is some sort of graph inside that component?
A. Yes.
Q. What does that graph depict to a person of skill in the art in the 2009 time period?
A. Typically, that kind of notation would imply the different switching thresholds on the rising and on the following transition, at the output of the circuit itself.
So a circuit component that shows hysteresis with respect to the rising trip point and the falling trip points.



A. Yeah. But, I mean, it's not describing what -- so Figure 1 of the Steinacker just shows a triangle with a bullet at the end that shows it's inverting.
And this particular notation which I describe to you to indicate there's hysteresis between the falling and rising trip point of this inverter. It doesn't have any disclosures about what is inside of that.

APPLE-1017 (Dr. Pedram Depo. Trans.), 135:10-136:2, 139:6-14 (cited at Paper 16, p. 17).

Explicit Motivation to Combine Steinacker and Doyle

> 40. A POSITA seeking an inverter circuit with hysteresis for use as a voltage level detector in a multiple supply voltage system would naturally have considered Doyle's inverter circuit, which satisfies each of these requirements.

APPLE-1018 (Dr. Horst Supp. Decl.), ¶ 40.

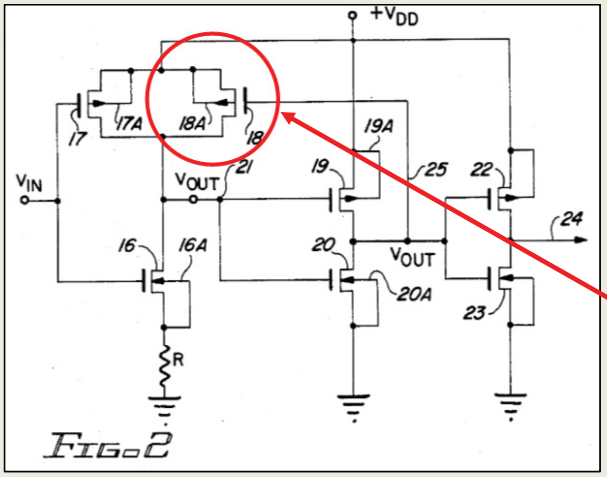


FIG. 2

APPLE-1006 (Doyle), FIG. 2.

> threshold voltage of the MOSFET. In the described embodiment of the invention, the self-compensating MOS circuit is contained in a CMOS inverting circuit as an inverter pull-down MOSFET having its drain electrode connected to the drain electrode of a P-channel pull-up MOSFET, the gates of both the pull-up MOSFET and the pull-down MOSFET being connected to an input conductor to which a TTL logic signal is applied. A second P-channel pullup MOSFET is provided in parallel with the first, and has its gate coupled to a feedback signal produced by a second CMOS inverting stage in order to provide a "polarized" hysteresis characteristic of the MOS level shifting circuit, making the trip point or switching point of the MOS level shifting circuit relatively independent of the power supply voltage applied across the CMOS level shifting circuit. The

APPLE-1006 (Doyle), 2:67-3:14.

Cited at Paper 16, p. 18.

Explicit Motivation to Combine Steinacker and Doyle

circuit block. The first circuit block receives the reset signal only when, during a turn-on operation for the circuit arrangement, the first supply voltage is sufficiently high to ensure reliable operation of the first circuit block. Delaying the reset signal is advantageous particularly for slow turn-on profiles.

APPLE-1005 (Steinacker), 3:9-14.

applicable to the role of the voltage level detector 5 in Steinacker. In particular, I noted that hysteresis is especially desirable for detection of power voltages because these voltages change slowly, and the processor should remain reset until the input voltage is reliably above the higher threshold. Ex. 1003, ¶ 51. In fact, Steinacker specifically notes that it sought for its circuit to operate effectively even where the power supplies exhibit "slow turn-on profiles." Ex. 1005, 3:12-14. Doyle similarly assumed and optimized his circuit for power supplies with slow turn-on profiles. *See* Ex. 1006, 6:28-41. It was well known that signals with slow turn-on profiles were more prone to being affected by noise. APPLE-1024, 87-89. Thus, a POSITA would have had additional motivation to select Doyle's improved inverter when implementing Steinacker's voltage detector 5, because Doyle described its improved inverter as providing "relatively high noise immunity." *See* Ex. 1006, 2:14-26.

APPLE-1018 (Dr. Horst Supp. Decl.), ¶ 41.

The transfer characteristics shown in FIGS. 3A and 3B show the V_{in} and V_{out} voltages of input level shifting circuit **15**, assuming that V_{DD} is +15 volts and also assuming that the slopes of the input signal V_{in} are such that delay between V_{in} and V_{out} is negligible. The curves of FIG. 3A show V_{in} and V_{out} when V_{in} is reduced slowly from +15 volts to 0 volts. V_{in} decreases slowly, as indicated by segment **6A**, until a first trip point **8** is reached, at which time V_{out} increases sharply (with respect to time) from 0 volts to +15 volts, as indicated by segment **7A** of V_{out} waveform **7**. The MOSFET device geometries are selected so that the trip point voltage, designated by dotted line **41**, has a nominal value of 1.5 volts.

APPLE-1006 (Doyle), 6:28-41.

Steinacker Concerned with Slow Turn-On Profiles and Doyle Optimized For That

Cited at Paper 16, p. 19-20.

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Explicit Motivation to Combine Steinacker and Doyle

In communications technology, particularly in mobile radio technology, a circuit arrangement frequently has two circuit blocks which operate at two different supply voltages.

current after the first circuit block is started up. This is advantageous particularly for circuit arrangements with limited current resources, such as in the case of mobile electronic appliances.

APPLE-1005 (Steinacker), 1:18-20, 3:19-22.

2.1 *Reliability and Environmental Issues*

The reliability requirements of mobile phones are challenging when compared to many commercial products. This requirement is primarily due to the need to satisfy vastly varying environmental conditions. This is due to fact that a mobile phone can be used in; indoor, outdoor and in a motor vehicle. The indoor and outdoor environmental conditions can vary significant from one country or continent to another. Also the environmental conditions within a vehicle can significantly vary in different countries. These can be temperature and or humidity extremes and dusty conditions. Typical environmental conditions in which a mobile phone needs to operate are:

Temperature range -30 to +60 deg C

APPLE-1019, 2.

It is another object of the invention to provide a CMOS inverter circuit having a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters.

In accordance with the present invention, the circuit consisting of N channel MOSFET 16 with both its source and bulk terminals connected to resistor R, functions as a "self-compensating" MOSFET, wherein the resistance of resistor R can be selected to cause trip points 8 and 8A (FIGS. 3A and 3B, respectively), to be very independent of temperature and certain processing parameter variations. In order to understand the opera-

APPLE-1006 (Doyle), 2:37-40, 7:17-24.

Steinacker Intended for Use In Mobile Devices, Where Temperature Independence Provided by Doyle Known to Be Beneficial

Cited at Paper 2, p. 21, Paper 16, p. 20.

Motivation to Combine with Park

current after the first circuit block is started up. This is advantageous particularly for circuit arrangements with limited current resources, such as in the case of mobile electronic appliances.

one another by the first circuit block. This development is therefore found to be particularly advantageous in a circuit arrangement with a limited resource for the second supply voltage, for example a battery or a storage battery.

APPLE-1005 (Steinacker), 3:19-22, 3:48-54.

I. INTRODUCTION

POWER consumption is one of the top concerns of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay, and area, and thus, designers are required to choose appropriate techniques that satisfy application and product needs.

Another technique to reduce leakage power is transistor stacking. Transistor stacking exploits the stack effect; the stack effect results in substantial subthreshold leakage current reduction when two or more stacked transistors are turned off together. Narendra *et al.* study the effectiveness of the stack effect including effects from increasing the channel length [6].

APPLE-1007 (Park), pp. 1-2.

Steinacker Intended for Use In Applications with Limited Resources and Park Provides Methods for Reducing Power

Cited at Paper 2, pp. 21-22, Paper 16, pp. 21-23.

Motivation Specific To Context of Steinacker

1. Whether impermissible hindsight was used in the selection and combination of the prior art

   No.

2. Whether the reasons given in the Petition are generic statements divorced from the prior art elements or focus on the specific references used

   No.

Paper 7, p. 40; Paper 16, pp. 13-14, 20.

Motivation to Combine with Park

Q. Is it fair to say that to implement the sleep stack technique of Park, it's necessary to have a sleep signal?

A. Not that -- I mean, the name is irrelevant. Right? I mean, you can call it anything you want. You could call it active or inactive or sleep or control signal X, Y, Z. The name has no significance here.

But -- but the fact is, to achieve the sleepy stack results to -- to implement the sleepy stack technique, you have to have a control signal that comes in and indicates that you are in the sleep mode or in the active mode of operation.

APPLE-1017 (Dr. Pedram Depo. Trans.), 149:24-150:11

Q. Did you see any discussion in Doyle of any kind of sleep signal?

A. Not that I recall.

APPLE-1017 (Dr. Pedram Depo. Trans.), 133:22-24

Q. Do you recall a discussion of any sleep signal in the Steinacker reference?

A. I don't recall that. I know there's a lot of discussion about voltage levels of the first block and the second block, but I don't recall a specific reference to sleep. Maybe there is some, but I don't recall.

APPLE-1017 (Dr. Pedram Depo. Trans.), 136:3-9

Sleep Signal Required By Sleepy Stack Technique Not Present in Steinacker or Doyle

Cited at Paper 16, p. 23.

Motivation to Combine with Park

1(a). On the other hand, the sleepy stack technique includes six transistors, two of which are driven by sleep signals S and S'. *See* APPLE-1007, 2, FIG. 2. I agree with Dr. Pedram that, "to implement the sleepy stack technique, you have to have a control signal that comes in and indicates that you are in the sleep mode or in the active mode of operation." APPLE-1017, 149:24-150:11. I also agree with Dr. Pedram that neither Steinacker nor Doyle disclose a sleep signal as required to implement Park's sleepy stack. *See* APPLE-1017, 133:22-24, 136:3-9. Thus, in the context of Steinacker and Doyle, a POSITA would have preferred the forced stack technique described by Park, as it would not have required the complication of the adding sleep signals S and S' to either of the Steinacker or Doyle systems.

APPLE-1018 (Dr. Horst Supp. Decl.), ¶ 47.

Sleep Signal Required By Sleepy Stack Technique Not Present in Steinacker or Doyle

Cited at Paper 16, p. 23.

Motivation to Combine with Park

48. Park noted that, when selecting between "different ideas" for "solv[ing] the power dissipation problem," "there is no universal way to avoid tradeoffs between power, delay, and area, and thus, designers are required to choose appropriate techniques that satisfy application and product needs." Ex. 1007, 1. Even the Park reference noted there are tradeoffs with regard to its preferred design (e.g., "delay and area overheads") and that it was most appropriate for certain situations (e.g. "systems spending a large percentage of time in sleep mode yet requiring ultra-fast wakeup through maintenance of precise logic state"). *See* Ex. 1007, 1, 13. I agree with Dr. Pedram that, depending on the application, Park teaches that the forced stack technique offers several potential benefits over the sleep stack technique. *See* APPLE-1017, 155:12-18, 157:25-158:12, 159:24-160:11, 162:6-164:4, 165:16-23.

APPLE-1018 (Dr. Horst Supp. Decl.), ¶ 48.

Let us focus on the single V_{th} 0.07-μm technology implementation of each benchmark shown in Table II: we see that our sleepy stack approach with single-V_{th} results in leakage power roughly equivalent to the other three leakage-reduction approaches, i.e., forced stack, sleep, and zigzag when each uses single-V_{th} technology. Compared to the sleep and zigzag approaches, which do not save state, the sleepy stack approach results in up to 68% delay increase and up to 138% area increase. Furthermore, compared to the forced stack approach, which saves state, the sleepy stack approach results in up to 118% area increase, but the sleepy stack is up to 31% faster. Thus, we recommend the sleepy stack approach with single-V_{th} when state-preservation is needed, dual-V_{th} is not available, the speedup over forced stack is important and the area penalty for sleepy stack is acceptable.

APPLE-1007 (Park), p. 9.

Contrary to QC's Assertions
Forced Stack Has Advantages Over Sleepy Stack

Cited at Paper 16, p. 23.

Motivation Specific To Context of Steinacker

1. Whether impermissible hindsight was used in the selection and combination of the prior art

   No.

2. Whether the reasons given in the Petition are generic statements divorced from the prior art elements or focus on the specific references used

   No.

3. Whether a person of ordinary skill in the art would have selected the forced stack technique over the sleepy stack technique

   Yes.

Paper 7, p. 40; Paper 16, pp. 13-14, 20, 22-23.

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Mitigation of Alleged Disadvantages Within Skill of POSITA

Adjusting Transistor Size & Threshold Voltage (VT) Mitigates Leakage & Glitch

V. Summary

74. In running the SPICE simulations in this report, it was clear that the setting of the MOSFET thresholds is key to making the circuits function as intended. The FET thresholds determine the input level where POC (power on control) signal is asserted and the levels also affect the leakage once that input level is reached. A key difference in the AAPA circuit and the circuits with feedback is in the setting of the thresholds for the P channel FETs. In all circuits,

76. Circuits with feedback, including the '674 Figure 4 circuit and prior art combinations, do not have the same problem because the gate of the feedback transistor is driven all the way to the high (5 V) rail by the inverter, and that completely turns off the P-channel feedback FET. The other P-channel FETs can have thresholds far below the maximum input voltage to keep them off as well. With a -2.3V threshold and the input at 3.3V, the P-channel FET(s) do not start conducting until the input voltage drops below 5-2.3=2.7V, keeping the P channel strongly off during normal operation when the input voltage is a 3V or higher. Glitch current is reduced to a very low value by setting this threshold near the inverter threshold where the feedback transistor turns off. Thus, with proper thresholds, none of these circuits have high glitch current or high leakage.

APPLE-1018, ¶¶ 74, 76 (cited at Paper 16, p. 9).

Mitigation of Alleged Disadvantages Within Skill of POSITA

Selecting Transistor Sizes Within Skill of POSITA

41. The '674 Patent does not specify V_{th} or R_{on} for the transistors in the circuits in the drawings and specification. The fact that the '674 Patent does not give guidance in the selection of these key parameters indicates that a POSITA should be assumed to have sufficient skill in circuit design to understand and modify circuits in a way that a POSITA would be able to select the appropriate parameters, or to construct stacks of transistors to obtain the desired and useful power detection functionality described in the '674 Patent.

APPLE-1003, ¶ 41
(cited at Paper 16, p. 10).

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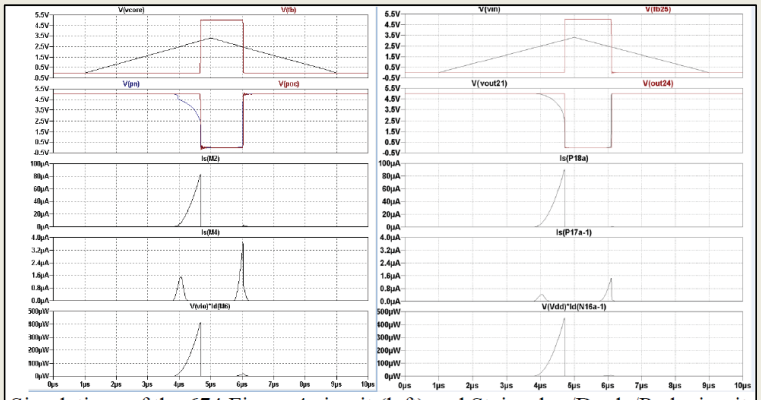
Dr. Horst Confirmed Absence of Disadvantages Through SPICE Simulation



Simulations of the 674 Figure 4 circuit (left) and Steinacker/Doyle/Park circuit (right). Waveforms are nearly identical.

18. The slightly higher peak current of the Steinacker/Doyle/Park circuit on the rising edge causes the peak power dissipation to be about 50 microwatts greater than the 400 microwatts of the '674 Figure 4 circuit. However, this circuit is used for power up/down detection and the input voltage passes through this transition very infrequently. It occurs, for instance, during the brief period when the voltage is first reaching a valid level during the time a portable device is powered up. The small increased power would occur perhaps a maximum of a few times per hour (much less than 1 cycle per second), not at GHz frequencies (a billion times per second) as implied by Dr. Pedram. Ex. 1017, 180:17-181:9. Thus, a POSITA would not have been dissuaded from making the proposed Steinacker/Doyle/Park combination based on these small differences in power.

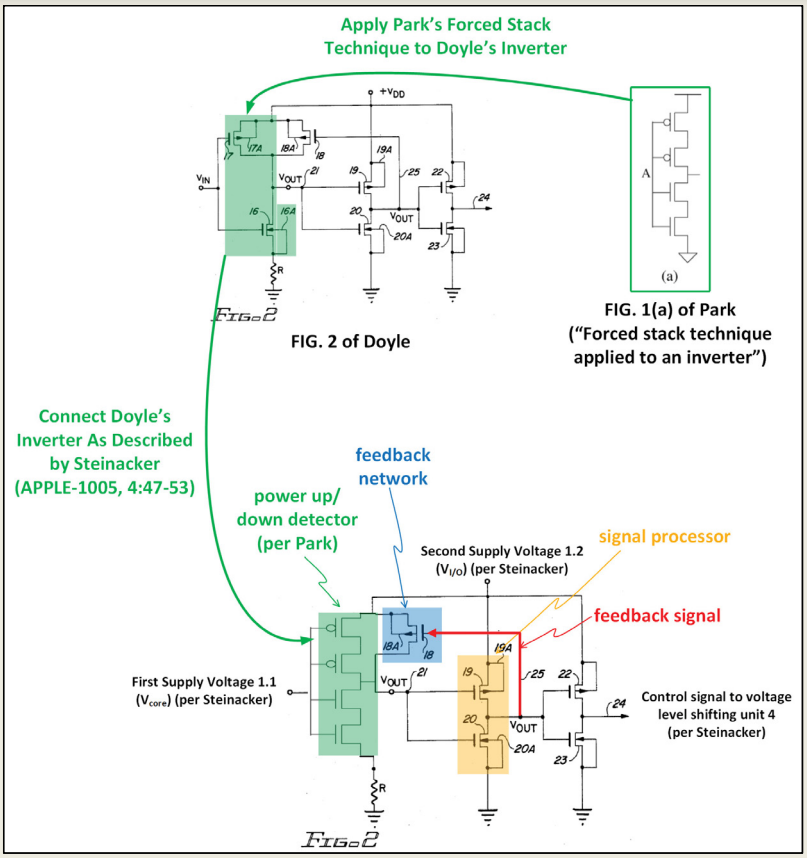
19. The simulations show results that are almost identical. There are small differences in the stack and feedback currents, but the resulting power graphs are nearly indistinguishable. *See* Ex. 1017, 162:6-163:2 (Dr. Pedram agreeing that small differences in the milliwatt to microwatt range make the results in FIG. 17(b) of Park no better or worse than one another).

20. The simulations show that with the chosen simulation parameters, the Steinacker/Doyle/Park circuit does not exhibit the problems imagined by Dr. Pedram. The leakage current is not significantly increased, there are no DC fighting conditions, and there is no breakdown in circuit functionality[4].

APPLE-1018, ¶¶ 18-20
(cite at Paper 16, p. 24).

APPENDIX

Combination of Steinacker, Doyle, and Park

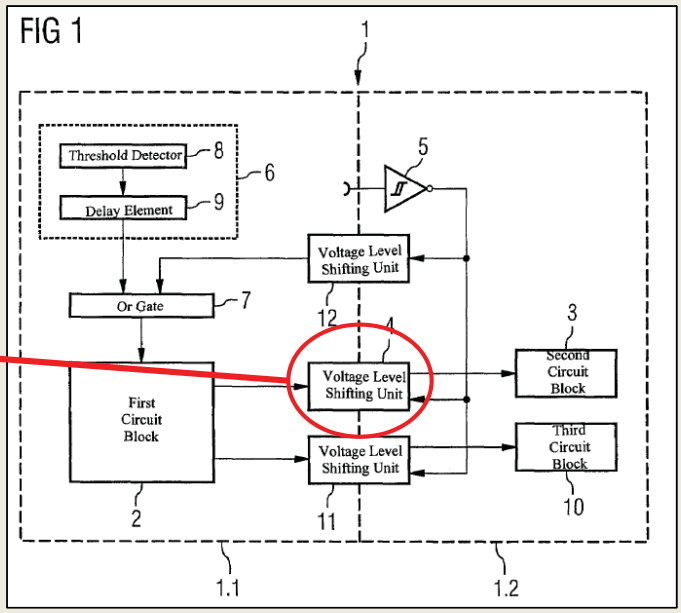


Paper 2, p. 20.

Dependent Claim 5 – Level Shifting Circuit Receives Control Signal

[5.0] The multiple supply voltage device of claim 1 further comprising: an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal.

The combination set forth in Sections III.A.1-5 renders limitation [5.0] obvious. The level shifting unit 4 described by Steinacker is at least a portion of the input/output (I/O) network recited in claim 5. Steinacker describes that the level shifting unit 4 is connected to (and operative at) the second supply voltage via connection 16. *See* APPLE-1005, FIG. 2, 6:25-29; *see also* APPLE-1003, ¶ 94.



Paper 2, p. 35.

Dependent Claim 5 – Mapping Consistent with Analogous Prior Art

[5.0] The multiple supply voltage device of claim 1 further comprising: an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal.

The combination set forth in Sections III.A.1-5 renders limitation [5.0] obvious. The level shifting unit 4 described by Steinacker is at least a portion of the input/output (I/O) network recited in claim 5. Steinacker describes that the level shifting unit 4 is connected to (and operative at) the second supply voltage via connection 16. *See* APPLE-1005, FIG. 2, 6:25-29; *see also* APPLE-1003, ¶ 94.

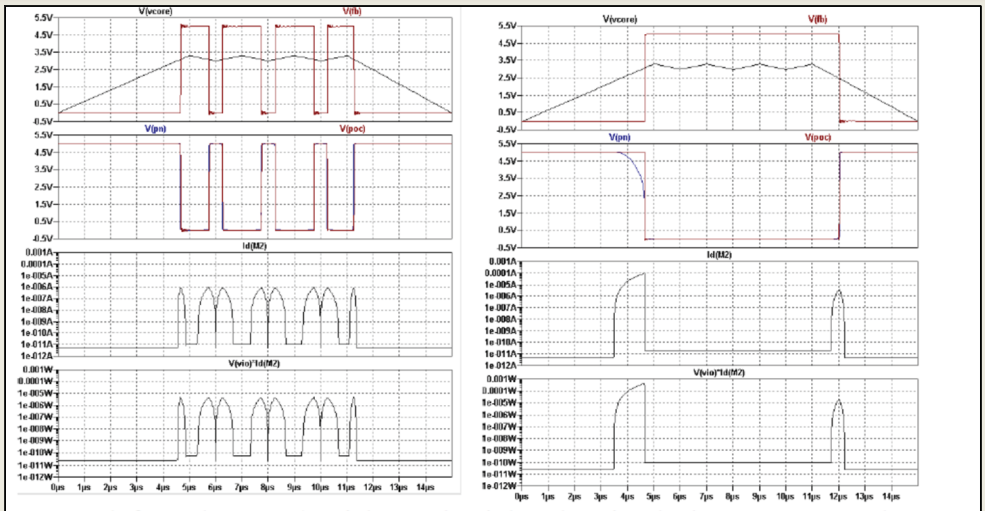
Paper 2, 20.

[**0003**] Since these circuits have to be used in systems whose power supply voltage is higher, the input/output interface circuits include a level-matching stage. For the transmission of output signals, this level matching is carried out by a level translator type selector switch, which receives the interface power supply voltage. This switch matches the levels of the logic signals received from the core of the integrated circuit, and those received from the external circuits with which it exchanges data.

APPLE-1008 (Majcherczak), ¶ 0003 (cited at Paper 15, p. 26).

Analogous prior art classifies level shifting circuits as part of input/output (I/O) network.

Apple's Expert Confirmed Through SPICE Simulation No Increased Leakage Compared to AAPA

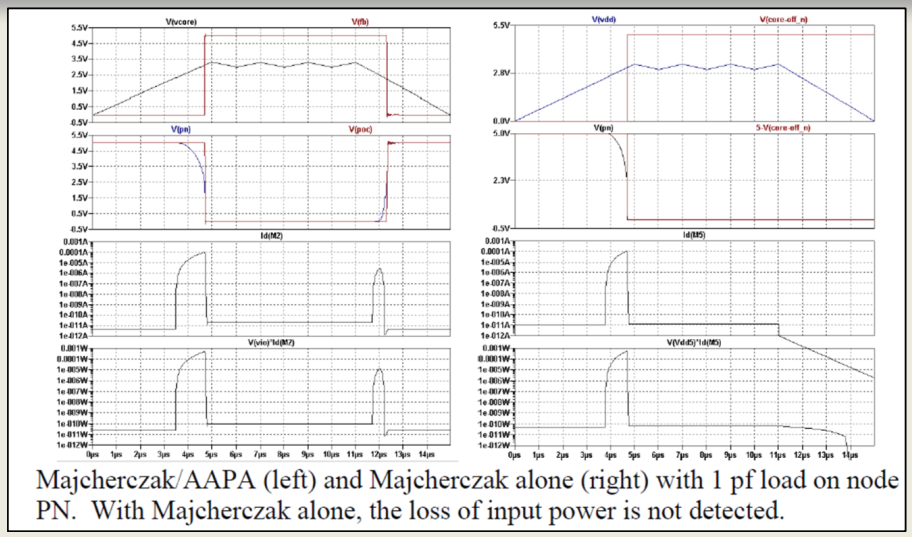


AAPA (left) and AAPA/Majcherczak (right) showing leakage current and power on log scales as input voltage oscillates between 3 and 3.3V.

64. Based on these results, it is clear to see that when the input voltage only slightly exceeds the threshold and is subject to normal variations due to load and noise, the AAPA/Majcherczak combination would have resulted in significant decreases in power consumption over the AAPA. This is motivation to choose the AAPA/Majcherczak combination.

APPLE-1018, ¶¶ 59, 64
Cited at Paper 18, p. 10.

Apple's Expert Confirmed Through SPICE Simulation Negligible Leakage Compared to Majcherczak



Majcherczak/AAPA (left) and Majcherczak alone (right) with 1 pf load on node PN. With Majcherczak alone, the loss of input power is not detected.

71. These simulation results indicate that Majcherczak alone functions in a quite similar manner to the AAPA/Majcherczak combination. Both have hysteresis and nearly identical switching current as the input voltage rises. Both have extremely low leakage during normal operation. The AAPA/Majcherczak combination has a small current pulse when the input voltage is falling, but Majcherczak alone draws almost no current when the input voltage is falling. This might look like a benefit, but in fact it means that the circuit does not actively pull down the PN node when the input is falling. Simulation showed that a tiny

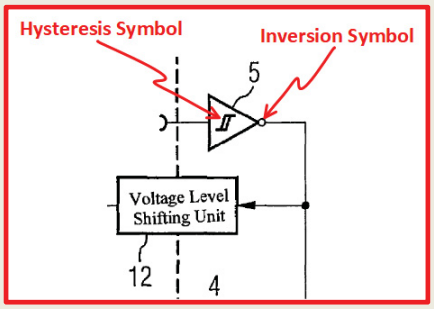
APPLE-1018, ¶ 71
Cited at Paper 18, p. 10.

QC Argues Against Its Own Expert's Testimony

A. Yeah. But, I mean, it's not describing what -- so Figure 1 of the Steinacker just shows a triangle with a bullet at the end that shows it's inverting.

And this particular notation which I describe to you to indicate there's hysteresis between the falling and rising trip point of this inverter. It doesn't have any disclosures about what is inside of that.

APPLE-1017 (Dr. Pedram Depo. Trans.), 139:6-14 (cited at Paper 16, p. 17).



But Petitioner reads too much into Steinacker. The text of Steinacker includes no mention of hysteresis or feedback, much less a "recommend[ation]" to use a voltage level detector with hysteresis. Further, the symbol shown in Steinacker's figure for the voltage level detector 5 is, in fact, a symbol for a Schmitt trigger, which uses hysteresis to have differing trip points. But Steinacker also teaches that in place

QC Sur-Reply (Paper 19), p. 22.

Dr. Pedram Relies On Unclaimed Features to Distinguish Prior Art Combinations

The '674 solution to this problem (as seen in Fig. 4 of '674, for example) is to (i) add a series-connected second PMOS transistor M5 below the first PMOS transistor M4 to reduce leakage current from VI/O to the said output terminal due to the stack effect of series-connected transistors in the pull-up section of the Power U/D Detector 100, and (ii) connect the feedback PMOS transistor M8 only in parallel with the first PMOS transistor M4 and not across the complete pull-up section of the Power U/D Detector 100. In this way, when Vcore is high, the

QC-2002 (Dr. Pedram Decl.), ¶ 72 (cited at Paper 12, p. 24).

1. A multiple supply voltage device comprising:

…

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;

at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

APPLE-1001, 8:44-9:3 (cited at Paper 7, pp. 6-7).