A Sequence Independent Power-on-Reset Circuit for Multi-Voltage Systems

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***Abstract*— With the advent of multiple supply domains on a single chip, issues related to power sequencing are becoming a major hurdle for system designers. Existing POR strategies fail to cope up with these issues. We propose a scheme in which the power on reset generation is independent of the sequence of supply ramp-up. The circuit implementation of the proposed methodology has been realized for a dual supply system. The basic circuit is modified so as to consume zero static current. An attempt to reduce any leakage current during supply rampup has also been made successfully. Simulation results verify the sequence independence concept and low power consumption. Further the proposed realization is modular enough to be extended for more number of supplies.**

I. INTRODUCTION

Many integrated systems utilize multiple voltage domains [1], i.e., the different parts of the chip operate at different power supply voltages. When a digital circuit is powered up, it is usually reset to establish a predetermined state (i.e., initial digital values are populated in registers, memory, etc.). For chips containing multiple voltage domains, some existing POR (Power-on-Reset) techniques only detect the ramp-up of the power supply that occurs last in time. Until this time, however, the state of the POR signal or signals is undetermined. This may lead to unexpected behavior of the chip, such as contention in tri-state logic circuits and/or undesirable R/W operation of memory circuits. All such conditions can lead to excessive and undesirable current consumption. The need for multi-voltage supervision and voltage detection mechanism is addressed in [2]. Some other POR techniques are shown in [3-7] but they are either sequence-dependent or detect a single supply with reference to the other. Since the ramp-up sequence of such circuits needs to be predefined, a random power-up sequence may lead to system failure. Some designs also use separate POR circuits for different supply domains. This can also lead to synchronization issues between them.

Accordingly, it is desirable to have a sequence independent POR methodology for use in a multi-voltage architecture. In addition, power supplies have large ramp-up times and hence it is desirable to have a circuit implementation that minimizes steady state and dynamic current consumption associated with the generation of POR signals for use in battery operated applications.

II. CONVENTIONAL POR METHODOLOGY

Fig. 1 shows the above scenario in a general perspective with 'n' number of supplies. It is clear from the figure that the signal RESET (assumed to be active LOW) is not driven till the last supply VDDn does not ramp-up. The dotted lines show the region (POR Region) where the RESET is driven and recognized by different supply domains.

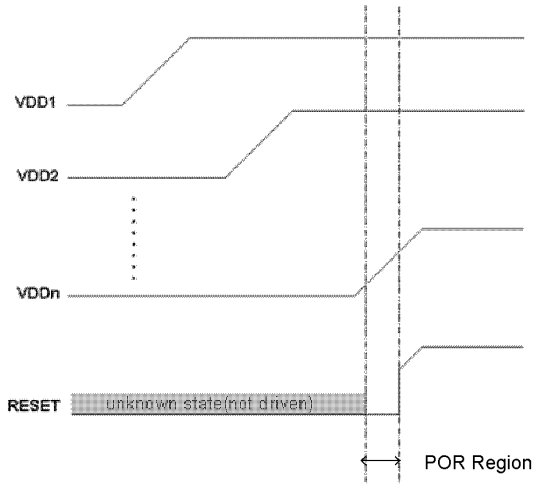

Figure 1. Waveform showing conventional POR Methodology

Till the time the last supply VDDn appears the RESET is not driven to any logic level. Also, if the ramp-up sequence is changed, some supply domains may not be able to register a valid reset and will malfunction.

III. PROPOSED POR METHODOLOGY

Fig. 2 shows the proposed POR methodology where the reset generation is sequence independent. Unlike the RESET waveform in Fig. 1 the RESET is asserted LOW as soon as any supply appears and hence avoids the hazards mentioned

in Section I. The RESET is de-asserted at the ramp-up of the last supply.

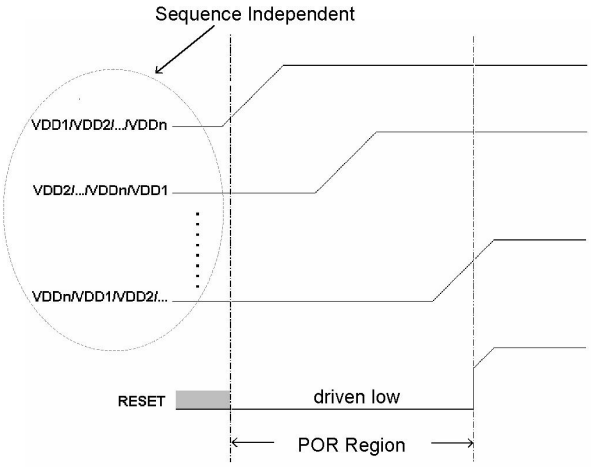

Figure 2. Waveform showing Proposed Reset Methodology

IV. NAND Logic as a Por

The basic implementation of the proposed methodology can be realized using a dual-supply NAND gate as shown in Fig. 3. As shown in Table 1, if one input is 0 (Logic LOW), the output is 1(Logic HIGH) and only when all the inputs are 1 (Logic HIGH) the output switches to 0 (Logic LOW). When none of the supplies are present, the node POR_OUT remains floating.

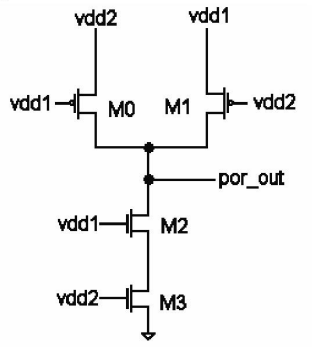

Figure 3. Basic NAND gate structure as multi-voltage POR.

TABLE I. LOGIC TABLE FOR NAND GATE AS A POR

VDD1	VDD2	POR_OUT
1	1	1
1	0	0
0	1	0
0	0	X

Thus, the POR remains asserted if any of the supply is absent. POR is de-asserted when all the supplies are ramped up. POR Thresholds can be adjusted by appropriate sizing of the transistors. The drawback of this circuit is that if the voltage levels of vdd1 and vdd2 are not equal, there will be steady state power consumption in the circuit once both the supplies ramp up. This power consumption is proportional to the difference between the two supplies and is hence not suitable for low-power applications. To reduce the static power consumption, it is required to add control circuitry to the PMOS gates of the circuit in Fig. 3 to ensure that the pull-up paths are completely turned off once all the supplies are ramped up.

V. Low Power Implementation

Fig. 4 shows the POR circuit with control circuitry for two-supplies. Assuming vdd2 ramps-up first. Node n1 is pulled LOW by M5 and PMOS M1 turns OFF. Due to capacitive coupling (C0) the node n2 follows vdd2, output of inv2 goes LOW and hence the PMOS M0 charges output node por_out to logic HIGH. When supply vdd1 ramps up, M4 pulls node n2 LOW and hence output inv2 goes HIGH turning OFF M0. NMOS M2 and M3 turn ON and por_out goes LOW. At steady state, both PMOS are OFF and there is no path from supplies VDD1 and VDD2 to ground. Since the circuit is symmetric w.r.t. VDD1 and VDD2 the sequence of supplies will not affect the operation thus making the circuit independent of supply ramp-up sequence. The inverters, inv3 and inv4, are used to level shift the node por_out to the respective supply domains.

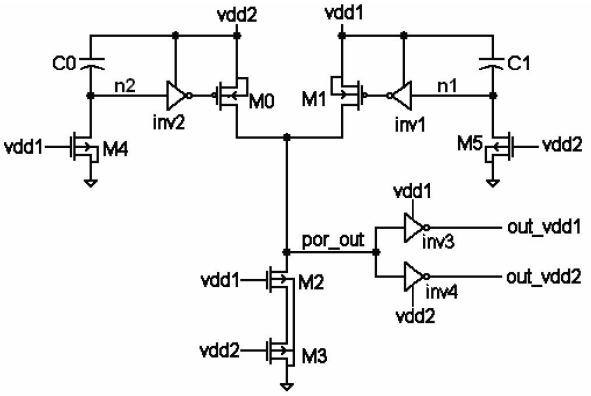

Figure 4. Dual Supply POR with Zero static current consumption

Though circuit in Fig. 4 does not consume any steady state current, there exists a path between the two supplies, during the period when only one supply is ON and the other is not present (ground), through M0 and M1. To avoid this situation, the circuit in Fig. 5 has PMOS M6 and M7 to cutoff the direct path between the two supplies during ramp-up. Now, consider a situation when the node por_out is high indicating that only one of the supplies has ramped up. The body diodes of the PMOS pull up structure of the supply that is not ramped up can get forward biased and cause a huge

drain from the supplies. Thus, even though M6 and M7 turn OFF, their body diodes conduct and create a leakage path. To prevent this body leakage, an adaptive body bias scheme has been employed. As shown in Fig. 5, the body is dynamically switched from the output voltage level (when only one supply is present) to the respective supply voltage level by controlling PMOS transistors M8 and M9.

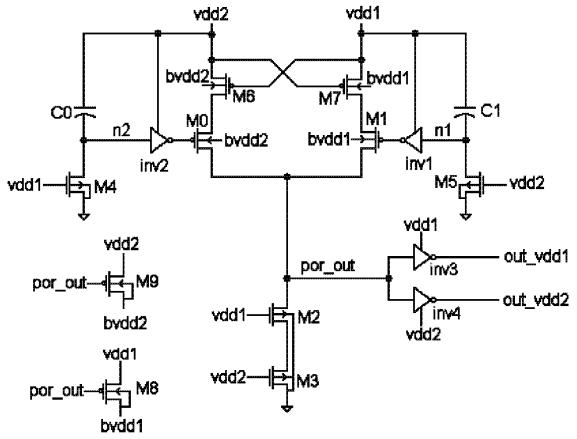

Figure 5. Dual Supply POR with Ultra low current consumption

VI. Simulation Results

The circuits were implemented in 90nm CMOS Bulk Process and simulated in SPICE. Fig. 6 and Fig. 7 show the waveforms with two different ramp-up sequences. It can be inferred that irrespective of the sequence, the reset signals out_vdd1 and out_vdd2 remain asserted LOW when any of the supply is not present and de-asserts only after both the supplies have ramped up. From Fig. 8 it can be seen that the current drawn from the supplies is negligible during and after power up. Fig. 9 shows simulation results for the adaptive body-biasing technique employed.

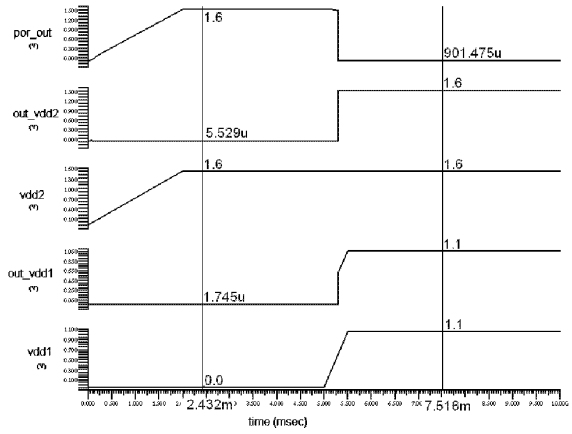

Figure 6. POR response with ramp-up sequence VDD2 => VDD1

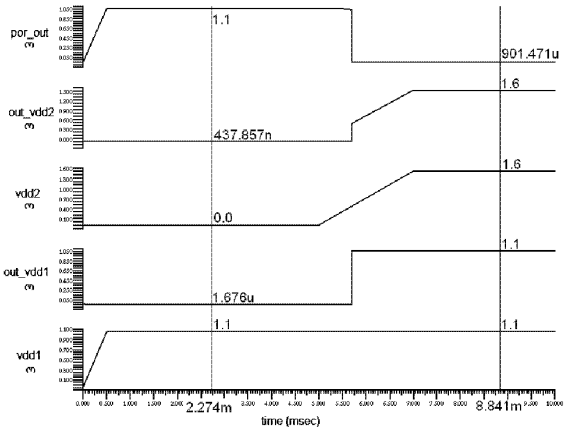

Figure 7. POR response with ramp-up sequence VDD1 => VDD2

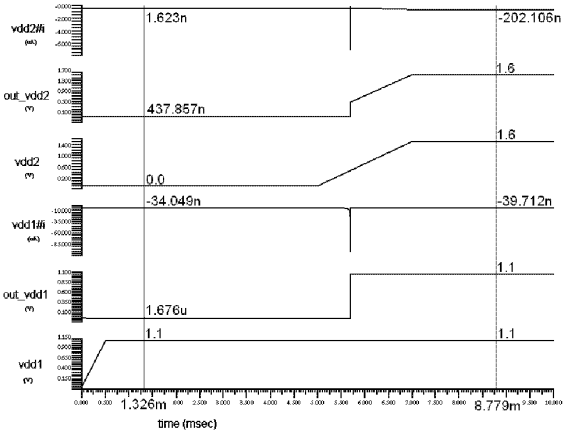

Figure 8. Waveforms showing current consumption with ramp-up sequence VDD1 => VDD2

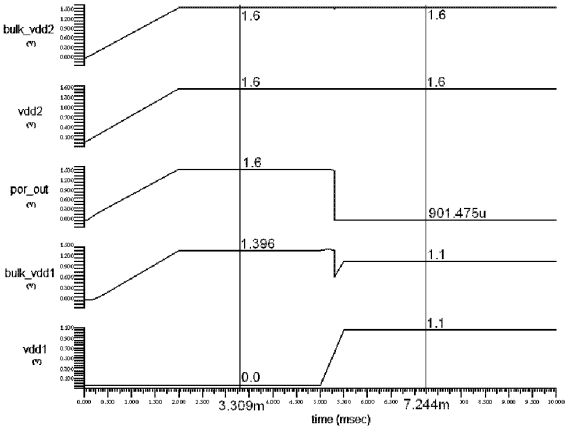

Figure 9. Response of Adaptive bulk bias scheme with ramp-up sequence VDD2 => VDD1

VII. Extension for more than Two Supplies

Fig. 10 shows the modularity of the circuit by using two dual-supply POR circuits (shown in Fig. 4 and Fig. 5) to realize a quad-supply POR circuit. The outputs of the individual dual-supply POR circuit are combined in a Sync Logic that synchronizes all the resets such that they are deasserted at the same time while maintaining the sequence independent nature of the circuit. The same architecture can be used for a tri-supply POR circuit by grouping vdd3 with vdd2 or vdd1 in the second dual-supply POR circuit.

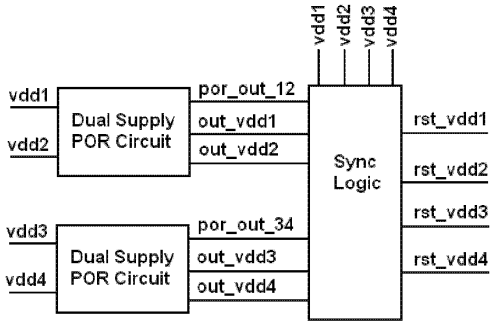

Figure 10. POR Generation for Four Supplies using Dual Supply POR

Fig. 11 shows the circuit implementation of Sync Logic. It consists of four similar structures to generate the resets rst_vdd1, rst_vdd2, rst_vdd3, and rst_vdd4 at the respective supply levels. It primarily contains a NOR gate logic and uses the outputs generated from the two Dual Supply POR circuits. Consider the Logic portion for generation of rst_vdd1. Initially, if vdd1 ramps-up first, then por_out_12 goes HIGH. Also capacitor C couples the supply to ctrl_vdd1 and is latched at vdd1 level. Thus, the node rst_vdd1 goes low. Now, if vdd2 ramps-up por_out_12 goes low, but since ctrl_vdd1 is latched, rst_vdd1 remains low. Else if vdd3/vdd4 ramp-up, out_vdd3/out_vdd4 goes high so as to turn off the pull-down NMOS receiving signal out_vdd3/out_vdd4 at the gate, but since por_out_12 is high rst_vdd1 remains low.

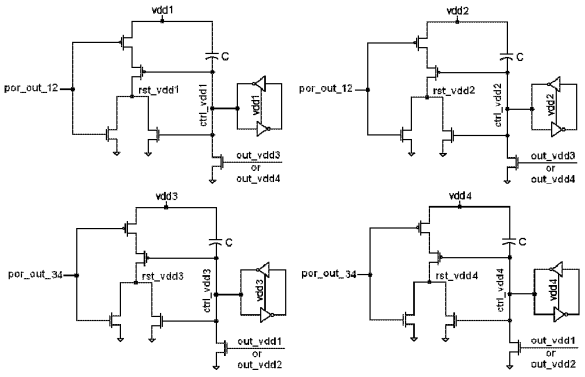

Figure 11. POR Sync Logic for 4 supplies

If vdd1 ramps up later in time with respect to other supplies, it is ensured that the signal rst_vdd1 goes low as soon as vdd1 ramps-up. Thus, once all the supplies ramp-up and por_out_12 goes high and out_vdd3/out_vdd4 goes low, reset de-asserts. All the Sync structures are similar and operate in the same fashion. As soon as any supply ramps up, the reset corresponding to that supply gets asserted. The reset de-asserts only when all the supplies ramp-up. The circuit avoids any kind of static current consumption due to difference in the levels of the supplies.

Fig. 12 shows the generalized Sync Logic structure for i^{th} supply (where i = 1 to n; and n is the number of supplies). The operation is similar to the circuit in Fig. 11.

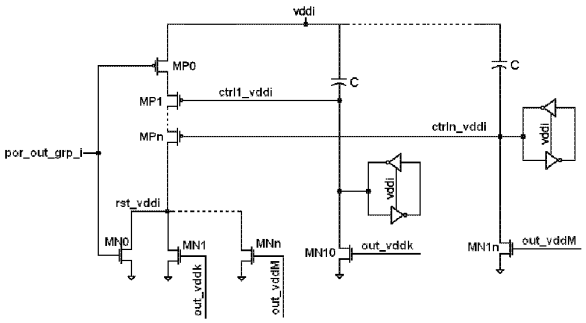

Figure 12. Sync Logic for i^{th} out of n (>4) supplies

VIII. Conclusion

A sequence Independent POR methodology suitable for a multi-supply domain IC's has been presented. The concept ensures the reset synchronization between multi voltage domains. The POR is driven at the appearance of the very first supply and prevents any malfunctioning of the chip. This eases post-silicon testability and can be used to arrive at the optimum power-up sequence after fabrication of the chip. The technique has been successfully implemented for dual-supply with zero static current and negligible dynamic current. The circuit implementation is modular in nature and can be easily extended for more than two supplies.

References

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