A REVIEW OF SEMICONDUCTOR PACKAGING AND ITS ROLE IN ELECTRONICS MANUFACTURING

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ABSTRACT

The low cost functionality brought by semiconductor technology is the most important factor in the widespread use of electronics. Interconnection and assembly technologies enable semiconductor science to bring its processing power to fulfilment in overall systems integration. The small semiconductor structures must be brought into contact with the outside world. Together with suitable substrate technologies, semiconductors can be used in any of the forms available, from bare dice to encapsulated, tested and burnt-in complex functions in LSI. This review examines the development of semiconductors, with the emphasis on the forms of packaging available. Until the dream of total self-sufficiency of silicon becomes a reality more and more innovative and complex means will be proposed to deal with the problems of ever increasing lead counts, some of which will mature into manufacturing methods. Designing on silicon has a strong influence, bringing into focus the fact that interconnection adds cost not functionality, this latter lies in the silicon.

INTRODUCTION

Electronics started by using semiconductors but the early detector crystals and oxide rectifiers had little impact outside their immediate area of use. Where amplification or nonlinear signal processing was needed thermionic devices prevailed until semiconductor microwave diodes ousted thermionic types in the 1940s. The invention of the transistor started the modern technological revolution that has changed the whole industrial scene.

Early semiconductors, mostly in germanium, had open pn junctions with a high susceptibility to moisture and needed hermetic encapsulation. This meant that little choice was available in packaging. Silicon was handicapped by the material properties and its use was restricted to areas where its technical properties were needed.

The invention of the diffused planar method of fabrication brought silicon to the fore as the material for low cost high performance transistors. The planar process involves the thermal growth of silicon dioxide on a silicon wafer which acts as a mask to the gaseous dopants used during diffusion and remains after as a hermetic seal over the pn junction. Planar processing gives significant advantages in manufacturing methods for silicon semiconductors.

Photographic imaging and chemical etching can define multiple, very small diffusion windows over a large area enabling many devices to be processed simultaneously on single wafer.

Control over diffusion processes enables a high degree of uniformity and reliability to be obtained at low cost.

Oxide protection of the junctions, inherent in the process, removes the need for hermetic encapsulation, allowing low cost device packaging in plastic.

Planar methods encompass bipolar and field effect structures.

CH2833-2/90/0000- 0405 $1.00 ©1990 IEEE

The oxide can support metal connections defined by photographic means on a microscopic scale between diffused areas, diffused tracks can also be used under the oxidise so enabling multi-level wafer interconnection.

Continuous refinements in technology have lead to Small Scale Integration (SSI), Medium Scale Integration (MSI), Large Scale Integration (LSI) and Very Large Scale Integration (VLSI) with the promise of Wafer Scale Integration. In achieving this the high involvement in circuitry of semiconductor manufacturers has lead to them a having a significant amount of the initiative in electronics.

Basic semiconductor parts - transistors and ICs are cut from the wafer into "die" or "chips" which are small and inaccessible for connection using normal assembly processes. For technical and economic reasons, the silicon in a transistor or an integrated circuit should be no larger than the diffused areas dictate. Bonding pads do not contribute to the function and must be minimised in area, well below the size which would allow for direct connection to a PCB. Presenting the devices to the user in a practical form is part of semiconductor manufacturing, a large sector of which is given over to packaging.

FEATURES OF PACKAGING

It allows handling the devices on a scale compatible with other components for testing, grading and assembly - automated or otherwise.

It protects against physical damage during assembly and use.

Type, date code and other information can be printed on the package.

Much of the added value is in the packaging which is something the semiconductor manufacturers are unwilling to forgo.

Packaging involves several operations, some physical, some electrical, some both.

Mounting:

The dice must be physically held on a supporting structure - header, lead frame or substrate. This may include making some or all of the electrical connections. Mass production of "conventional" semiconductors uses die bonding to locate, fix and in some cases electrically connect the dice, the latter for example in bipolar transistors where a low ohmic connection between the die and substrate is needed. Bonding may be by metallurgical means, by forming a gold/silicon eutectic or soldering. Alternatively gluing can be used with the glue having metallic additives for electrical conductivity. Eutectic bonding is strong and convenient to mechanise. No materials other than the silicon die and a gold plated headers or lead frames are needed. Thick Film gold will work for this purpose also. The process used a fairly high temperature and does not find favour in multi-chip applications for this reason. Gluing is an alternative for both single and multi-chip applications, with mechanisation being possible. As it reduces the amount of gold needed, gluing offers savings in materials. It offers flexibility of choice on mounting materials and finishes due to low processing temperatures.

Connections:

Connectioning to the bonding pads on "conventional" semiconductors is a further operation. Fine wires of gold or aluminium are diffusion bonded to the metal pads and taken to the terminals of the package. The process uses pressure, temperature, and frequently ultrasonic energy. Aluminium predominates for metallisation but where additional passivation is required more complex metallisations are adopted using noble and refractory metals.

Protection:

The silicon dice and fine wires needs protection against physical damage and chemical contamination. Protection can be by a metal enclosure around the dice or by embedding it in plastic. The use of plastic is widespread and, whilst not truly hermetic offers protection to a level suitable for the most applications. Plastic allows a high degree of mechanisation and standardisation, both at the manufacturer's and user's end.

Alternative die types:

By modifying the processing the mounting and connections may be integrated into one process. Some processes use totally different wafer processing - Beam Lead for example - some use the standard processing up to a late stage in the wafer processing - flip chip, TAB for example.

The forms of semiconductor dice and the packaging options are discussed below.

DEVICES FROM STANDARD DIFFUSION PROCESSING

Direct Die Mounting on to Substrates - Chip & Wire, Chip-on-Board.

Film technologies developed alongside silicon planar. As no Surface Mounting Types were available to start, the inconvenience of mounting wire ended devices on to surfaces without holes could be avoided by using elemental silicon dice and treating the substrate as a header. Dice directly mounted on substrates gives very high density packaging and is, in principle, low cost - but there are technical and commercial problems to be overcome.

Problems and solutions:

Semiconductor manufacturers are being asked to supply a product with most of the value yet to be added. They draw attention to the problems and support a lobby favouring encapsulated devices. The difficulties can be overcome and the advantages make the technology attractive.

Wafer scribing with a diamond could damage dice. This could cause whole circuits to be rejected with only one bad die on them. The use of wafer sawing has all but eliminated this problem.

Device checking at the wafer stage is by probing to sort out absolute rejects, with no attempt at measurement and grading into parameter groups. However parameters vary gradually with position on the wafer so that large areas contain very similar devices. Sampling can characterise devices and be used to map wafers. Sample die can be used for stress testing to assess long term reliability. The semiconductor manufacturers could do this it is pointless when devices are going to be finally tested anyway.

Hybrid circuit manufacturers had to acquire specialised knowledge, skills and machines. For some time the only equipment available was designed for mounting on headers or lead frames and ill suited to hybrid manufacture. Attempts to adapt machines never had much success. Hybrid manufacturers initially had to make a lot of their own equipment and developed associations with machine makers or spawned breakaway groups to create sources for suitable equipment. The general availability of equipment today is helping to speed the adoption of chip and wire assembly on hybrid and PCBs.

Device degradation due to exposure to high the temperatures of eutectic bonding lead to gluing, now in general use by the semiconductor manufacturers. The use of conductive adhesives for die mounting can, by using good back metallisation on the wafer, give electrical characteristics better than eutectic bonding. For most ICs, with all connections on the top surface, using cheaper, nonconducting, adhesives is possible. Thermosonic gold wire bonding at about 150 deg. C, gives no measurable device deterioration but restricts substrate materials. Ultrasonic aluminium wire bonding, done at room temperature, can be applied to most metallisations on organic or nonorganic substrates. Mechanisation of aluminium bonding is complex but well supported with equipment.

Commercial Aspects

Semiconductors from differing diffusion sources, Bipolar, FET, Digital, IC, Discrete, Non-Silicon - GaAs, GaAsP LEDs etc. can be combined in a high density fashion on hybrid and PCB in a way that SM on PCB cannot rival in density and performance nor monolithic on its own in the combination of technologies.

Semiconductor manufacturers support chip and wire dice rather reluctantly. Frequently dice are treated as specials and offered only via die houses, at a very high added cost. This has restricted use to high cost, high density military/avionics type applications where the cost, due to multiple die handling by intermediaries can be accepted. That the use of naked dice is sound and economically viable is clear from their use by equipment manufacturers having their own semiconductor operations, a example is car electronics, where cost, reliability, ruggedness and performance are extremely challenging. An exception to the reluctance to supply dice is in the area of custom and custom ICs with most of the added value in the design and wafer processing. Many suppliers of custom and semicustom ICs prefer users to take wafers and sort out their own encapsulation.

Substrate requirements for direct bonding of dice:

Direct bonding to substrates is applicable over the whole range of semiconductor devices - from micro wave with devices on micro-strip having dimensions below 200 microns square, to LSI and large power devices up to 1cm square.

Conductive epoxy die bonding can be done on all substrate materials, plated copper on PCB, Pd/Ag & Au on thick film as well as Au or Ni on thin film. On bipolar devices saturation voltages are low and consistent. To satisfy some specification gold loaded epoxy may be substituted for silver loaded epoxy although usually the only difference to be seen is the cost. Bipolar devices need back metallising such as Ni, Au or various alloys, usually put on by the semiconductor supplier. Power devices with larger areas, having the need for high electrical and thermal conduction may be soft soldered. This is an

established technique on hybrid substrates and as a production method is done without flux, in an inert atmosphere, using a oven. The fairly close match between the thermal expansion of alumina and silicon alleviates the problem of solder crystalisation due to thermal stress (this is a characteristic of devices mounted on copper headers, forcing other methods or intermediate metal layers to be used). Jigging and weighting the dice, metering the solder by printing and good oven control will ensure a void-free joint. The method is not applicable to PCB as the materials have generally poor thermal conduction.

Wire bonding needs gold substrate metallisation. The effect of high material costs when using gold on thick film can be minimised by applying it only on the small area needed for bonding. On PCBs a soft gold coating of a few tenths of a micron is sufficient. This can be selectively plated but it must have a nickel barrier layer under to suppress copper diffusion into the gold. Aluminium wire may be applied by wedge bonding on cold substrates with wires up to 250 microns diameter. Aluminium wire is frequently used for power devices because it is economically obtainable in much heavier gauges than gold.

Plasma de-smearing can improve bond strengths on PCB and alumina substrates. Plasma cleaning appears to have no measurable effect on other substrate properties, such as resistor characteristics.

SO/SOT Devices.

Hybrid production in companies with no semiconductor experience makes solderable encapsulated active devices preferable. Users struggled with formed wire ended types until SOT devices, first made for use on PCBs in the 1960s, together with the SO IC versions became available. Diodes can also be supplied as Metal ELectrode Face bonded (MELF) format, wire ended devices with the wires left off. The use of surface mounting on PCBs means the availability of devices in these packages is extensive and expanding, with good availability. They are favoured by the semiconductor manufacturers who see more added value than on naked dice. Their use, and the associated problems are well reported. Some general comments can be made however. 90% of companies in electronics assembly do not make anything other than joints. The secret of success is obtaining good material and making good joints. Solder has been the traditional means to make connections to Dual-in-Line (DIL) devices and extended to SOT/SO, where it is frequently used to hold as well as connect. With four times the surface density of DIL, greater care needs to be taken to ensure that good joints are made, leads must have solder only on the joint areas. Too much will reduce the compliance of the leads and cause eventual failure during thermal cycling. Whereas passive components can have metallisation suited to epoxy adhesive attachment or solder, SOT/SO devices, having tinned leads, are only suited to solder attachment. Design rules, manufacturing control and production line discipline have to be more stringent with surface mounting.

As lead counts rise, packages with leads down two sides cease to be effective. The extension of the leads to the extremities can only be achieved by increasing the package width, due to the minimum limits on tracks and spaces. Reduction of spaces from the DIL 0.1" to the SO 0.05" and 0.03" or even 0.02" means a very small width lead with very thin material and this brings a problem of lead stability. Lead counts over 40 are rare for SO. For higher lead counts all four sides of the package are used. Packages of this type are available in both hermetic and plastic versions.

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