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(54) **POWER SUPPLY DETECTION DEVICE**

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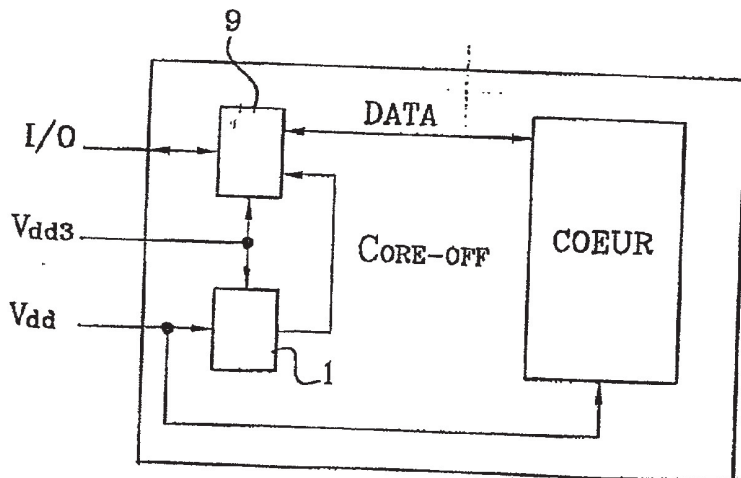
(57) **ABSTRACT**

In an integrated circuit, a detection device detects a drop in the supply voltage of the core of the integrated circuit or an excessively slow build-up of this voltage with respect to a supply voltage of the input/output interface circuits of the integrated circuit. Outputs of the interface circuits are set to a high impedance state by the detection device to minimize their power consumption.

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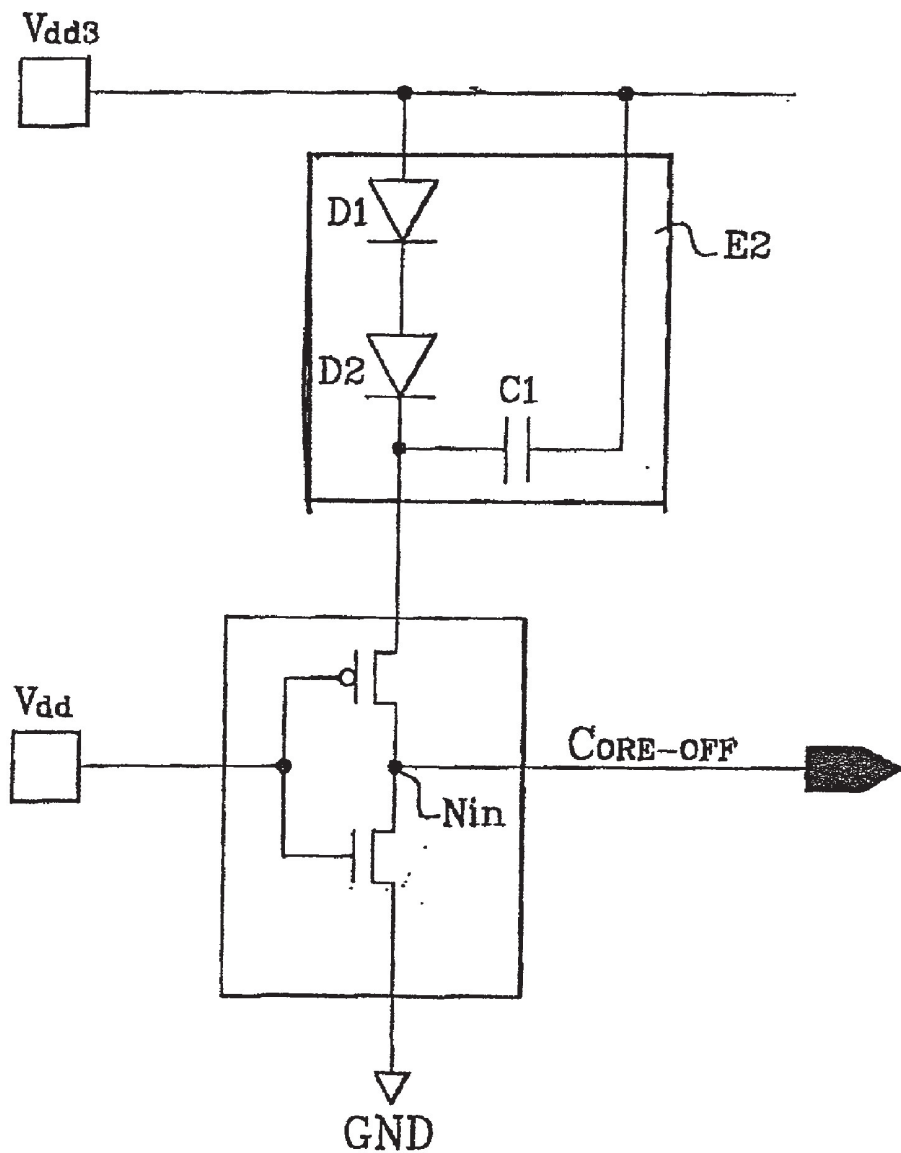


Fig. 1

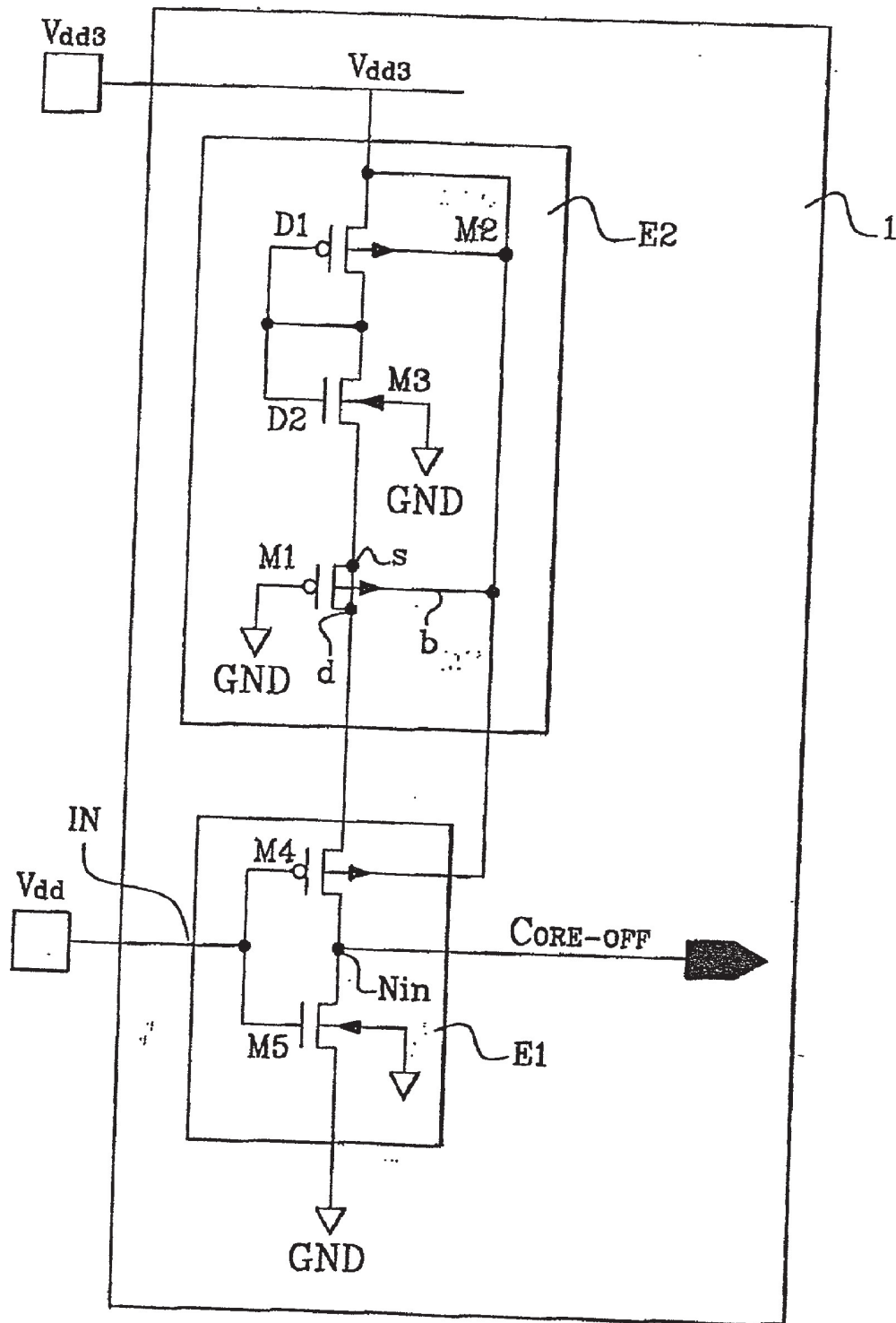


Fig. 1 bis

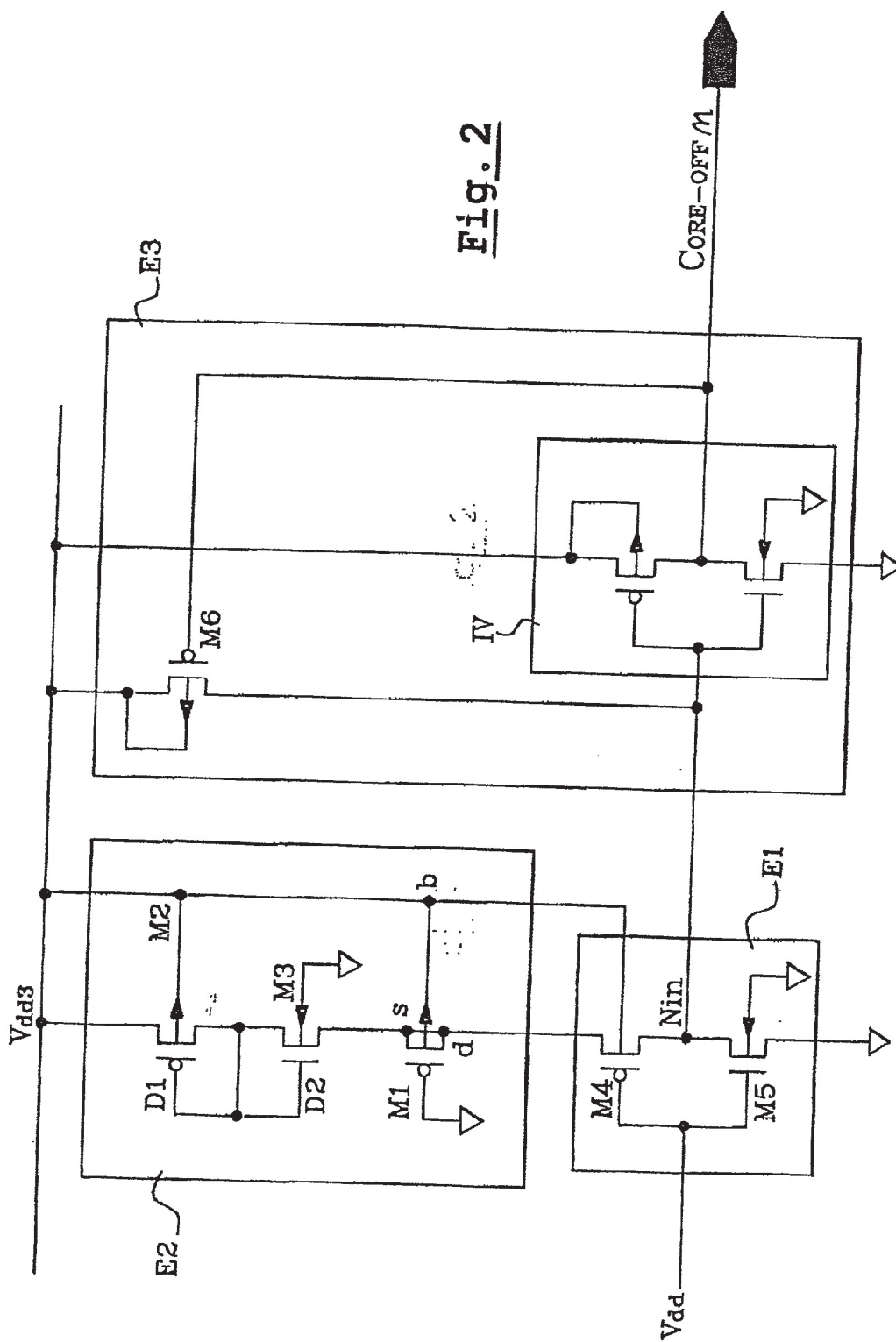


Fig. 2

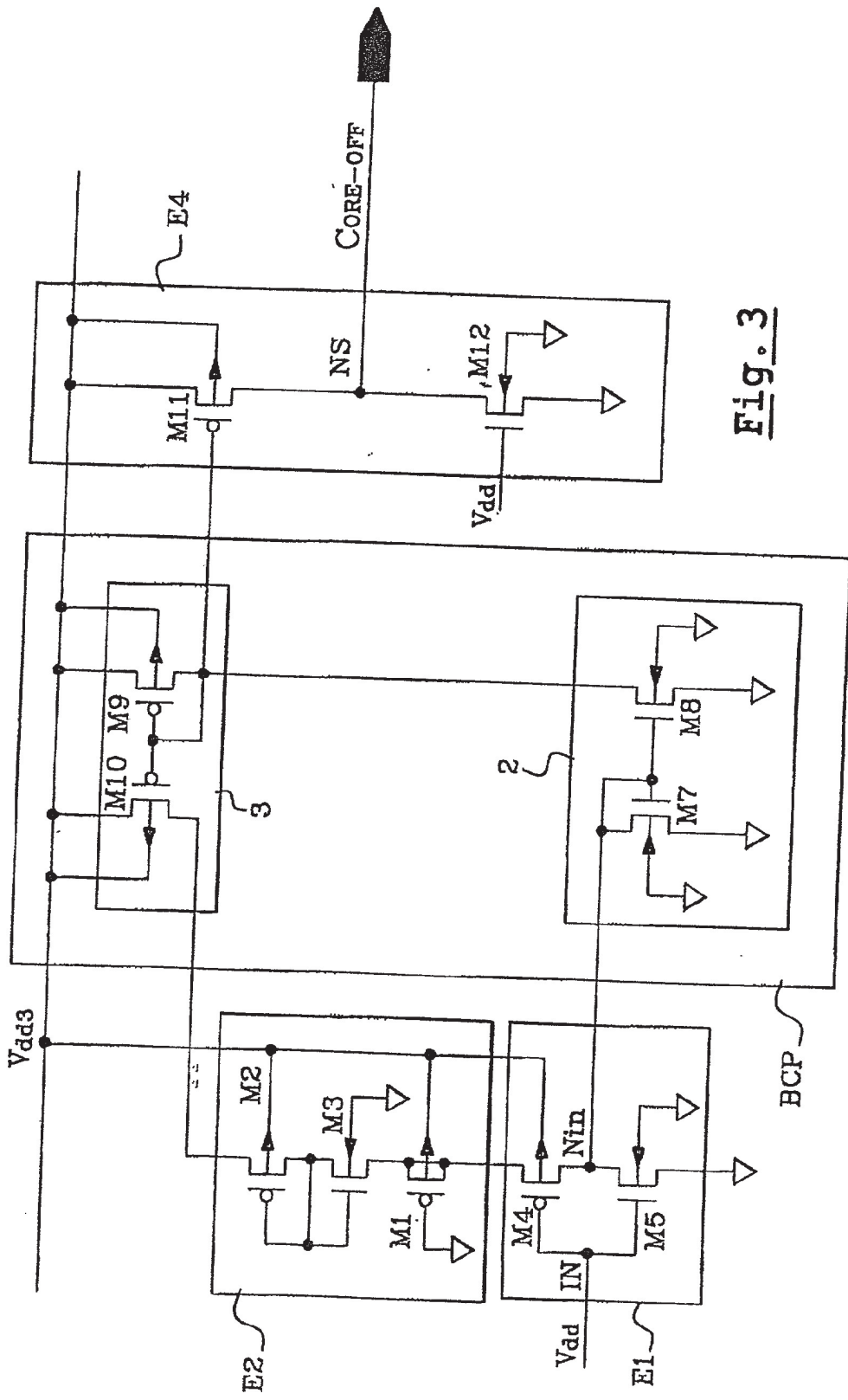
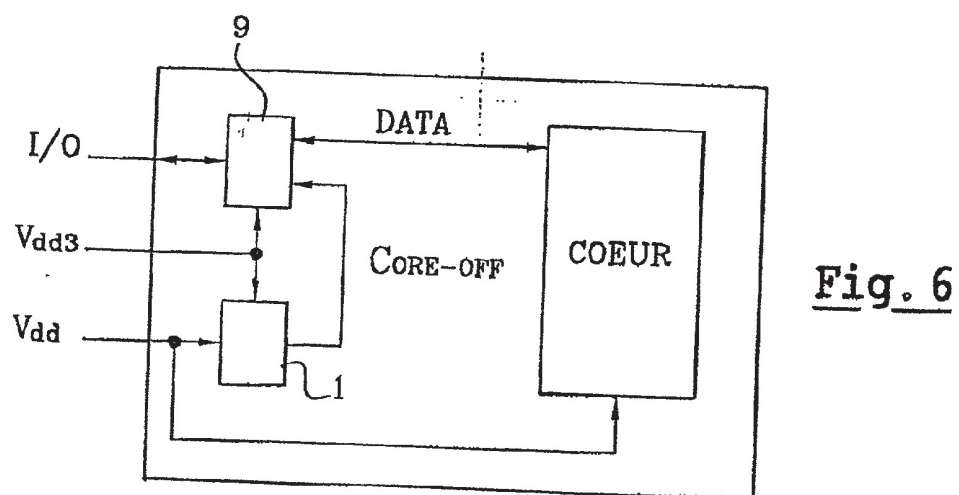
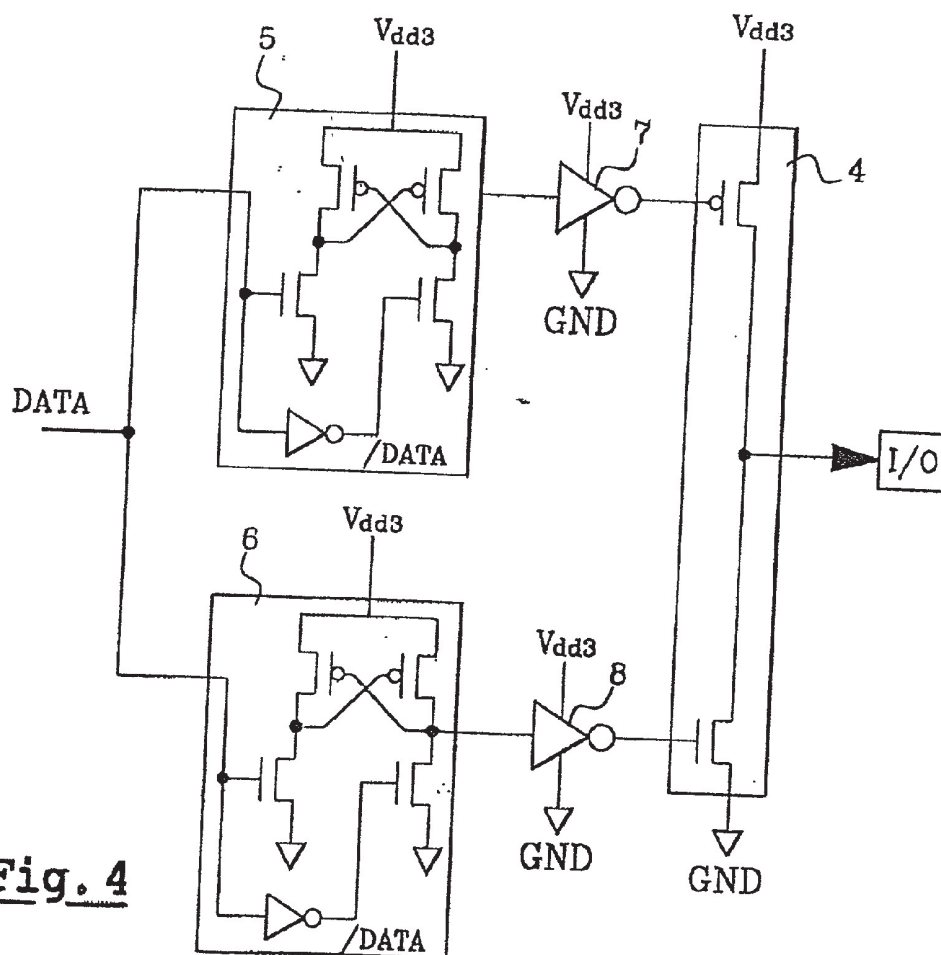
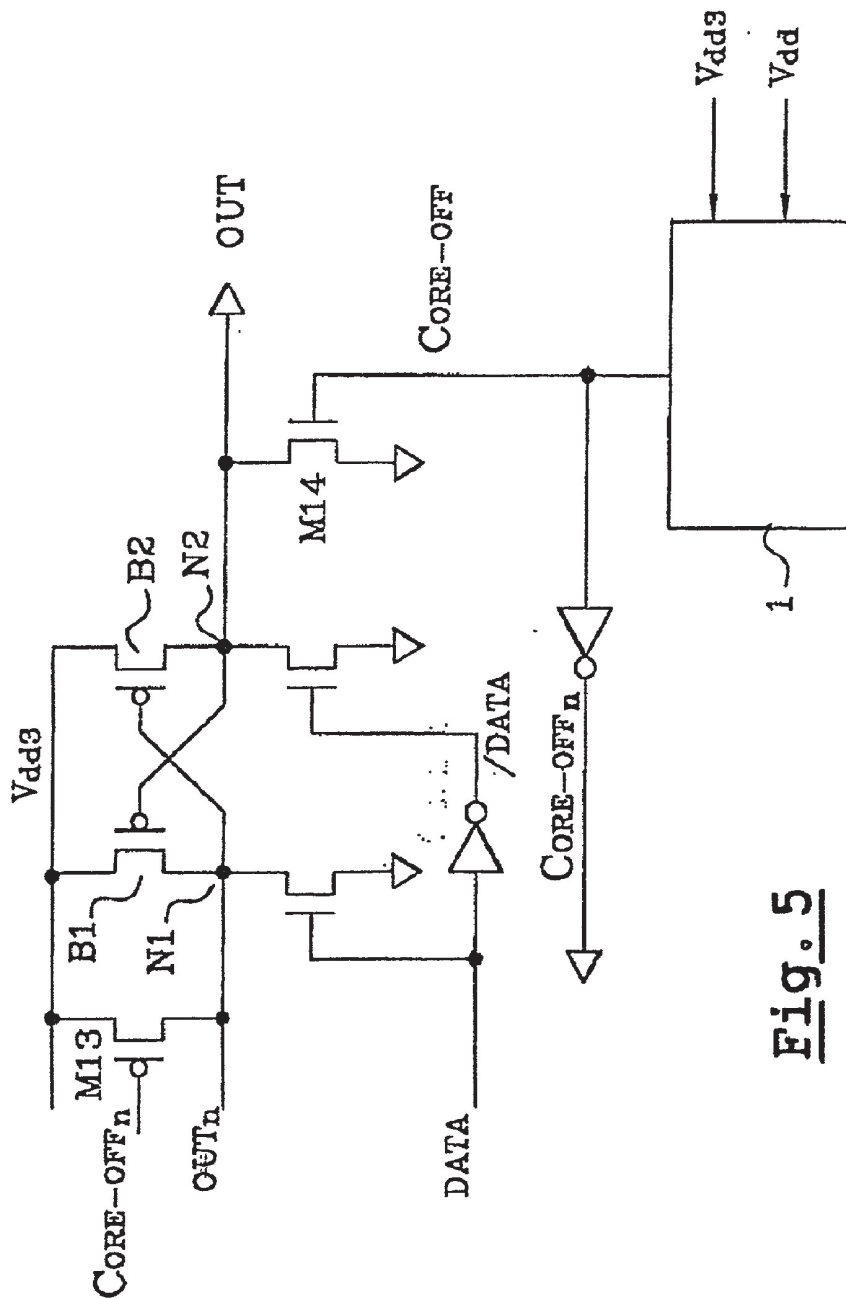


Fig. 3





**Fig. 5**

## POWER SUPPLY DETECTION DEVICE

### FIELD OF THE INVENTION

[0001] The present invention relates to power supplies, and more particularly, to a power supply detection device for an integrated circuit using at least two power supply voltages. One power supply voltage is for a core of the integrated circuit, which is defined by the manufacturing technology of the circuit. The other power supply voltage is a voltage greater than the power supply voltage for the core, and is applied to external interfaces of the integrated circuit and to input/output interface circuits within the integrated circuit.

### BACKGROUND OF THE INVENTION

[0002] Integrated circuits with a distinct core supply voltage and a distinct interface supply voltage have appeared with new manufacturing technologies used to make low-voltage integrated circuits. For these circuits, the core voltage has fallen to 1.8 volts in certain technologies (0.18  $\mu$ ) and 1.2 volts in other technologies (0.12  $\mu$ ).

[0003] Since these circuits have to be used in systems whose power supply voltage is higher, the input/output interface circuits include a level-matching stage. For the transmission of output signals, this level matching is carried out by a level translator type selector switch, which receives the interface power supply voltage. This switch matches the levels of the logic signals received from the core of the integrated circuit, and those received from the external circuits with which it exchanges data.

[0004] Internal control signals are commonly used to control the interface circuits. Some of these signals also go through the level translators. As for the signals received at input from the integrated circuit, they enter with an interface voltage level. Their level must therefore be lowered.

[0005] It has been observed that these input-output interface circuits are the site of malfunctions related either to the disappearance of the core supply voltage, or to the fact that the build-up of this voltage is slower than that of the interface supply voltage. In both situations, the level translators of the interface circuits do not work properly, and malfunctions are seen in the integrated circuit.

[0006] It may be recalled that level translators commonly have a structure with two arms, each comprising a control transistor and a load transistor. One of the control transistors is controlled by an input logic signal DATA, and the other is controlled by the inverse logic signal/DATA.

[0007] When the core supply voltage disappears, the two logic voltages DATA and /DATA fall to zero. The two control transistors are then off. The voltage at an output of the translator becomes uncontrollable and dependent on the leakage currents in the transistors of the translator, or on a contradiction between two logic signals.

[0008] There may then be unnecessary consumption in the interface circuit, related to an untimely operation of a part of the interface circuits. It would be desirable to detect these situations in order to force the output signals of the translators, and therefore the internal control signals and the output signals of the interface circuits, into a defined state.

In particular, the most reliable state for the output signals in a core power-off situation is the high impedance state.

[0009] A voltage detection device meeting these requirements must furthermore be adapted to various external constraints. The interface supply voltage may indeed have a different level depending on the application. For example, it may be 2.3 volts to 3.6 volts for interfaces covering typical supply voltages of 2.5 volts and 3.5 volts.

[0010] The detector must work properly throughout this range of voltage. Furthermore, it should not consume power in the stable states. A classic detector typically comprises an inverter stage controlled by the core supply voltage and powered by the interface supply voltage by a diode or series of diodes.

[0011] If, in a given application, the interface supply voltage is within the lower limit, 2.3 volts in the example, there will not be enough voltage to properly power the inverter stage because of the drop in voltage in the diodes. If, in a given application, the interface supply voltage is within the higher limit, 2.6 volts in the example, there will be, on the contrary, excessive voltage so that the inverter will consume power all the time.

### SUMMARY OF THE INVENTION

[0012] In view of the foregoing background, an object of the present invention is to provide a voltage detector that detects unnecessary consumption in the interface circuit while meeting the above described constraints.

[0013] The invention therefore relates to a device for the detection of the level of the core supply voltage of an integrated circuit with respect to the level of an interface power supply voltage at a higher nominal level, applied as a power supply voltage to interface circuits of the integrated circuit. For the transmission of input/output signals, the detection device gives a detection signal applied to the interface circuits to set their output in a state of high impedance and minimize their power consumption when the level of the core supply voltage is far too low to enable operation of the integrated circuit.

[0014] According to one aspect of the invention, this voltage detection device comprises an input stage comprising an inverter controlled by the core voltage. The input stage is powered with the interface power supply voltage by a power supply stage comprising a diode or series of diodes and a capacitor.

[0015] In one variation, the capacitor is formed by a P-type MOS transistor that is series-connected between the diode or series of diodes and the inverter of the input stage. Its gate is then connected to ground and its substrate electrode or well is connected to the interface supply voltage. Its drain and source may also be connected together.

[0016] In another alternative embodiment, the detection device furthermore comprises a buffer type output stage comprising an inverter directly powered by the interface power supply voltage and a pull-down transistor for pulling the output node of the inverter of the input stage, controlled by the signal delivered by the output stage, to the interface power supply voltage.

[0017] In another alternative embodiment, the detection device comprises a current loop with gain greater than 1



associated with the input stage, and an output stage is connected between the interface power supply voltage and ground. A first transistor copies the current of the loop, and a second transistor that is controlled by the core supply voltage is series-connected with the first transistor. The detection signal is given by the intermediate connection node between the first and second transistors. This output signal of the detection device is applied to the input/output interface circuits of the integrated circuit, powered by the interface supply voltage Vdd3, to set them in a high impedance state and minimize their consumption.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Other features and advantages of the invention are described in detail in the following description, given by way of an indication that in no way restricts the scope of the invention, with reference to the appended drawings of which:

[0019] FIGS. 1a and 1b show the basic structure of a power supply detection device according to the present invention;

[0020] FIG. 2 shows a first alternative embodiment of the detection device according to the present invention;

[0021] FIG. 3 shows a second alternative embodiment of the detection device according to the present invention;

[0022] FIG. 4 shows an exemplary embodiment of an input/output interface circuit of an integrated circuit with a core supply voltage and an interface supply voltage according to the present invention;

[0023] FIG. 5 shows an exemplary application of a detection signal to an interface circuit according to the present invention; and

[0024] FIG. 6 gives a schematic view of an integrated circuit comprising a detection device according to the present invention to set, if necessary, the circuits in a state of high impedance and minimize their power consumption.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] FIG. 1a shows a power supply detection device 1 according to the invention. This circuit outputs a detection signal CORE-OFF whose active level indicates that a core power-off situation has been detected. It may be recalled that the core power-off situation according to the invention occurs as a result of either of the following two situations. It may occur when the integrated circuit is powered on from a core supply voltage Vdd whose voltage buildup is far slower than that of the interface supply voltage Vdd3. It may also occur during the functional operation of the integrated circuit, through the disappearance of the core supply voltage Vdd, i.e., a drop in the core supply source.

[0026] A detection system according to the invention can be used to detect these power-off situations. According to the invention, this device generates a detection signal when the level of the core supply voltage is far too low to enable the operation of the integrated circuit. An exemplary embodiment of a device of this kind according to the invention is shown in FIG. 1a. It comprises an input stage E1 comprising an inverter controlled at input IN by the core supply voltage. The inverter of the input stage is typically a CMOS inverter

comprising, in the example, a PMOS transistor M4 and an NMOS transistor M5. This input stage is powered with the interface power supply voltage Vdd3, by a power supply stage E2 comprising a diode or a series of diodes (in the example, two diodes D1 and D2), and the capacitor C1.

[0027] As shown in the FIG. 1b, the diodes may be made out of MOS transistors whose gate and drain are short-circuited. In the example, the first diode D1 is connected to the interface power supply voltage, and is formed by a PMOS transistor M2. The second diode D2 is connected between the first diode and the capacitor C1, and is formed by an NMOS transistor M3. The capacitor C1 (FIG. 1a) has one of its terminals connected to the interface supply voltage Vdd. The other terminal is connected to the connection point between the diode D2 and the input of the inverter E1. The capacitor C1 makes it possible to switch the inverter of the input stage for low interface supply voltages, such as for voltages of 2.3 V, for example.

[0028] The transistors M2 and M3, which are diode configured, are sized so that the current that flows through them during normal operation remains low as compared with the power consumption of the rest of the integrated circuit, regardless of the conditions of the temperature and the interface power supply voltage. With a setting of this kind, in the power-off situations and when there is a low power supply voltage, the current that flows across the transistors M2 and M3 is also very low, which is in the range of only a few tens of pico-amperes ( $10^{-12}$  amperes). This current is far too low to power the inverter E1 and build up its voltage at output. The capacitor C1 is used to overcome this problem of detection at low interface supply voltages.

[0029] During normal operation, the low current that flows across the transistors M2 and M3 is stored in the form of electrical charges in the capacitor. If the core supply voltage drops, the transistor M4 becomes conductive, and the capacitor C1 is discharged through this transistor M4 towards the output of the inverter E1, and causes the voltage to build up at the output of the inverter.

[0030] In the other power-off situation, when the interface power supply voltage increases faster than the core power supply voltage, the capacitor C1 creates a capacitive coupling between the interface power supply voltage and the source of the transistor M4. This enables the transistor M4 to be placed in a conductive state and enables the transmission of the charges through this transistor M4 to the output of the inverter.

[0031] FIG. 1b shows a preferred embodiment of the capacitor C1. In this embodiment, the capacitor C1 is formed by a P-type MOS transistor M1, whose gate is grounded. The drain and source of this transistor are connected to each other at the connection point between the diode D2 (or a series of diodes D1, D2) and the inverter of the input stage E1.

[0032] The substrate or well electrode of this transistor M1 is connected to the interface supply voltage Vdd3. One variation (not shown) may be obtained by removing the drain-source link of the transistor M1. Since the gate of this transistor is biased to ground, the drain and source electrodes are already connected to each other by the transistor itself, since it is conductive. In this case, the source of the transistor M1 is connected to the diode D2 (or a series of diodes) and

the drain of the transistor M1 is connected to the transistor M4 of the inverter of the input stage E1.

[0033] In a capacitor C1 formed by a transistor M1 of this kind, it is the parasitic source-substrate and drain-substrate capacitors that are used. This embodiment using a transistor-capacitor M1 is advantageous because it makes use of the inverse source-substrate diode current and drain-substrate diode current of this transistor which are added to the current that flows across the series of diodes D1, D2 (M2, M3), thus favoring the charging of this transistor-capacitor M1.

[0034] The capacitor C1 may be made with an N-type MOS transistor configured as a classic capacitor, whose gate would be connected to the interface power supply voltage Vdd3 and whose substrate electrode or well, drain and source would be connected together to the connection point between the diode D2 and the inverter of the input stage E1. However, in this case, no benefit will be derived from the inverse diode currents. A detection device of this kind can therefore be used for the efficient detection of the power-off situations in which the logic signals of the core of the integrated circuit no longer have any meaning.

[0035] FIG. 2 shows an alternative embodiment of a detection device according to the invention. With the detection device shown in FIG. 1a, a detection signal CORE-OFF is obtained at output Nin of the inverter. The two levels of this signal corresponding to the logic states 0 and 1 are 0 and Vdd3-2V<sub>tm</sub>, where V<sub>t</sub> represents a threshold voltage of the MOS transistor.

[0036] This detection circuit is to be applied to interface circuits powered by the interface supply voltage Vdd3. In particular, if it is sought to turn off a P-type MOS transistor in a reliable way, the full level of the supply voltage Vdd3 must be applied to its gate. The voltage level corresponding to the logic state 1 given by the detection device described with reference to FIG. 1a does not meet this condition.

[0037] The detection device shown in FIG. 2 thus comprises an output stage E3 following the input stage E1, to obtain the desired output levels for the inverse detection signal C<sub>ORE-OFF<sub>th</sub></sub>. This output stage E3 comprises an inverter IV directly powered by the interface supply voltage Vdd3, and a pull-down transistor M6 for pulling the output node Nin of the inverter of the input stage to the interface power supply voltage Vdd3. This pull-down transistor M6 is typically a P-type MOS transistor, controlled at its gate by the inverse detection signal C<sub>ORE-OFF<sub>th</sub></sub> given by the inverter IV of the output stage E3. This positive pull-down transistor M6 enables the proper stabilizing of the detection device. It maintains the node Nin at Vdd3, by feedback.

[0038] With the output stage E3, a hysteresis detection is obtained with a low threshold of switching from a state of the presence of a core power supply to a state of the absence of a core power supply, and a high threshold of switching of the detection circuit from a state of absence of the core supply to a state of presence of the core supply. In particular, if the output node Nin of the input stage is at Vdd3, then the signal IN applied to its input rises sufficiently to force the output node Nin downwards, and consequently, cut off the pull-down transistor M6. In a practical example, for integrated circuits using 0.18 μ technology with a core supply voltage of 1.8 volts, the high threshold may thus be equal to 0.98 volts and the low threshold may be equal to 0.33 volts.

[0039] FIG. 3 shows another alternative embodiment of a detection device according to the invention. This variation can be used to give not only the desired voltage level at the output, namely 0 and Vdd3, but also a satisfactory operation of the detection device, while the difference between the minimum and maximum interface supply voltages is greater than the nominal level of the core supply voltage Vdd itself.

[0040] This is what happens especially with integrated circuits using 0.12 μ technology, with a core supply voltage that can drop to 0.9 volts, in applications requiring a wide range of operation with respect to the interface power supply voltage, such as 2.3 volts to 3.6 volts, for example. In this case, the detection of the power-off situation cannot rely on a detection of an increase in the difference between the core supply voltage and the interface supply voltage, since this voltage difference may be greater in certain cases of normal operation than in power-off situations.

[0041] In this alternative embodiment, the detection circuit comprises, in addition to the input stage E1 and its power supply stage E2, a current loop BCP with gain greater than 1 associated with the input stage. An output stage E4 comprising a transistor M11 for copying the current in the loop is connected to the interface supply voltage, and a transistor M12 is directly controlled by the core supply voltage, and is connected to ground.

[0042] In the exemplary embodiment shown in FIG. 3, the current loop associated with the input stage comprises two current mirror structures 2 and 3. The first current mirror structure comprises a MOS transistor M7 configured as a diode (with the gate and drain connected), and is connected between the output node Nin of the input stage E1 and ground. A second MOS transistor M8, has its gate connected to the gate of the transistor M7, namely therefore to the node Nin.

[0043] The second current mirror structure 3 comprises a first MOS transistor M9 configured as a diode (with gate and drain connected), and a second MOS transistor M10 connected between the interface power supply voltage Vdd3 and the power supply stage E2. The transistor M9 is series connected with the transistor M8, between the interface power supply voltage Vdd3 and ground. The transistor M9 has its gate connected to the gate of the second transistor M10. The sizes of the transistors of the structures 2 and 3 of the loop are determined so that they have a gain greater than 1. They are determined by the usual methods.

[0044] The output stage E4 comprises the transistors M11 and M12 series connected between the interface power supply voltage Vdd3 and ground. The first MOS transistor M11 is connected between the interface power supply voltage Vdd3 and the output node Ns which gives the detection signal C<sub>ORE-OFF</sub>. It has its gate controlled by the gate of the transistor M9 with which it forms a current mirror. Thus, the current of the loop is copied by the transistor M11. The second MOS transistor M12 is connected between the node Ns and ground. It has its gate controlled by the core power supply voltage Vdd.

[0045] With a detection device of this kind, if the core power supply voltage is at its nominal value, 1.2 volts in the example, the transistor M5 of the input stage E1 is on and the output node Nin is pulled to ground. No current flows in the loop BCP. Furthermore, the transistor M12 of the output

stage E4 is conductive and pulls the node Ns of the stage to ground. The current in the stages E1 and E2 is then cut off by the transistor M10.

[0046] If the core power supply voltage Vdd drops to zero, the transistors M5 and M12 are off. The current loop is active and the transistor M11 of the output stage E4 copies the loop current. The node NS (CORE-OFF) is pulled to the interface power supply voltage Vdd3.

[0047] With a detection device of this kind, the detection is effective even for very nominal values of the power supply voltage that are very low when compared with the interface power supply voltage. Furthermore, when the power supply voltages are at their nominal values, this device does not show any consumption (current loop off), and this is advantageous.

[0048] FIG. 4 shows an exemplary interface circuit for the transmission of a piece of data at output, to which it is possible to apply a detection signal according to the invention. This interface circuit comprises a buffer type output stage 4. An output stage of this kind is generally a stage with N-type and P-type transistors. It is connected between the interface power supply voltage Vdd3 and ground. This output stage is to be controlled by level signals defined with respect to this interface voltage.

[0049] Thus, a level translator, referenced 5 and 6 in the figure, provides the control signal for each of the transistors of the output stage, from a logic signal DATA, namely the piece of data to be transmitted, coming from the core of the integrated circuit. Each translator (references 5 and 6) is usually followed by an inverter (references 7 and 8) powered by the interface power supply voltage Vdd3, so as to preserve the same polarity.

[0050] In an interface circuit of this kind it is important to prevent the transmission of the logic signal DATA at the output in power-off situations of the core supply voltage Vdd as defined in the invention. It is therefore necessary to set the output of the interface circuit, namely the output of the buffer, in a high impedance state.

[0051] It is also necessary to prevent unnecessary consumption in translators crossed by internal control signals of the interface circuit. For this purpose, in power-off situations defined in the invention, it is enough to set the output of the translators of the interface circuit in an appropriate state. Setting the output of the translators in a determined logic state that is independent of the signal to be transmitted, and such that the two transistors of the buffer are set in the off state provides an answer to the different problems of control of the interface circuits.

[0052] FIG. 5 shows a level translator in which there are provided means controlled by a detection device 1 according to the invention. These means are used, in a power-off situation, to set its output in a determined state, independent of the logic signal DATA applied at input. Thus, in addition to the usual two-arm structure B1 and B2 of the translator, an additional transistor is provided on each arm.

[0053] A first transistor M13 is connected between the interface power supply voltage Vdd3 and an output node N1 of an arm B1, and a second transistor M14 is connected between the output node of the other arm B2 and ground. In the example, the transistor M13 is a P-type MOS transistor

and the transistor M14 is an N-type MOS transistor. Of these two transistors, the first one is controlled by the inverse detection signal  $C_{\text{CORE-OFFn}}$  and the second one is controlled by the detection signal  $C_{\text{CORE-OFF}}$ .

[0054] When the detection signal CORE-OFF goes to the active state, Vdd3 in the example, the transistor M13 sets the output node N1 of the associated arm at Vdd3 while the transistor M14 pulls the output node N2 of the other arm to zero. If it is sought to pull the nodes N1 and N2 to 0 and Vdd3 respectively, it will be enough to reverse the roles of the transistors M13 and M14.

[0055] With a detection device according to the invention, it is thus possible to control the interface circuit in a sure way so that operation of the integrated circuits in their applications environment is made more dependable. FIG. 6 gives a schematic view of an integrated circuit comprising a detection device 1 according to the invention. This detection device gives a detection signal CORE-OFF applied to the interface circuits 9 powered by the interface power supply voltage Vdd3 to set them, in the power-off situation, in a state of high impedance.

That which is claimed is:

1. A device for the detection of the level of the core supply voltage of an integrated circuit with respect to the level of an interface power supply voltage at a higher nominal level, applied as a power supply voltage to interface circuits of said integrated circuit, for the transmission of input/output signals, said detection device giving a detection signal applied to said interface circuits to set their output in a state of high impedance and minimize their power consumption when the level of the core supply voltage is far too low to enable the working of the integrated circuit, said detection corresponding to a power-off situation of the core power supply.

2. A detection device according to claim 1, comprising an input stage comprising an inverter controlled by the core supply voltage, said input stage being powered with the interface power supply voltage by a power supply stage comprising a diode or series of diodes and a capacitor, these diodes being series-connected between said interface power supply voltage and the input stage and said capacitor having an electrode connected to the input stage, the other electrode being directly connected to the interface supply voltage.

3. A detection device according to claim 2, wherein the capacitor is formed by a P type MOS transistor, series-connected between the diode or series of diodes and the inverter of the input stage, said transistor having its gate connected to the ground and its substrate electrode or well connected to the interface supply voltage.

4. A detection device according to claim 3, wherein said MOS transistor has its drain and its source connected together.

5. A detection device according to one of the claims 2 to 4, furthermore comprising a latch type output stage, comprising an inverter controlled by the output of the input stage and directly powered by the interface power supply voltage and a pull-down transistor connected between said interface supply voltage and said output of the input stage, said pull-down transistor being controlled by the signal delivered by said inverter.

6. A detection device according to one of the claims 2 to 4, comprising a current loop with positive gain associated with the input stage and an output stage comprising a first transistor to copy the current of the loop, series-connected

with a second translator controlled by the core supply voltage, said first and second transistors being series-connected between the interface supply voltage and the ground, the detection signal being given by the intermediate connection node between said first and second transistors.

7. A low-voltage MOS technology integrated circuit comprising a detection device according to any of the claims 1 to 6, to set input/output interface circuits, powered by the interface supply voltage, in high impedance and minimize their consumption in the core supply power-off situations.

8. An integrated circuit according to claim 7, an interface circuit comprising at least one level translator powered by the interface supply voltage and associated with a buffer type data output stage, said translator being used to adapt the level of a logic signal coming from the core of the integrated circuit, wherein said translator receives a control signal

given by said detection device to set an output of said level translator in a state determined independently of the logic signal applied at input; to set the associated output stage in a state of high impedance, in the core supply power-off situations.

9. An integrated circuit according to claim 8, said translator comprising two arms connected between the interface supply voltage and the ground, each arm giving an output node, the integrated circuit furthermore comprising a first transistor connected between the interface power supply voltage and the output node of an arm of the translator and a second transistor connected between the output node of the other arm of the translator and the ground, to set each of said nodes in a determined state.

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