

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Chang Ki Kwon *et al.*  
U.S. Patent No.: 8,063,674  
Issue Date: November 22, 2011  
Appl. Serial No.: 12/365,559  
Filing Date: February 4, 2009  
Title: Multiple supply-voltage power-up/down detectors

### DECLARATION OF ROBERT W. HORST, PH.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

#### **I. Qualifications and Background Information**

1. I am currently an Adjunct Research Professor in the Department of Electrical and Computer Engineering the University of Illinois at Urbana-Champaign and am also an independent consultant at HT Consulting. I am an independent consultant with more than 30 years of expertise in the design and architecture of computer systems. I have testified as an expert witness and consultant in patent and intellectual property litigation as well as *inter partes* reviews and re-examination proceedings. My curriculum vitae is provided as APPLE-1004.

2. I earned my M.S. (1978) in electrical engineering and Ph.D. (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master's program, I designed, constructed and debugged a shared memory parallel

microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded task flow computer.

3. After receiving my bachelor's degree and while pursuing my master's degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to 1999, I worked at Tandem Computers, which was acquired by Compaq Computers in 1997. While at Tandem, I was a designer and architect of several generations of fault-tolerant computer systems and was the principal architect of the NonStop Cyclone superscalar processor. The system development work at Tandem also included development of the ServerNet System Area Network and applications of this network to fault tolerant systems and clusters of database servers.

4. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware, Network Appliance, Tibion, and AlterG in the areas of network-attached storage and biomedical devices. From 2012 to 2015, I was Chief Technology Officer of Robotics at AlterG, Inc., where I worked on the design of anti-gravity treadmills and battery-powered orthotic devices to assist those with impaired mobility.

5. In 2001, I was elected an IEEE Fellow "for contributions to the architecture and design of fault tolerant systems and networks." I have authored over

30 publications, have worked with patent attorneys on numerous patent applications, and I am a named inventor on 82 issued U.S. patents.

6. My patents include those directed to computer systems with multiple supply voltages including U.S. Pat. No. 6,496,940 (Multiple processor system with standby sparing) and U.S. Pat. No. 5,193,175 (Fault-tolerant computer with three independently clocked processors asynchronously executing identical code that are synchronized upon each voted access to two memory modules). My patents also include aspects of circuit design including U.S. Pat. No 5,034,964 (N:1 time-voltage matrix encoded I/O transmission system) and U.S. Pat. No. 9,893,604 (Circuit with low DC bias storage capacitors for high density power conversion).

7. In writing this Declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of computer systems and circuit design and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent No. 8,063,674 (APPLE-1001), and its accompanying prosecution history (APPLE-1002)
- U.S. Patent No. 7,279,943 to Ulrich Steinaker (“Steinaker”) (APPLE-1005)
- U. S. Patent No. 4,717,836 to James Doyle (“Doyle”) (APPLE-1006)

- J. C. Park and V. J. Mooney III, “Sleepy Stack Leakage Reduction,” 14 IEEE Transactions on Very Large Scale Integration (VLSI) Systems 11, pp. 1250-1263 (Nov. 2006) (“Park”) (APPLE-1007)
- U.S. Patent Application No. 2002/0163364 to Sylvain Majcherczak (“Majcherczak”) (APPLE-1008)
- U.S. Patent No. 6,646,844 to Lloyd P. Matthews (“Matthews”) (APPLE-1009)
- G. W. Griffiths, “A Review of Semiconductor Packaging and Its Role in Electronics Manufacturing,” 8th IEEE/CHMT International Conference on Electronic Manufacturing Technology Symposium (1990) (APPLE-1010)
- Wang-Chang Albert Gu, “RF Front-End Modules in Cellular Handsets,” 2004 IEEE Compound Semiconductor Integrated Circuit Symposium (Feb. 2005) (APPLE-1011)
- Roy, K, S Mukhopadhyay, and H Mahmoodi Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,” 91 Proceedings of the IEEE 2, pp. 305-327 (Apr. 2003) (“Roy”) (APPLE-1012)
- Y. Ye, S. Borkar and V. De, “A new technique for standby leakage reduction in high-performance circuits,” 1998 Symposium on VLSI

Circuits. Digest of Technical Papers (Cat. No.98CH36215), Honolulu, HI, USA, 1998, pp. 40-41 (“Borkar”) (APPLE-1013)

- U.S. Patent No. 7,049,865 to Parker *et al.* (“Parker”) (APPLE-1014)
- Qadeer A. Khan *et al.*, “A Sequence Independent Power-on-Reset Circuit for Multi-Voltage Systems,” 2006 IEEE International Symposium on Circuits and Systems (Sep. 2006) (APPLE-1015)

## **II. Legal Principles**

8. In forming my opinions expressed in this declaration, I have applied the legal principles described in the following paragraphs.

### **A. Legal Standards for Prior Art**

9. I am not an attorney. My understanding of the legal standards throughout this section are based on discussion with Counsel and my experience in prior patent cases.

10. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

11. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the effective filing date of the asserted patent. I further understand from Counsel that a printed publication, such as an article published in a journal, magazine, or trade publication, qualifies

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