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Paper 26
Date: January 3, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01315
IPR2018-01316
Patent 8,063,674 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

INTRODUCTION

In these *inter* partes reviews, instituted pursuant to 35 U.S.C. § 314, Apple Inc. ("Petitioner") challenges claims 1, 2, 5–9, 12, 13, and 16–22 ("the challenged claims") of U.S. Patent No. 8,063,674 B2 (Ex. 1001, "the '674 patent"), owned by Qualcomm Incorporated ("Patent Owner").

As explained in detail below, the references applied against the challenged claims are identical in each of the cases. A joint hearing was held for these cases. The parties rely on the same declarants submitting identical declarations in each case for testimonial evidence. Under these circumstances, we determine that a combined Final Decision will promote a just, speedy, and inexpensive resolution of these proceedings.

The Board has jurisdiction under 35 U.S.C. § 6(b). This Final Written Decision issues pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

A. IPR2018-01315 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 1, 2, and 5–7 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. Paper 2[1] ("Petition" or "Pet."). Patent Owner filed a Preliminary Response. Paper 6. We instituted an *inter partes* review of claims 1, 2, and 5–7 on all grounds of unpatentability alleged in the Petition. Paper 7 ("Institution Decision" or "Inst. Dec.").

[1] Unless otherwise noted, all citations are to IPR2018-01315. We note that identical exhibits were filed in each of the proceedings.

After institution of trial, Patent Owner filed a Response (Paper 12, "PO Resp."), Petitioner filed a Reply (Paper 16, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 19, "PO Sur-reply").

A joint hearing for IPR2018-01315 and IPR2018-01316 was held on October 11, 2019. Paper 25 ("Tr.").

B. IPR2018-01316 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 8, 9, 12, 13, and 16–22 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. IPR2018-01316, Paper 2 ("1316 Pet."). Patent Owner filed a Patent Owner Preliminary Response. IPR2018-01316, Paper 6. We instituted an *inter partes* review of claims 8, 9, 12, 13, and 16–22 on all grounds of unpatentability alleged in the Petition. IPR2018-01318, Paper 7 ("1316 Inst. Dec.").

After institution of trial, Patent Owner filed a Response (IPR2018-01316, Paper 12, "1316 PO Resp."), Petitioner filed a Reply (IPR2018-01316, Paper 16, "1316 Pet. Reply"), and Patent Owner filed a Sur-reply (IPR2018-01316, Paper 19, "1316 PO Sur-reply").

A joint hearing for IPR2018-01315 and IPR2018-01316 was held on October 11, 2019. IPR2018-01316, Paper 25 ("Tr.").

C. Real Party in Interest

Petitioner identified Apple, Inc. as the real party in interest. Pet. 64.

Patent Owner identified Qualcomm Incorporated as the real party in interest. Patent Owner's Mandatory Notices, Paper 3, 2; IPR2018-01315 Patent Owner's Mandatory Notices, Paper 3, 2.

D. Related Proceedings

The parties identified the following patent litigation proceedings in which the '674 patent was asserted: *In re Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof* (ITC Inv. No. 337-TA-1093) and *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-02398 (S.D. Cal.). *Id.* at 64–65; Patent Owner's Mandatory Notices, Paper 3, 2.[2]

E. The '674 Patent

The '674 patent is titled "Multiple Supply-Voltage Power-Up/Down Detectors." Ex. 1001, code (54). According to the '674 patent, "many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices." *Id.* at 1:22–25.

The '674 patent further states that "[i]n order to facilitate communication between the core and I/O devices, level shifters are employed." *Id.* at 1:28–29. "Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down." *Id.* at 1:29–32. An example of such a problem described in the '674 patent is how stray currents while the core is powering down can cause the level shifters to "send a signal to the I/O devices for transmission" resulting in the I/O devices "transmit[ting] the erroneous signal into the external environment." *Id.* at 1:34–40.

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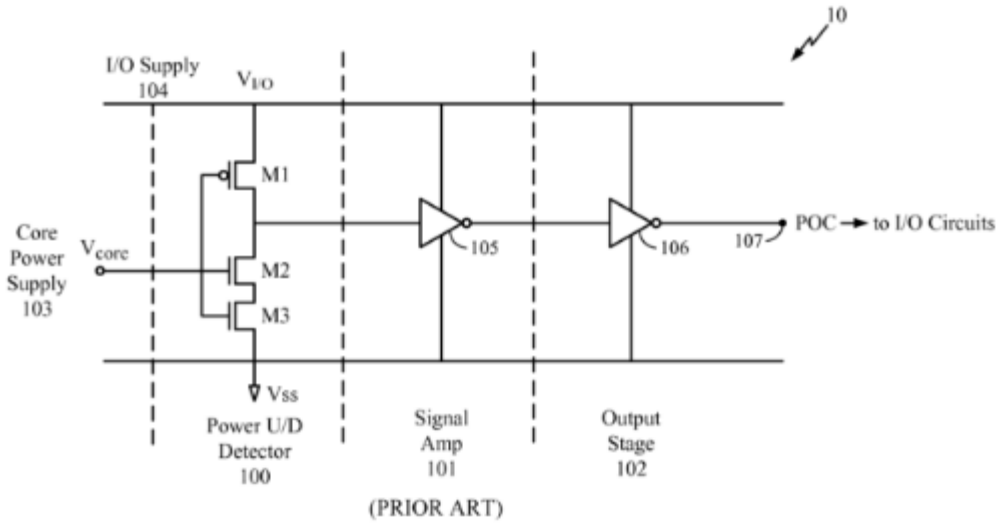
[2] According to Petitioner, the district court proceeding and the ITC investigation have been dismissed. Petitioner's Updated Mandatory Notices, Paper 15, 1.

One prior art solution identified in the '674 patent is the use of "power-up/down detectors to generate a power-on/off-control (POC) signal internally [which] instructs the I/O devices when the core devices are shut down." Ex. 1001, 1:55–58. Figure 1 of the '674 patent is reproduced below.



(PRIOR ART)
FIG. 1

Figure 1 "is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" which is identified as being prior art. *Id*. at 4:18–19, Fig. 1.

The '674 patent identifies a number of issues associated with the Figure 1 design. For example, when I/O power supply 104 is on and core power supply 103 is off, powering on the core power supply results in "a period in which all three transistors within power up/down detector 100 are on," resulting in a virtual short "to ground causing a significant amount of current to flow from I/O power supply 104 to ground." Ex. 1001, 2:21–29. "This 'glitch' current consumes unnecessary power." *Id*. at 2:29–30. Although the glitch current can be reduced by reducing the size of transistors M1-M3, such a reduction limits "the actual amount of current that can pass through the transistors" and reduces their switching speeds, which

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