UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01315
Patent 8,063,674

PRELIMINARY PATENT OWNER RESPONSE TO PETITION FOR INTER PARTES REVIEW PURSUANT TO 37 C.F.R. § 42.107

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I. INTRODUCTION

Apple Inc. ("Apple" or "Petitioner") seeks review of claims 1, 2, and 5-7 of U.S. Patent No. 8,063,674 (the "'674 Patent") based on obviousness grounds.[1] In determining whether to institute *inter partes* review, the Board must resolve whether a person of ordinary skill in the art (POSA) would have found it obvious to combine prior-art elements in the manner proposed by Apple. For this inquiry, the Federal Circuit has cautioned that "[t]he inventor's own path itself never leads to a conclusion of obviousness; that is hindsight." *Otsuka Pharm. Co. v. Sandoz, Inc.*, 678 F.3d 1280, 1296 (Fed. Cir. 2012). Thus, it is improper to rely on the patent itself as a roadmap for combining prior-art elements "like separate pieces of a simple jigsaw puzzle." *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1349 (Fed. Cir. 2014).

Yet that is exactly what Apple does in its Petition. In Ground 1, Apple asserts that the challenged claims are obvious over the combination of Steinacker, Doyle, and Park. But the POSA would *never* consider implementing the voltage level detector of Steinacker's analog/digital mixed signal circuit with the interface circuit of Doyle, as Apple proposes. Doyle's circuit is designed to provide an interface between a TTL circuit and a CMOS circuit. The design and purpose of Doyle's

[1] Apple seeks review of claims 8, 9, 12, 13 and 16-22 of the '674 Patent over the same combination of references in IPR2018-01316.

TTL/CMOS interface circuit is entirely unrelated to the analog/digital mixed signal circuit of Steinacker, and the POSA would not combine the circuits absent a desire to recreate the circuits disclosed in the '674 Patent. Likewise, the POSA would not combine Park with the hypothetical Steinacker/Doyle circuit to reduce leakage current (Petition at 22) because neither Steinacker nor Doyle recognizes any problem relating to leakage power consumption. Only impermissible hindsight would lead one to make this combination.

Apple's Grounds 2a and 2b based on the alleged AAPA and Majcherczak are also deficient. These grounds are nothing more than a rehash of art that the Office already considered during prosecution, and the Board should deny them on this basis alone.

Because Apple's petition fails to establish a reasonable likelihood of prevailing on any claim, the Board should decline to institute trial on the '674 Patent.

II. THE '674 PATENT AND ITS PROSECUTION HISTORY

A. Overview of the '674 Patent

U.S. Patent No. 8,068,674 ("the '674 Patent"), titled "Multiple Supply-Voltage Power-Up/Down Detectors," generally relates to power-up/down detectors. The '674 Patent issued on November 22, 2011, from an application filed on February 4, 2009.

Modern integrated circuits include multiple networks operating with different supply voltages (*e.g.*, V1 and V2). For example, a lower voltage V1 may be used for a core logic network, while a higher voltage V2 may be used for an input/output ("I/O") network. Multiple independent supply voltages provide flexibility in operating different networks independently, such as being able to turn off parts of the circuit that are not needed (*e.g.*, sleep mode), which results in significant power savings. Also, because new integrated circuit devices often interface with older technology, "input/output (I/O) circuits within the integrated circuit have remained at higher operating voltages to interface with the higher voltage requirements of these older systems." Ex. 1001 ('674 Patent) at 1:22-25.

The Background section of the '674 Patent recognizes that many previous power up/down detectors suffered from problems. For example, the '674 Patent explains:

> Core devices and applications communicate with operations outside of the integrated component through the I/O devices. In order to facilitate communication between the core and I/O devices, level shifters are employed. Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down. Powering down or power collapsing is a common technique used to save power when no device operations are pending or in progress. For example, if the core network is power collapsed, it is possible that the lever shifters, whether through stray

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