DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

CLASS sites

ENEE 359A: Digital VLSI Circuits by B. Jacob

Spring 2007

Course Information:

Lecture:	Tue Thu 2:00 - 3:15, EGR-3114
Mailing List:	*enee359a-0101-spring07@coursemail.umd.edu*
Required Text:	*Digital Integrated Circuits: A Design Perspective, 2nd Ed.*, by Rabaey, Chandrakasan, and Nikolic
Recommended Texts:	Dally & Poulton: *Digital Systems Engineering*
	Johnson & Graham: *High-Speed Digital Design*
	Uyemura: *Introduction to VLSI Circuits and Systems*
	Baker, Li, & Boyce: *CMOS: Circuit Design, Layout, and Simulation*

Instructor Information:

Professor:	Bruce L. Jacob, Associate Professor, Electrical & Computer Engineering
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Email:	*blj@ece.umd.edu*
Office Hours:	*Open door policy (for now ...)*

TA:	Elliott Cooper-Balis
Email:	ecc17@umd.edu
Recitations:	Tue 3:30 - 4:30pm, ???

Course Handouts and General Information:

- Syllabus.pdf
- A great Verilog tutorial on-line, and PDF of that same tutorial.
- verilog-handbook.pdf. This is a concise overview of the Verilog programming language.
- realize-verilog.pdf. Gives a functional view of Verilog; i.e. if you want to build a processor model, this shows how. However, it confuses blocking/non-blocking assignments (calls "=" non-blocking and "<=" blocking). Otherwise, it is a decent overview.
- scaling.gif. A **very** interesting picture illustrating the degree to which VLSI designs have reduced in size since the Intel 4004.
- 2007-midterm-solutions.pdf. Midterm exam, grade distribution, solutions.

Weeks 1/2	enee359a-overview.pdf	Ch. 1	*Course overview in a nutshell*
Weeks 2/3	enee359a-devices.pdf	Ch. 3.1-3.3.2, 5.1-5.3	*Intro to (Verilog) design, P/N junctions, MOS transistors, CMOS inverter*
Week 4	enee359a-CMOS.pdf	Ch. 6-6.2	*Static CMOS Design*
Week 5	enee359a-manufacturing.pdf		*Cadence tools & manufacturing processes*
Week 6	enee359a-sizing.pdf	Ch. 5.4-5.7	*Transistor Sizing & Logical Effort*
Week 7	enee359a-wires.pdf	Ch. 4	*Interconnects (i.e., wires)*
Week 8	**Review** and **Midterm**		
Week 9	*SPRING BREAK*		
Weeks 10/11	enee359a-sequential.pdf	Ch. 7	*Sequential Circuits: Latches, Registers, Pipelines*
Week 12	enee359a-parasitics.pdf	Ch. 9	*Capacitive, Resistive, and Inductive Parasitics*
Weeks 13/14	enee359a-timing.pdf	Ch. 10	*System Timing: Synchronous, Asynchronous, etc.*
Weeks 15	enee359a-SRAM-i.pdf	*not really in book*	*Low-Power SRAM Circuits*
Week 16	enee359a-DRAM-i.pdf enee359a-DRAM-ii.pdf	*not really in book*	*DRAM Systems & Circuits* ... pictures of cells

Assignments:

ID	Out	Due	Write-up	Homework Solution/Project Distribution
Project 1	01-Feb-2007	13-Feb-2007	p1.pdf	Project 1 Distribution
HW-1	15-Feb-2007	20-Feb-2007	hw1.pdf	
Project 2	20-Feb-2007	06-Mar-2007	p2.pdf	Project 2 Distribution
HW-2	20-Feb-2007	27-Feb-2007	hw2.pdf	
Project 3	01-Mar-2007	29-Mar-2007	p3.pdf	Project 3 Distribution
HW-3	09-Mar-2007	13-Mar-2007	hw3.pdf	
Project 4	12-Apr-2007	24-Apr-2007	p4.pdf	
HW-4	01-May-2007	10-May-2007	hw4.pdf	DFF-sim.pdf

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ENEE 359a
Digital VLSI Design

Transistor Sizing & Logical Effort

Prof. Bruce Jacob
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Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Dally's EE273 slides (Stanford), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).

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Overview

- **Sizing of transistors to balance performance of single inverter**
- **More on RC time constant, first-order approximation of time delays**
- **Sizing in complex gates, examples**
- **Sizing of inverter chains for driving high capacitance loads (off-chip wires)**

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Resistance

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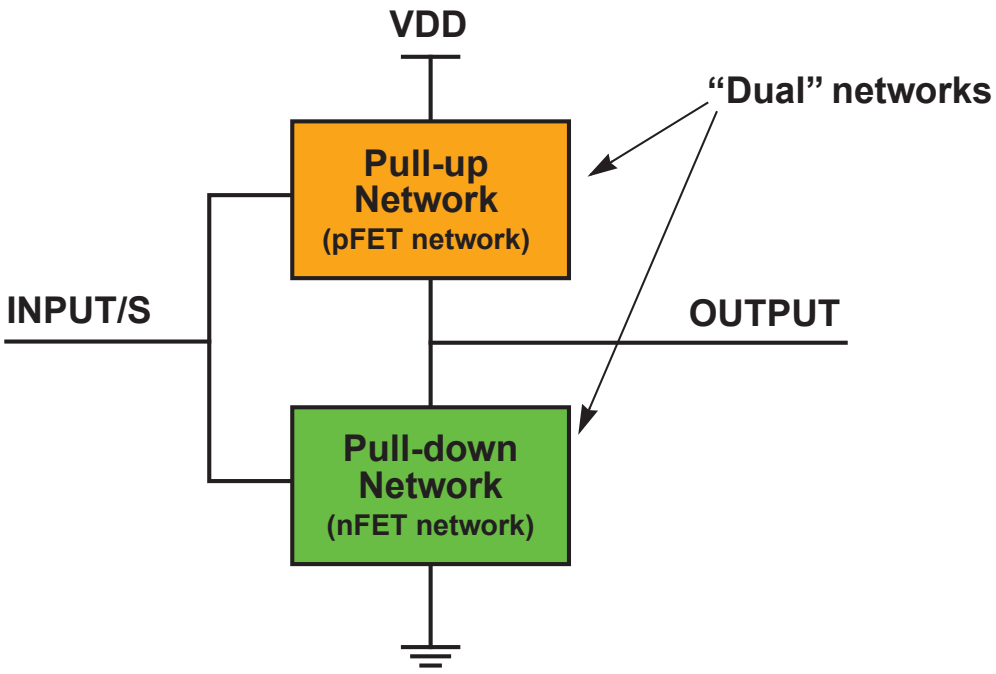

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