UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD
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APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

_____

Cases IPR2018-01315
Patent 8,063,674 B2

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Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I.	INTRODUCTION

Apple Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 1, 2, and 5–7 of U.S. Patent No. 8,063,674 B2 (Ex. 1001, "the '674 patent") pursuant to 35 U.S.C. §§ 311–319. Paper 2 ("Petition" or "Pet."). Qualcomm Incorporated ("Patent Owner") filed a Patent Owner Preliminary Response. Paper 6 ("Preliminary Response" or "Prelim. Resp.").

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless "the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

For the reasons set forth below, upon considering the Petition, Preliminary Response, and evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims. Accordingly, we institute *inter partes* review on all of the challenged claims based on the all of the grounds identified in the Petition.

A.	*Real Party-In-Interest*

Petitioner identifies Apple, Inc. as the real party-in-interest. Pet. 64.

B. Related Proceedings

The parties identify the following currently pending patent litigation proceedings in which the '674 patent is asserted: *In re Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof* (ITC Inv. No. 337-TA-1093) and *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-02398 (S.D. Cal.). *Id.* at 64–65; Paper 3, 2. Patent Owner identifies a second *inter partes* review for the '674 patent: *Apple Inc. v. Qualcomm Inc.*, Case IPR2018-01316. Paper 3, 2.

C. The '674 Patent

The '674 patent is titled "Multiple Supply-Voltage Power-Up/Down Detectors." Ex. 1001, [54]. According to the '674 patent, "many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices." *Id.* at 1:22–25.

The '674 patent further states that "[i]n order to facilitate communication between the core and I/O devices, level shifters are employed." *Id.* at 1:28–29. However, "[b]ecause the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down." *Id.* at 1:29–32. An example of such a problem described in the '674 patent is how stray currents while the core is powering down can cause the level shifters to "send a signal to the I/O devices for transmission" resulting in the I/O devices "transmit[ting] the erroneous signal into the external environment." *Id.* at 1:34–40.

One prior art solution identified in the '674 patent is the use of "power-up/down detectors to generate a power-on/off-control (POC) signal

internally [which] instructs the I/O devices when the core devices are shut down." *Id.* at 1:55–58. Figure 1 of the '674 patent is reproduced below.
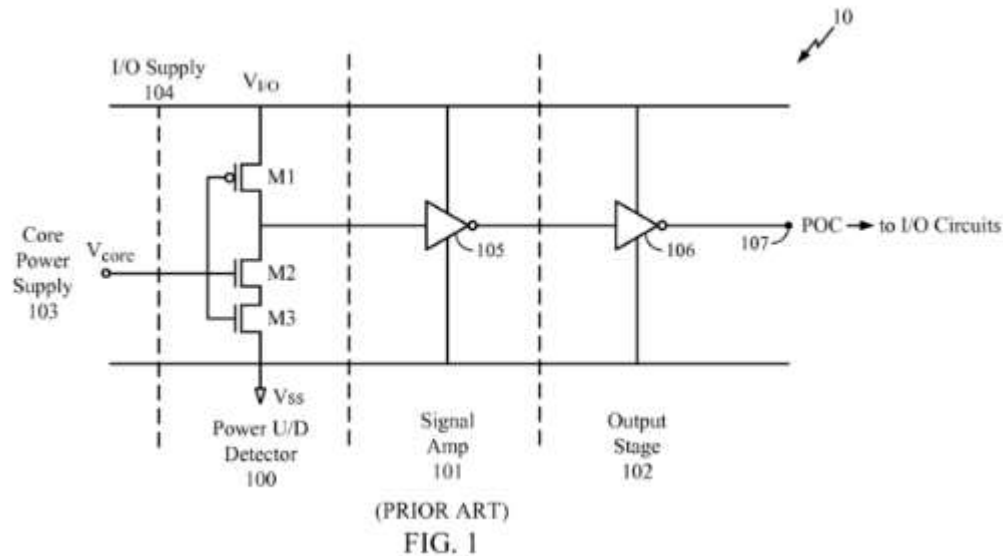

(PRIOR ART)
FIG. 1

Figure 1 "is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" which is identified as being prior art. *Id.* at 4:18–19, Fig. 1.

The '674 patent identifies a number of issues associated with the Figure 1 design. For example, when I/O power supply 104 is on and core power supply 103 is off, powering on the core power supply results in "a period in which all three transistors within power up/down detector 100 are on," resulting a virtual short "to ground causing a significant amount of current to flow from I/O power supply 104 to ground." *Id.* at 2:21–29. "This 'glitch' current consumes unnecessary power." *Id.* at 2:29–30. Although the glitch current can be reduced by reducing the size of transistors M1-M3, such a reduction limits "the actual amount of current that can pass through the transistors" and reduces their switching speeds, which "translates into less sensitivity in detecting power-up/down of core supply

voltage 103 or longer processing time for power-up/down events." *Id*. at 2:31–39; *see also id*. at 2:63–3:11.

According to the '674 patent, these problems can be solved by using "one or more feedback circuits coupled to the up/down detector" that "are configured to provide feedback signals to adjust a current capacity of said up/down detector." *Id*. at 3:31–34. An example of such a feedback circuit is shown in Figure 4, reproduced below:
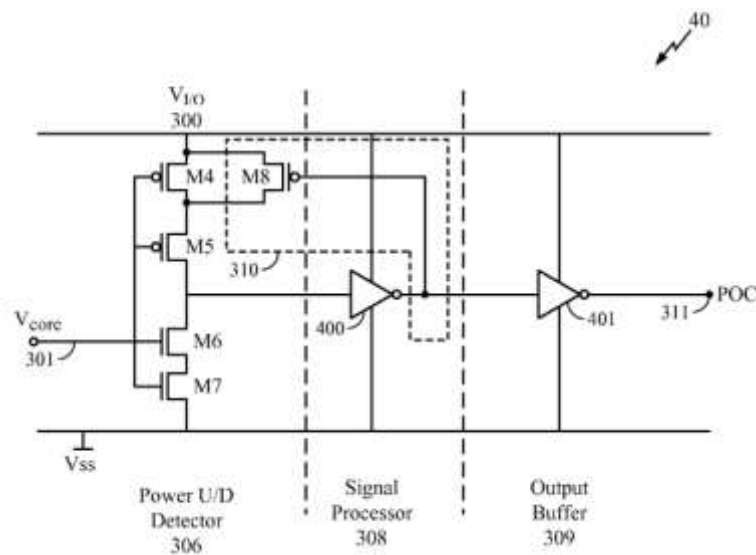

Figure 4 "is a circuit diagram illustrating another POC network configured according to the teachings of the present disclosure." *Id*. at 4:28–30. The '674 patent describes the operation of the feedback circuit in Figure 4 as follows:

> The feedback network 310 comprises a transistor M8 connected in parallel to the transistor M4. The transistor M8 is also configured as a p-type transistor, such that when the feedback signal from the inverting amplifier 400 is high, the transistor M8 is switched off, and when the feedback signal is low, the transistor M8 is switched on. Thus, when the V_{core} 301 is off, producing a high detection signal, the inverting amplifier 400 inverts that signal to a logic low which causes the transistor M8 to switch on. As the V_{core} 301 is powered-on, the detection

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