

**United States Court of Appeals
for the Federal Circuit**

QUALCOMM INCORPORATED,
Appellant

v.

APPLE INC.,
Appellee

**ANDREW HIRSHFELD, PERFORMING THE
FUNCTIONS AND DUTIES OF THE UNDER
SECRETARY OF COMMERCE FOR
INTELLECTUAL PROPERTY AND DIRECTOR OF
THE UNITED STATES PATENT AND TRADEMARK
OFFICE,**
Intervenor

2020-1558, 2020-1559

Appeals from the United States Patent and Trademark
Office, Patent Trial and Appeal Board in Nos. IPR2018-
01315, IPR2018-01316.

Decided: February 1, 2022

JENNIFER L. SWIZE, Jones Day, Washington, DC, ar-
gued for appellant. Also represented by ROBERT BREETZ,
DAVID B. COCHRAN, DAVID MICHAEL MAIORANA, JOSEPH M.
SAUER, Cleveland, OH; MATTHEW JOHNSON, JOSHUA R.

NIGHTINGALE, Pittsburgh, PA; ISRAEL SASHA MAYERGOYZ, Chicago, IL.

LAUREN ANN DEGNAN, Fish & Richardson PC, Washington, DC, argued for appellee. Also represented by MICHAEL JOHN BALLANCO, CHRISTOPHER DRYER; WHITNEY REICHEL, Boston, MA.

MAUREEN DONOVAN QUELER, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor. Also represented by THOMAS W. KRAUSE, ROBERT J. MCMANUS, FARHEENA YASMEEN RASHEED.

Before TARANTO, BRYSON, and CHEN, *Circuit Judges*.

CHEN, *Circuit Judge*.

Qualcomm Inc. (Qualcomm) appeals from two related *inter partes* review (IPR) decisions of the Patent Trial and Appeal Board (Board) finding several claims of Qualcomm's U.S. Patent No. 8,063,674 ('674 patent) unpatentable under 35 U.S.C. § 103.¹ To reach its unpatentability finding, the Board relied on a ground raised by Apple Inc. (Apple) that relied in part on applicant admitted prior art (AAPA)—here, statements in the challenged patent

¹ Congress amended §§ 102 and 103 when it passed the Leahy-Smith America Invents Act (AIA). Pub. L. No 112-29, §§ 3(b), 3(c), 125 Stat. 284, 287 (2011). Because the application that led to the '674 patent has never contained a claim having an effective filing date on or after March 16, 2013 (the effective date of the statutory changes enacted in 2011), or a reference under 35 U.S.C. §§ 120, 121, or 365(c) to any patent or patent application that ever contained such a claim, the pre-AIA §§ 102 and 103 apply. *Id.* § 3(n)(1), 125 Stat. at 293.

acknowledging that most of the limitations of the patent's claims were already known—and a prior art patent. Qualcomm argues the Board's reliance on AAPA runs afoul of 35 U.S.C. § 311(b), which limits an *inter partes* review petitioner to challenge claims as unpatentable “only on a ground that could be raised under section 102 or 103 and *only on the basis of prior art consisting of patents or printed publications.*” § 311(b) (emphasis added). Because we agree with Qualcomm that the Board erred in concluding that AAPA constitutes “prior art consisting of patents or printed publications” under § 311(b), we vacate the Board's decision. We remand for the Board to determine whether Apple's petition nonetheless raises its § 103 challenge “*on the basis of prior art consisting of patents or printed publications.*” § 311(b) (emphasis added).

BACKGROUND

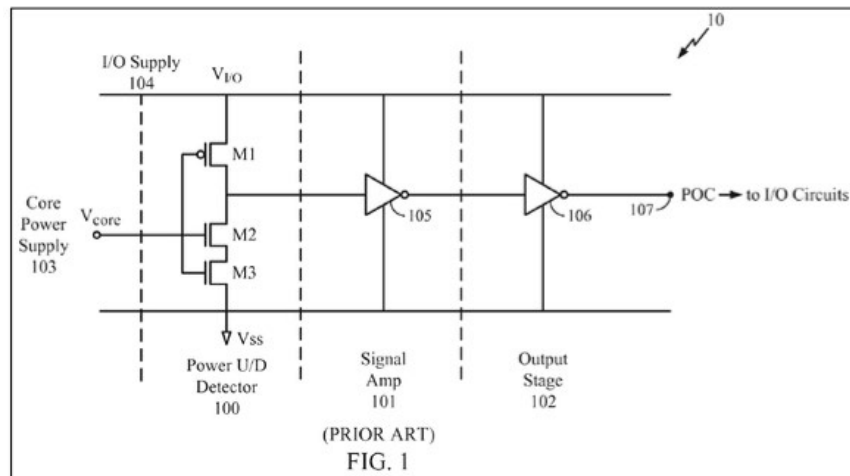
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Qualcomm owns the '674 patent, which is directed to integrated circuit devices with power detection circuits for systems with multiple supply voltages. *See* '674 patent at Abstract, col. 1 ll. 6–8. According to the '674 patent, modern integrated circuits often contain multiple networks operating at different supply voltages. *See id.* at col. 1 ll. 22–25. For example, a core logic network may operate at a lower voltage, and an input/output network may simultaneously operate at a higher voltage. *See id.* Such a system can save power by allowing the broader circuit to power down a network, like the core logic network, when it is not needed. *See id.* at col. 1 ll. 26–40.

The patent describes “level shifters” that communicate between the input/output devices and the core devices. *See id.* at col. 1 ll. 28–29. When the core devices are powered down, the connection between the core and input/output network through the level shifters can lead to problems. One such problem is stray currents causing the level shifters to trigger the input/output devices for transmission

resulting in erroneous output signals from the circuit. *See id.* at col. 1 ll. 29–40.

The '674 patent describes a prior art method to remedy the stray current problem. The Background states that power-up/down detectors can be used to generate a power-on/off-control (POC) signal internally that instructs the input/output devices when the core devices are shut down. *See id.* at col. 1 ll. 55–58. Figure 1 of the patent depicts a “prior art” “standard POC system” with a power-up/down detector 100:



Id. at Figure 1.

The patent asserts that there are problems with the prior art solution in Figure 1. For example, when the input/output power supply 104 is on and the core power is off, powering up the core results in “a period in which all three transistors [M1-M3] within power up/down detector 100 are on,” causing “a significant amount of current to flow from [input/output] power supply 104 to ground.” *Id.* at col. 2 ll. 21–29. The '674 patent recognizes that “decreas[ing] the sizes of the transistors M1-M3” can physically limit this “glitch current” or leakage but notes that smaller transistors may reduce detection sensitivity or result in “longer

processing time for power-up/down events.” *Id.* at col. 2 ll. 31–39; *see also id.* at col. 2 l. 63–col. 3 l. 11.

The ’674 patent avoids these problems by adding a feedback network to increase detection speed. *See id.* at col. 6 ll. 25–28. Specifically, as depicted in Figure 4, the ’674 patent includes power-up transistor M8. Transistor M8 transitions from on to off during power-up and from off to on during power-down. *See id.* at col. 6 ll. 12–18, 21–28. When M8 is off, the current capacity of the power-up/down detector is reduced. When M8 is on, the power-up/down detector has increased current capacity resulting in quicker detection of the core powering down. *See id.*

Claims 1, 2, 5–9, 12, 13, and 16–22 of the ’674 patent are at issue on appeal. Claim 1, reproduced below, is illustrative of the claimed invention:

1. A multiple supply voltage device comprising:

a core network operative at a first supply voltage;
and

a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;

one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first

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