

<http://www.ece.umd.edu/courses/enee359a.S2007/>

 JUN JUL MAR
 ◀ 04 ▶
 2007 2008 2016

10 captures
 4 Jul 2008 - 8 Nov 2018


 About this capture



DEPARTMENT OF
ELECTRICAL &
COMPUTER ENGINEERING

CLASS
sites

ENEE 359A: Digital VLSI Circuits by B. Jacob

Spring 2007

Course Information:

Lecture: Tue Thu 2:00 - 3:15, EGR-3114
 Mailing List: enee359a-0101-spring07@coursemail.umd.edu
 Required Text: *Digital Integrated Circuits: A Design Perspective, 2nd Ed.*, by Rabaey, Chandrakasan, and Nikolic
 Recommended Texts:
 Dally & Poulton: *Digital Systems Engineering*
 Johnson & Graham: *High-Speed Digital Design*
 Uyemura: *Introduction to VLSI Circuits and Systems*
 Baker, Li, & Boyce: *CMOS: Circuit Design, Layout, and Simulation*

Instructor Information:

Professor: [Bruce L. Jacob](#), Associate Professor, Electrical & Computer Engineering
 Office: 1325 A.V. Williams Building
 Phone: (301) 405-0432
 Email: blj@ece.umd.edu
 Office Hours: *Open door policy (for now ...)*

TA: Elliott Cooper-Balis
 Email: ecc17@umd.edu
 Recitations: Tue 3:30 - 4:30pm, ???

Course Handouts and General Information:

- [Syllabus.pdf](#)
- [A great Verilog tutorial on-line](#), and [PDF of that same tutorial](#).
- [verilog-handbook.pdf](#). This is a concise overview of the Verilog programming language.
- [realize-verilog.pdf](#). Gives a functional view of Verilog; i.e. if you want to build a processor model, this shows how. However, it confuses blocking/non-blocking assignments (calls "=" non-blocking and "<=" blocking). Otherwise, it is a decent overview.
- [scaling.gif](#). A **very** interesting picture illustrating the degree to which VLSI designs have reduced in size since the Intel 4004.
- [2007-midterm-solutions.pdf](#). Midterm exam, grade distribution, solutions.

<http://www.ece.umd.edu/courses/enee359a.S2007/>

Go

JUN JUL MAR

◀ 04 ▶

2007 2008 2016



▼ About this capture

10 captures

4 Jul 2008 - 8 Nov 2018

Weeks 1/2	enee359a-overview.pdf	Ch. 1	<i>Course overview in a nutshell</i>
Weeks 2/3	enee359a-devices.pdf	Ch. 3.1-3.3.2, 5.1-5.3	<i>Intro to (Verilog) design, P/N junctions, MOS transistors, CMOS inverter</i>
Week 4	enee359a-CMOS.pdf	Ch. 6-6.2	<i>Static CMOS Design</i>
Week 5	enee359a-manufacturing.pdf		<i>Cadence tools & manufacturing processes</i>
Week 6	enee359a-sizing.pdf	Ch. 5.4-5.7	<i>Transistor Sizing & Logical Effort</i>
Week 7	enee359a-wires.pdf	Ch. 4	<i>Interconnects (i.e., wires)</i>
Week 8	Review and Midterm		
Week 9	<i>SPRING BREAK</i>		
Weeks 10/11	enee359a-sequential.pdf	Ch. 7	<i>Sequential Circuits: Latches, Registers, Pipelines</i>
Week 12	enee359a-parasitics.pdf	Ch. 9	<i>Capacitive, Resistive, and Inductive Parasitics</i>
Weeks 13/14	enee359a-timing.pdf	Ch. 10	<i>System Timing: Synchronous, Asynchronous, etc.</i>
Weeks 15	enee359a-SRAM-i.pdf	<i>not really in book</i>	<i>Low-Power SRAM Circuits</i>
Week 16	enee359a-DRAM-i.pdf enee359a-DRAM-ii.pdf	<i>not really in book</i>	<i>DRAM Systems & Circuits ... pictures of cells</i>

Assignments:

ID	Out	Due	Write-up	Homework Solution/Project Distribution
Project 1	01-Feb-2007	13-Feb-2007	p1.pdf	Project 1 Distribution
HW-1	15-Feb-2007	20-Feb-2007	hw1.pdf	
Project 2	20-Feb-2007	06-Mar-2007	p2.pdf	Project 2 Distribution
HW-2	20-Feb-2007	27-Feb-2007	hw2.pdf	
Project 3	01-Mar-2007	29-Mar-2007	p3.pdf	Project 3 Distribution
HW-3	09-Mar-2007	13-Mar-2007	hw3.pdf	
Project 4	12-Apr-2007	24-Apr-2007	p4.pdf	
HW-4	01-May-2007	10-May-2007	hw4.pdf	DFF-sim.pdf

ENEE 359a
Lecture/s 9
Transistor Sizing

Bruce Jacob

University of
Maryland
ECE Dept.

SLIDE 1

ENEE 359a *Digital VLSI Design*

Transistor Sizing & Logical Effort

Prof. Bruce Jacob
blj@ece.umd.edu

Credit where credit is due:

Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Dally's EE273 slides (Stanford), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).



UNIVERSITY OF MARYLAND

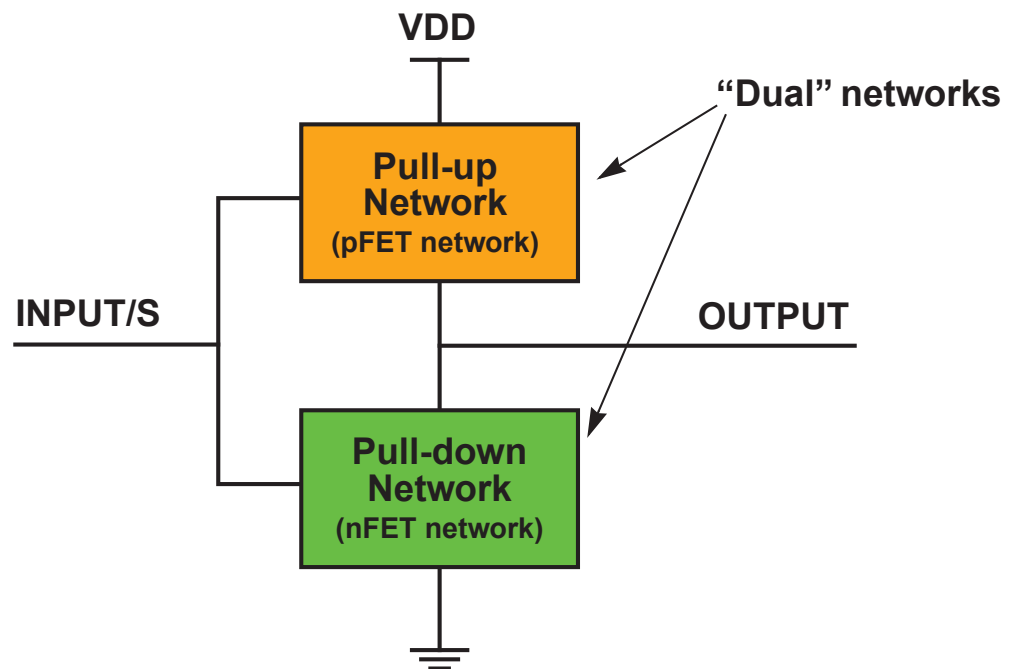
Overview

- **Sizing of transistors to balance performance of single inverter**
- **More on RC time constant, first-order approximation of time delays**
- **Sizing in complex gates, examples**
- **Sizing of inverter chains for driving high capacitance loads (off-chip wires)**



Resistance

WOULD LIKE BALANCED NETWORKS:



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.