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# United States Patent [19]

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Voss et al.

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- [54] **BUFFER WITH PSEUDO-GROUND HYSTERESIS**
- [75] Inventors: **Peter H. Voss, Watsonville; Shahryar Aryani, Santa Clara, both of Calif.**
- [73] Assignee: **Cypress Semiconductor Corporation, San Jose, Calif.**
- [21] Appl. No.: **126,065**
- [22] Filed: **Sep. 23, 1993**
- [51] Int. Cl.<sup>6</sup> ..... **H03K 17/16**
- [52] U.S. Cl. .... **326/34; 326/65; 327/206**
- [58] Field of Search ..... **307/443, 451, 475**

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

### [57] ABSTRACT

A buffer utilizing the pseudo-ground hysteresis of the present invention contains first and second stage switching elements and a resistive element. The pseudo-ground hysteresis is implemented via a ground path from the switching elements. The first stage switching element is configured to have a first DC voltage trip point, and the second stage switching element is configured to have a second DC voltage trip point. As an input voltage, transitioning from a first state to a second state, is applied to the first stage switching element, a first current ( $I_1$ ), from the first stage switching element, and a second current ( $I_2$ ), from the second stage switching element, is generated. When the input voltage equals the first stage DC voltage trip point, the first and second stage switching elements transition. During the transition of the input voltage from the second state to the first state, the total current flowing through resistive element is reduced, and the voltage at the resistive element decreases. Consequently, the first stage switching element transitions at a voltage level offset from the first DC voltage trip point to provide hysteresis for the second state to first state transition of the input voltage.

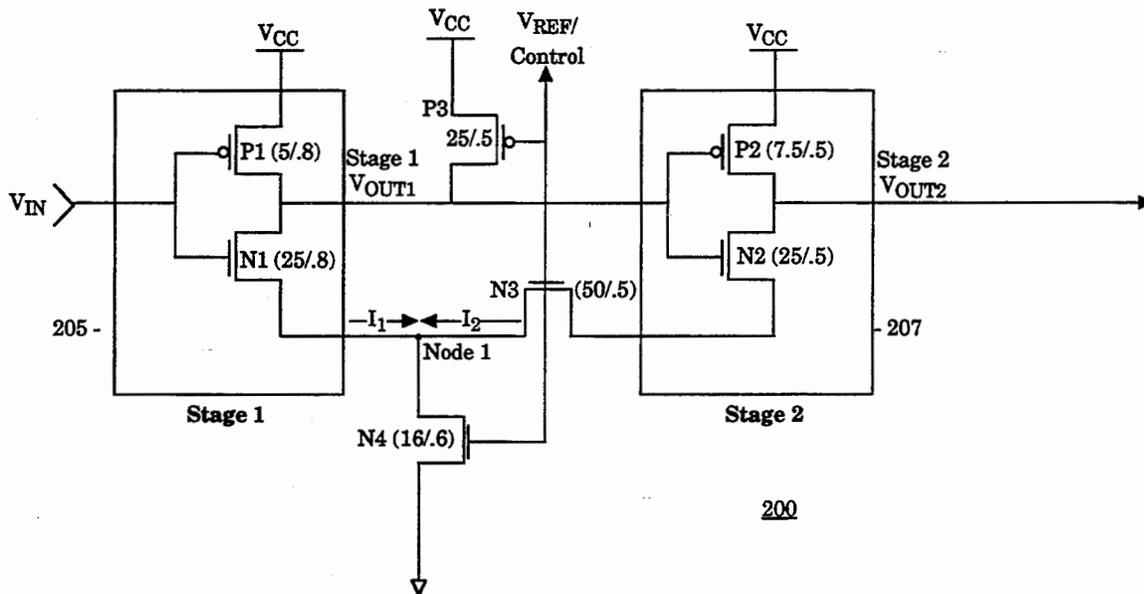
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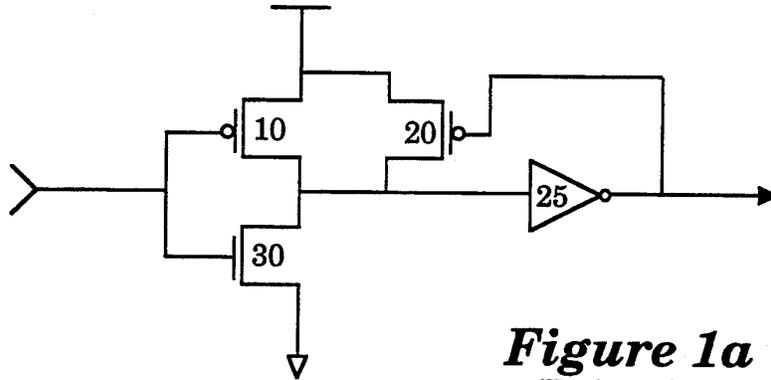
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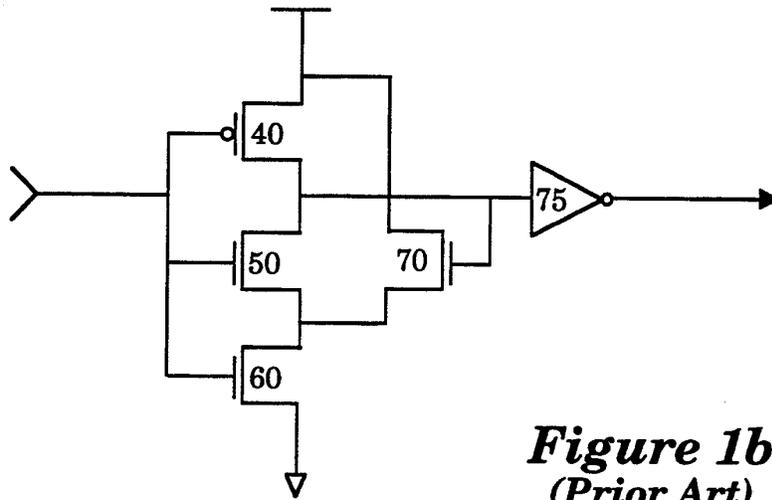
Primary Examiner—Edward P. Westin  
 Assistant Examiner—Andrew Sanders

15 Claims, 6 Drawing Sheets

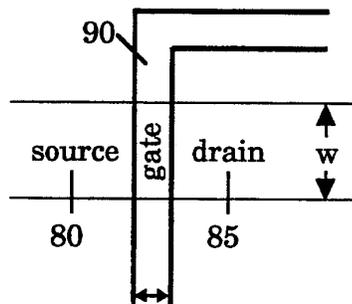




**Figure 1a**  
*(Prior Art)*



**Figure 1b**  
*(Prior Art)*



**Figure 1c**

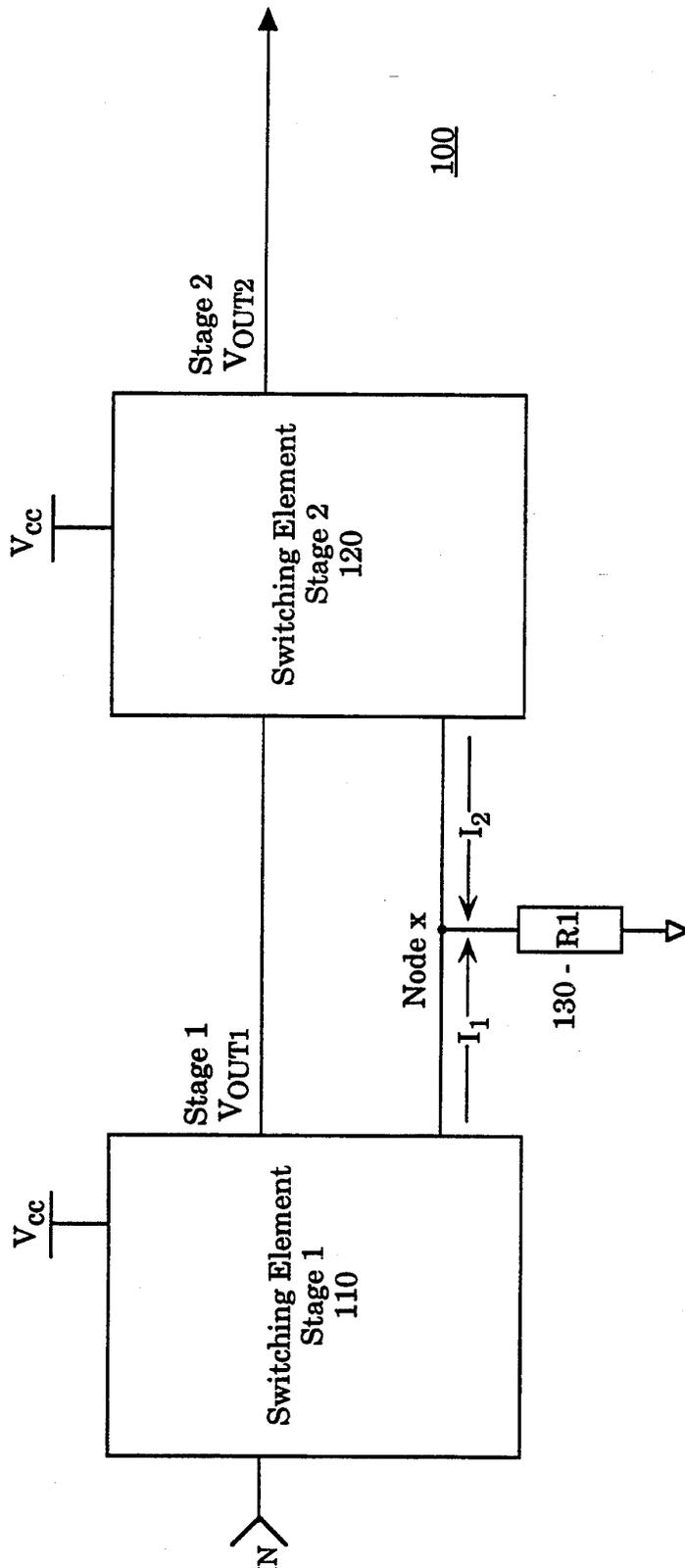


Figure 2

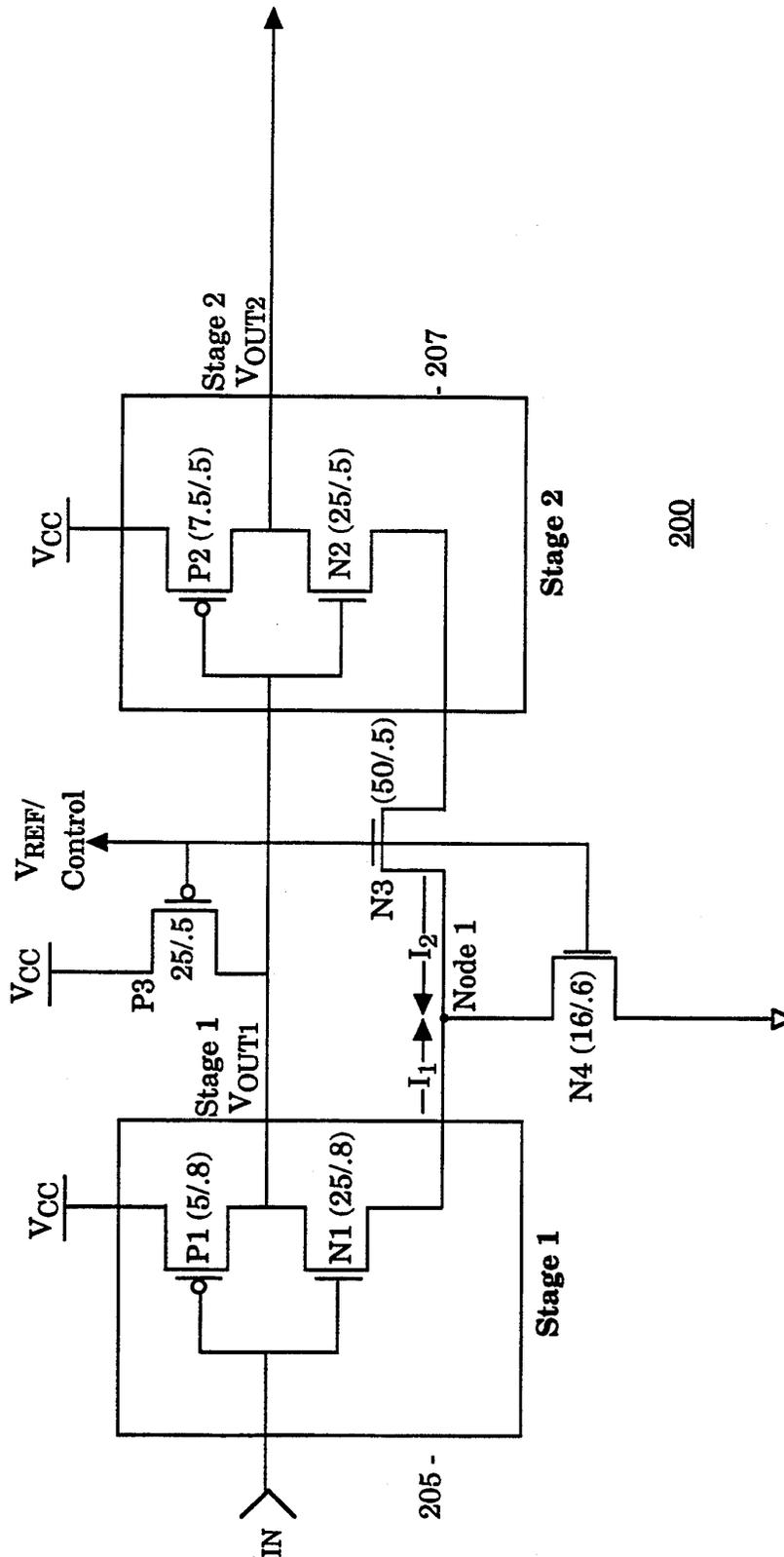


Figure 3

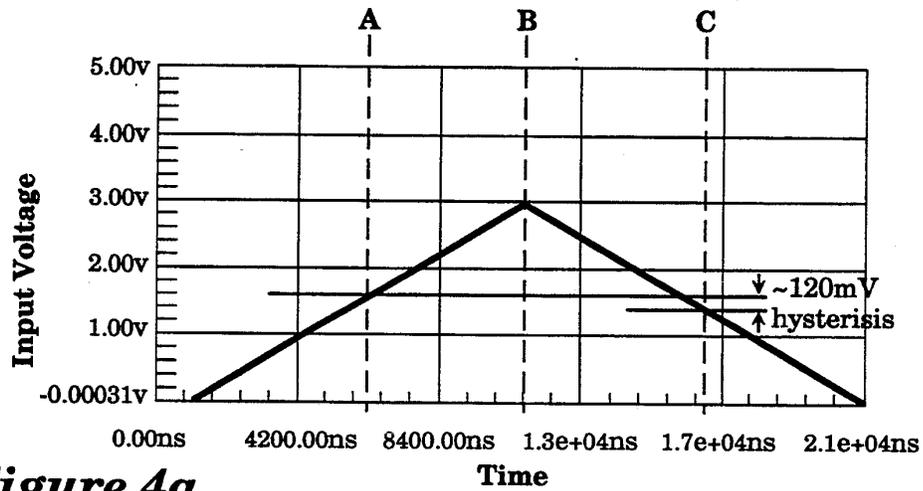


Figure 4a

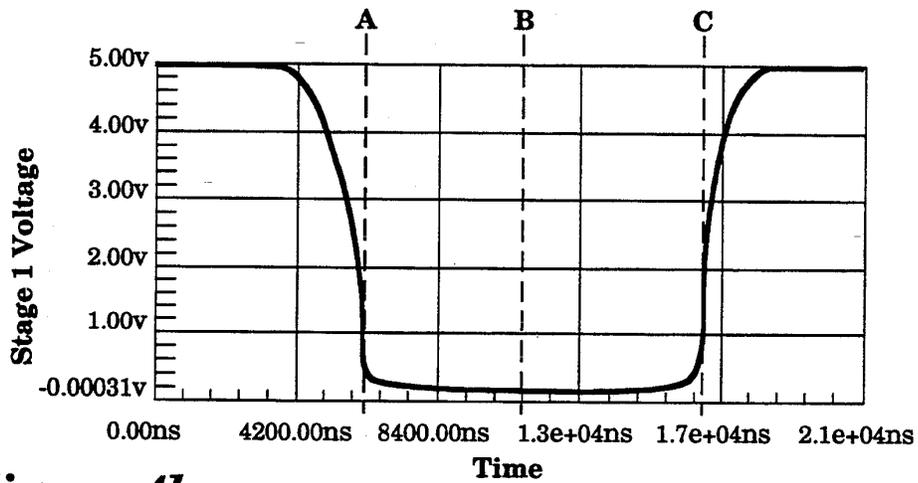
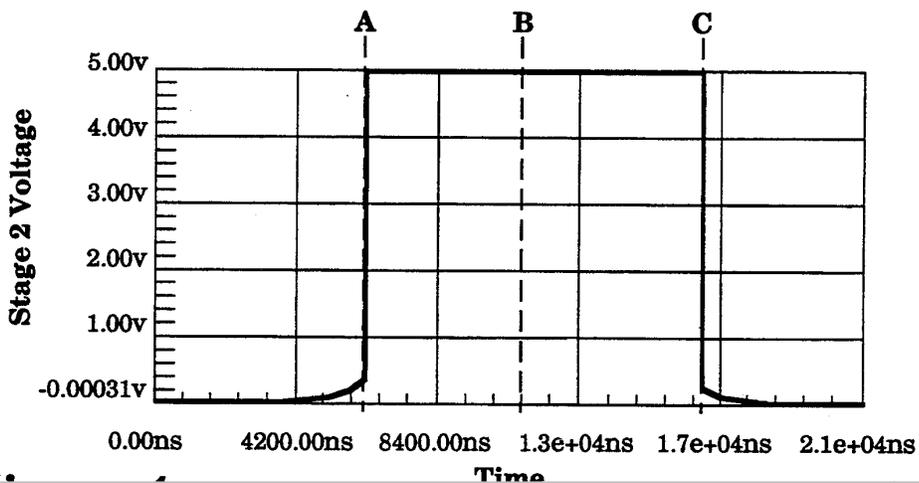


Figure 4b



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