IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Chang Ki Kwon *et al.*
U.S. Patent No.:	8,063,674
Issue Date:	November 22, 2011
Appl. Serial No.:	12/365,559
Filing Date:	February 4, 2009
Title:	Multiple supply-voltage power-up/down detectors

SUPPLEMENTAL DECLARATION OF ROBERT W. HORST, PH.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

I. Introduction

1. This declaration supplements the declaration entitled "Declaration of Robert W. Horst, Ph.D." dated June 17, 2018 (hereinafter "Original Declaration"). The statements made and opinions rendered therein can be assumed to be incorporated into this supplemental declaration, except as may be explicitly noted otherwise herein.

2. In addition to the materials I reviewed in preparation of my Original Declaration—which were noted in paragraph 7—I have reviewed the following list of materials in preparation of this declaration:

- Patent Owner Response to Petition (Paper 12)
- Dr. Massoud Pedram's Declaration (Ex. 2002)
- Horst Declaration Transcript (Ex. 2003)
- Pedram Deposition Transcript (APPLE-1017)

- U. Daya Perera, *Reliability of Mobile Phones*, 1995 IEEE Proceedings Annual Reliability and Maintainability Symposium (Jan. 1995) (APPLE-1019)
- U.S. Patent No. 5,386,153 ("Voss") (APPLE-1022)
- Wikipedia Entry for "LTspice" available at https://en.wikipedia.org/wiki/LTspice (accessed on July 17, 2019) (APPLE-1023)
- John F. Wakerly, DIGITAL DESIGN PRINCIPLES AND PRACTICES 4th Ed. (2006) (APPLE-1024)
- Bruce Jacob, ENEE 359a Digital VLSI Design - Transistor Sizing & Logical Effort, available at https://ece.umd.edu/courses/enee359a.S2007/ (APPLE-1025)

II. Dr. Pedram's Analysis of the Prior Art is Incorrect and Incomplete

A. SPICE simulation shows a Steinacker/Doyle/Park combination that does not result in increased leakage current, DC fighting conditions, or a breakdown in circuit functionality.

3. Dr. Pedram has claimed that the Steinacker/Doyle/Park combination would not function in the same manner as the '674 patent and could suffer from increased leakage current, DC fighting conditions, or a breakdown in circuit functionality.

Q. Dr. Pedram, it's your opinion that the petitioner's proposed combination of Steinacker, Doyle and Park would result in increased leakage current, potentially a DC fighting condition and potentially a complete breakdown of circuit functionality; correct?

A. Yes, that's what I said.

Q. Your declaration does not include any simulations of the applicant's proposed application of Steinacker, Doyle and Park; correct?

A. That's correct. Yes.

Ex. 1017, 167:13-23.

4. However, Dr. Pedram did not run any simulations or include detailed analysis to support his conclusions. *See* Ex. 1017, 40:15-41:13, 167:20-23, 171, 20-172:1, 180:6-16. I do not agree with his conclusions and have run SPICE circuit simulations to show that he is incorrect or has analyzed the circuits under unspecified conditions that introduce such problems. Based on my analysis and simulations, the prior art combinations operate nearly identically to the circuit

shown in Figure 4 of the '674 Patent (hereinafter referred to as the "'674 Figure 4 circuit") and do not introduce the presumed problems described by Dr. Pedram.[1]

5. SPICE is a widely-available, well-known circuit simulation program which is often used for the development and analysis of analog circuits. For the following simulations, I used LTSpice XVII from Analog Devices, a widely used and free circuit electronic circuit simulator[2]. *See generally* Ex. 1023. SPICE circuit simulations were run to verify the operation of the '674 Figure 4 circuit, the prior art circuits, and the combinations described in my Original Declaration.

6. The simulations use a power supply with Vdd=5V ($V_{I/O}$) and test the ability of the circuit to detect power up and down of a 3.3V supply (V_{core}). Power up is detected at ~3V, and power down at ~2.5V. MOSFET thresholds have been

[1] The '674 Figure 4 circuit is one of three preferred embodiments described in the '674 Patent—Figures 5 and 6 being the other two. The '674 Figure 4 circuit includes various limitations that are not required by the claims of the '674 Patent. In fact, Dr. Pedram agrees the specific transistor configuration (including number of PMOS transistors and location of feedback) of the '674 Figure 4 circuit is not a requirement of any independent claim. *See* Ex. 1017, 80:19-86:21.

[2] The tool is available at https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

set based on these voltages, and all simulations of the '674 Figure 4 circuit and prior art combinations use the same threshold settings. Dr. Pedram agreed that the '674 Figure 4 circuit could operate at these voltages:

> Q. If I were designing a system where V I/O was 5 volts and Vcore ranged from 0 to 3.3 volts, would I be able to use the circuitry shown in Figure 4 to detect when Vcore reached 3.3 volts?
> A. Yes. When it reaches 3.3 volts, yes, you can.

Ex. 1017, 108:13-18.

7. SPICE requires setting parameters to match the circuit being simulated. Some of the required parameters for this circuit include the thresholds for the inverters and the thresholds and strengths (width and length) of the transistors. The '674 patent has no guidance for these parameters and expects someone applying the circuits to have sufficient expertise and experience to set the parameters appropriately. Where possible, I used channel length and width parameters based on the Voss reference (Ex. 1022) that was available prior to the critical date of the '674 patent. For other parameters, such as transconductance, I relied on the LTSpice default settings.

8. The following SPICE simulations specify the turn-on thresholds and channel width and length, but use defaults for the other MOSFET parameters. The thresholds were set to make the circuits operable to detect power up and down for a

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