UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,063,674 B2
APPLICATION NO. : 12/365559
DATED : November 22, 2011
INVENTOR(S) : Chang Ki Kwon and Vivek Mohan

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification

Column 8, Line 58, the word "more" should be deleted

Signed and Sealed this
Fifth Day of December, 2017

Joseph Matal
Performing the Functions and Duties of the
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,063,674

APPLICATION NO.: 12/365,559

ISSUE DATE : 11/22/2011

INVENTOR(S) : Chang Ki KWON
Vivek MOHAN

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8, Line 58, the word “more” should be deleted

MAILING ADDRESS OF SENDER (Please do not use customer number below):

5775 Morehouse Drive
San Diego, CA 92121

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	8,063,674	Confirmation No.	6210
Applicant	:	Chang Ki KWON		
Issued	:	11/22/2011		
Patentee	:	QUALCOMM Incorporated		
Docket No.	:	072302		
Customer No.	:	23696		

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

An error appears in this patent of a clerical nature, of a typographical nature, or a mistake of minor character. The correction does not involve changes which would constitute new matter or require reexamination. A certificate of correction for the above referenced patent is requested. Attached hereto, in duplicate, is Form PTO/SB/44.

Please charge any fees, including any fees required under §1.20(a), or credit overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: 10/25/2017

By: /Xiaotun Qiu/
Xiaotun Qiu, Reg. No. 73,093

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-2426 Facsimile: (858) 658-2502

Electronic Patent Application Fee Transmittal					
Application Number:	12365559				
Filing Date:	04-Feb-2009				
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS				
First Named Inventor/Applicant Name:	Chang Ki Kwon				
Filer:	Xiaotun Qiu/karina filer				
Attorney Docket Number:	072302				
Filed as Large Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description		**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
Certificate of correction		1811	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt	
EFS ID:	30762943
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Xiaotun Qiu/karina filer
Filer Authorized By:	Xiaotun Qiu
Attorney Docket Number:	072302
Receipt Date:	25-OCT-2017
Filing Date:	04-FEB-2009
Time Stamp:	18:51:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$100
RAM confirmation Number	102617INTEFSW00005946170026
Deposit Account	170026
Authorized User	karina filer
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	072302_Certificate_of_Correction_2017_10_25.pdf	163971 249b5a7953880b27e220e933e2feb7202461c132	no	2
Warnings:					
Information:					
2	Request for Certificate of Correction	072302_Request_Cert_Correction_XQ.pdf	30054 58706efd558a86879cf635909cb4c612fcec55d0	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30796 4f1e95b4de1ba5db65fb3d4239a2937f1b3b79df	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	224821		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	11/22/2011	8063674	072302	6210

23696 7590 11/02/2011

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 165 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Chang Ki Kwon, San Diego, CA;
Vivek Mohan, San Diego, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

QUALCOMM INCORPORATED
5775 MOREHOUSE DRIVE
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12365559	2009-02-04	Chang Ki Kwon	072302	6210

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$1810	10/12/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sam Talpalatsky
2 Nicholas J. Pauley
3 Jonathan T. Velasco

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
QUALCOMM Incorporated	San Diego, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 170026

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Sam Talpalatsky/ Date October 11, 2011

Typed or printed name Sam Talpalatsky Registration No. 35380

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12365559
Filing Date:	04-Feb-2009
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS
First Named Inventor/Applicant Name:	Chang Ki Kwon
Filer:	Peter M. Kamarchik/Theresa Boyce
Attorney Docket Number:	072302

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2040**

Electronic Acknowledgement Receipt	
EFS ID:	11166621
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Peter M. Kamarchik/Theresa Boyce
Filer Authorized By:	Peter M. Kamarchik
Attorney Docket Number:	072302
Receipt Date:	12-OCT-2011
Filing Date:	04-FEB-2009
Time Stamp:	09:20:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2040
RAM confirmation Number	7735
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	072302_IFP_10-12-11.pdf	58961 c44ac6a9fdb7088ebc437c1171a76ab1b92f a819	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32290 c9a1ee7a9a3f35007143cd601432f00ff0609 195	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	91251		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23696 7590 07/12/2011
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/12/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

TITLE OF INVENTION: MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/12/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23696 7590 07/12/2011
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

TITLE OF INVENTION: MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/12/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
WHITE, DYLAN C	2819	327-143000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

23696 7590 07/12/2011

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/12/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 165 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 165 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/365,559	KWON ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/24/2011*.

2. ☒ The allowed claim(s) is/are *1,3-5,7-10 and 12-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/24/2011
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Shawki S Ismail/
Supervisory Patent Examiner, Art Unit 2819

DETAILED ACTION

Information Disclosure Statement

The Examiner acknowledges the applicants submission of an Information Disclosure Statement on 6/24/2011.

Allowable Subject Matter

Claims 1, 3-5, 7-10, 12-25 are allowed. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, A multiple supply voltage device comprising: a core network operative at a first supply voltage; and a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state; one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector; at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; ***at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being***

configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down; at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor, nor would it have been obvious to one of skill in the art. Claims 3-5, and 7-9 are also allowed as being dependent on claim 1.

Regarding claim 10, A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising: detecting a power-on of a second supply voltage while a first supply voltage is already on; ***decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection***; detecting a power-down of said second supply voltage while said first supply voltage is on; ***increasing said current capacity of said power on/off detector in response to said power-down detection;*** receiving a logic-high signal at a control gate of at least one first transistor, at least one second transistor and ***at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor***, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal, nor would it have been obvious to one of skill in the art. Claims 12-19 are also allowed as being dependent on claim 10.

Regarding claim 20, A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said system comprising: means for detecting a power-on of a second supply voltage while a first supply voltage is already on; means, ***responsive to said power-on detection, for decreasing a current capacity of a power on/off detector of said POC network***; means for detecting a power-down of said second supply voltage while said first supply voltage is on; means, ***responsive to said power-down detection, for increasing said current capacity of said power on/off detector***; means for receiving a logic-high signal at a control gate of at least one first transistor at least one second transistor and ***at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor***, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and means for transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal, nor would it have been obvious to one of skill in the art. Claims 21-25 are also allowed as being dependent on claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to power up and power down circuits and their methods of operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Shawki S Ismail/
Supervisory Patent Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/365,559	Applicant(s)/Patent Under Reexamination KWON ET AL.	
	Examiner DYLAN WHITE	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,577,166	06-2003	Lim, Kyu-Nam	327/77
*	B	US-5,723,990	03-1998	Roohparvar, Frankie F.	327/81
*	C	US-2008/0100341	05-2008	Kim, Min-Hwahn	326/63
*	D	US-2006/0044027	03-2006	Chen, Kuan-Yeu	327/143
*	E	US-2008/0218223	09-2008	Kimura, Hiroyuki	327/142
*	F	US-4,781,051	11-1988	Schultes et al.	72/247
*	G	US-5,495,453	02-1996	Wojciechowski et al.	365/185.18
*	H	US-2009/0027087	01-2009	Sukup et al.	327/72
*	I	US-6,900,666	05-2005	Kursun et al.	326/95
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2010	02/11/2011	06/03/2011	06/29/2011					
1	1	✓	✓	=	=					
-	2	O	-	-	-					
2	3	O	✓	=	=					
3	4	O	O	=	=					
4	5	O	O	=	=					
-	6	O	-	-	-					
5	7	✓	✓	=	=					
6	8	✓	✓	=	=					
7	9	✓	✓	=	=					
8	10	✓	✓	=	=					
-	11	O	-	-	-					
9	12	O	✓	=	=					
10	13	O	O	=	=					
11	14	O	O	=	=					
12	15	O	✓	=	=					
13	16	O	O	=	=					
14	17	O	O	=	=					
15	18	O	O	=	=					
16	19	✓	✓	=	=					
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20	23	✓	✓	=	=					
21	24	✓	✓	=	=					
22	25	✓	✓	=	=					
-	26	✓	-	-	-					
-	27	✓	-	-	-					

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	**Art Unit**
	DYLAN WHITE	2819

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED									
327	143	H	0	3	L	7 / 00 (2006.0)										
CROSS REFERENCE(S)		H	0	3	L	5 / 00 (2006.0)										
		H	0	3	K	5 / 153 (2006.0)										
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	H	0	3	K	19 / 094 (2006.0)										
327	72	333														
326	68															

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	14	17												
-	2	15	18												
2	3	16	19												
3	4	17	20												
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-	11	-	27												
9	12														
10	13														
11	14														
12	15														
13	16														

/DYLAN WHITE/ Examiner.Art Unit 2819	6/3/2011	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	22	
/SHAWKI ISMAIL/ Supervisory Patent Examiner.Art Unit 2819	06/30/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	4

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	82, 83, 86, 87, 93, 112, 119	6/3/2011	DW
327	333, 108	6/3/2011	DW

SEARCH NOTES		
Search Notes	Date	Examiner
See Attached EAST Notes	6/29/2011	DW
Inventor Search	9/9/2010	DW
Assignee Search	9/9/2010	DW
Information Disclosure Statement	6/29/2011	DW
Keyword Search for classes 326 and 327	6/29/2011	DW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
326	All Subclasses	6/29/2011	DW

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known

Application Number	12/365,559
Filing Date	2009-02-04
First Named Inventor	Chang Ki KWON
Art Unit	2819
Examiner Name	Dylan C. WHITE
Attorney Docket No:	072302

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
/DW/	001	International Search Report and Written Opinion - PCT/US2010/023081, International Search Authority - European Patent Office - 08/05/2010 (072302).	☐

EXAMINER SIGNATURE /Dylan White/ **DATE CONSIDERED** 06/29/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes ofUSPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by theUSPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

EAST Search History

EAST Search History (Prior Art) /DW/

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	15	(detect$3 adj2 (power) with (on and off))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:31
S2	80695	(((voltage or power) adj2 (switch$3 or gat $3)) or (head$3 and foot$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:35
S3	41160	((voltage or power) adj (switch$3 or gat$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:36
S4	133254	((voltage or power) adj (detect$3 or (up and down)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:37
S5	2	("7253655").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:38
S6	6	("4859877" | "5381059" | "6172522" | "6233694" | "6498511" | "7116135").PN. OR ("7253655").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:42
S7	46	((voltage or power) adj (detect$3 with ((up and down) or (on and off))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45
S8	195	kwon-chang$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45

S9	19	S8 and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:46
S10	28	mohan-vivek$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:47
S11	5	("20040111649" | "20050117432" | "6611472" | "6650594" | "7372746").PN. OR ("7692998").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:56
S12	12	("4697097" | "5187389" | "5442312" | "5528182" | "5528184").PN. OR ("5781051").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:59
S13	65	("4683382" | "4975883" | "5193198" | "5301161" | "5305275" | "5331599" | "5339272" | "5412331" | "5414669").PN. OR ("5594360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:02
S14	4636	((voltage or power or level) adj (detect$3 or sens$3) with transistor) and feedback	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S15	628	S14 and core	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S16	74	S15 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:11
S17	859	S14 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S18	9901	(POC or (power adj (on adj off) adj control))	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S19	118	S18 and (feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S20	513	qualcomm.AS. and (((power or voltage) with control) and feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24

S21	123	qualcomm.AS. and (((power or voltage) with control) with feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24
S23	3959	((voltage or power or level) adj (detect$3 or sens$3) with feedback) and transistor	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S24	472	S23 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S25	0	(11/048260).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:14
S26	1	(10/339069).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:28
S27	5	("5629642" | "5774402" | "6011447" | "6111441").PN. OR ("6744295").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:29
S28	2	("20050140406" | "6163585").PN. OR ("7612588").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:37
S29	7	("5886567" | "5889664" | "6169426" | "6580312" | "6876246" | "7474140").PN. OR ("7605639").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:38
S30	11	("20060119417" | "4565977" | "5535160" | "5877651" | "6130829" | "6304469" | "6522558" | "6756827" | "6812776" | "6977828" | "7042774").PN. OR ("7429883").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:41
S31	11	("6307401" | "6433579" | "6437599" | "6518797" | "6590422" | "6664814" | "6664853" | "6731135" | "6847232").PN. OR ("7183805").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:44
S32	9	("5270584" | "5721510" | "5723990" | "6411157").PN. OR ("6577166").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:49

S33	36	("4961167" | "5189316" | "5315557" | "5337284" | "5557231" | "5602704" | "5633825" | "5673232" | "5856951" | "6031411").PN. OR ("6411157").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:01
S34	18	("5115150" | "5151620" | "5175448" | "5661419" | "5880604" | "6049245" | "6107869" | "6191615" | "6204696" | "6370052" | "6404269" | "6411157" | "6442086" | "6492837" | "6759873").PN. OR ("6900690").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:29
S35	7526	(input and output) and core and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S36	352	S35 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S37	389	(input and output) and (core adj2 voltage) and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S38	49	S37 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S39	0	(power adj ((on and off) or (up and down)) adj detect$3) and core and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:35
S40	9	(power adj ((on and off) or (up and down)) adj detect$3) and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:36

S41	1	(power adj ((on and off) or (up and down)) adj detect$3) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S42	2	(power adj ((on and off) or (up and down)) adj detect$3) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S43	40	("4234920" | "4473759" | "4746822" | "4882506" | "4902910" | "5039875" | "5063304" | "5066869" | "5081625" | "5087834" | "5103115" | "5103159" | "5120993" | "5157270" | "5159206" | "5164613" | "5166545" | "5168209" | "5181203" | "5220534" | "5233161" | "5270977" | "5297261" | "5347173").PN. OR ("6204701").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 15:38
S44	11869	((level or voltage) adj (shift$3 or translat$3)) and (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:40
S45	3036	S44 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S46	2898	S45 and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S48	920	((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41

S49	359	S48 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S51	3322	(((power or voltage) adj2 detect$3) with transistor) and inverter and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S52	930	S51 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S53	1130	(((power or voltage) adj2 detect$3) with transistor) and inverter and current and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S54	295	S53 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S55	5049	((power or (up and down)) adj2 detect$3) and feedback and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S56	405	S55 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S57	336	S56 not S54	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S58	5546	((level or voltage) adj (shift$3 or translat$3)) and feedback and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:49
S59	1712	S58 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:50

S60	430	(((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)) and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:52
S61	644	(((level or voltage) adj (shift$3 or translat$3)) with (feedback)) and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S62	283	S61 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S63	147	S61 and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:01
S64	15	("20020163364" | "20060103437" | "20070030039" | "5130569" | "6646844" | "2007091211").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:39
S66	1875	(voltage level) adj (shift $3 translat$3) and (transistor with series) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:10
S67	602	S66 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:11
S68	4569	(voltage level) adj (shift $3 translat$3) and (transistor with series) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:56
S69	1994	(voltage level) adj (shift $3 translat$3) and (transistor with series) and (feedback with current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:57
S70	918	(voltage level) adj (shift $3 translat$3) and (transistor near2 series) and (feedback with current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58

S71	312	S70 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58
S72	259	S71 not S67	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58
S73	78	("3333113" | "4254501" | "4385394" | "4393494" | "4419594" | "4588941" | "4645948" | "4647912" | "4723108" | "4751404" | "4760292" | "4763021" | "4774422" | "4825402" | "4855622" | "4855623" | "4894561" | "4922140" | "4929941" | "4972106" | "4978905" | "4980579" | "5015888" | "5017813" | "5021684" | "5021691" | "5023487" | "5023488" | "5029728" | "5034632" | "5041743" | "5070256" | "5079456" | "5081380" | "5095231" | "5117130" | "5118971" | "5165046" | "5198701" | "5200654" | "5208492" | "5216292" | "5218239" | "5231315" | "5241221" | "5254883" | "5285116" | "5291071" | "5293082" | "5296756" | "5304861" | "5313118" | "5315174" | "5319258" | "5329184" | "5334882" | "5338987").PN. OR ("5539341").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 14:06
S74	544	(MTCMOS or (power adj gating)) and ((current) with (increas$3 decreas$3))	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:38

S75	96	(MTCMOS or (power adj gating)) and ((current) with (increas $3 decreas$3)) and (transistor near2 series)	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:38
S76	505	(MTCMOS or (power adj gating)) and ((current) with (increas $3 decreas$3)) and (transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:39
S77	277	S76 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:39
S78	237	white-dylan$.XA.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:40
S79	19	("5973541" | "6049231" | "6429689" | "6522171" | "6580293").PN. OR ("6900666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:58
S80	6	((power adj2 (up and down)) adj2 detection) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/05 11:57
S82	3	"6646844"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/29 10:38
S83	2	"2002163364"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/29 10:51
S84	2	"20020163364"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/29 10:54
S85	3	"20070030039"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/29 10:58
S86	2	"20060103437"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/29 10:58

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	37	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2010/09/10 09:16
S65	39	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2011/02/13 21:21
S81	39	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2011/06/05 12:14

6/29/2011 2:22:53 PM
H:\East\Workspaces\12365559.wsp

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	12/365,559	Filing Date	2009-02-04	Docket Number (if applicable)	072302	Art Unit	2819
First Named Inventor	Chang Ki Kwon			Examiner Name	Dylan C. White		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 170026

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

PTO/SB/30EFS (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/ Semion Talpalatsky /	Date (YYYY-MM-DD)	2011-06-23
Name	Semion Talpalatsky	Registration Number	35380

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	12/365,559	Filing Date	2009-02-04	Docket Number (if applicable)	072302	Art Unit	2819
First Named Inventor	Chang Ki Kwon			Examiner Name	Dylan C. White		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
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SUBMISSION REQUIRED UNDER 37 CFR 1.114

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☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 170026

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/ Semion Talpalatsky /	Date (YYYY-MM-DD)	2011-06-23
Name	Semion Talpalatsky	Registration Number	35380

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known

Application Number	12/365,559
Filing Date	2009-02-04
First Named Inventor	Chang Ki KWON
Art Unit	2819
Examiner Name	Dylan C. WHITE
Attorney Docket No:	072302

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
	001	International Search Report and Written Opinion - PCT/US2010/023081, International Search Authority - European Patent Office - 08/05/2010 (072302).	☐

EXAMINER SIGNATURE **DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes ofUSPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by theUSPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	**2**	**of**	**2**

Complete if Known

Application Number	12/365,559
Filing Date	2009-02-04
First Named Inventor	Chang Ki KWON
Art Unit	2819
Examiner Name	Dylan C. WHITE
Attorney Docket No:	072302

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/ Semion Talpalatsky /	Date (YYYY-MM-DD)	2011-06-23
Name/Print	Semion Talpalatsky	Registration Number	35,380

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 072302WO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2010/023081	International filing date *(day/month/year)* 03/02/2010	(Earliest) Priority Date *(day/month/year)* 04/02/2009
Applicant QUALCOMM Incorporated		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 3B
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/22
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 646 844 B1 (MATTHEWS LLOYD P [US]) 11 November 2003 (2003-11-11) figures 1,3	1,2,4, 6-11,13, 15,17, 19-27
X	US 2002/163364 A1 (MAJCHERCZAK SYLVAIN [FR] ET AL) 7 November 2002 (2002-11-07) figure 2	1-3, 7-12,15, 16,19-27
X	US 2007/030039 A1 (CHEN KER-MIN [TW]) 8 February 2007 (2007-02-08) figure 3	1,2, 6-11,15, 19-22, 24-27

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2010	05/08/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Santos, Paulo

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/103437 A1 (KANG KHIL O [KR]) 18 May 2006 (2006-05-18) figure 3	1,6, 8-10, 19-27
A	WO 2007/091211 A2 (NXP BV [NL]; WESTENDORP JOEN [NL]; HOEFNAGEL LOUW [NL]) 16 August 2007 (2007-08-16) figure 3	1-27
A	US 5 130 569 A (GLICA STEPHEN J [US]) 14 July 1992 (1992-07-14) figure 1	1-27

1

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/023081

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6646844 B1	11-11-2003	NONE	
US 2002163364 A1	07-11-2002	EP 1249707 A1	16-10-2002
		FR 2822956 A1	04-10-2002
US 2007030039 A1	08-02-2007	NONE	
US 2006103437 A1	18-05-2006	JP 2006148858 A	08-06-2006
		KR 20060054612 A	23-05-2006
WO 2007091211 A2	16-08-2007	CN 101379406 A	04-03-2009
		JP 2009526461 T	16-07-2009
		US 2009002034 A1	01-01-2009
US 5130569 A	14-07-1992	DE 69216663 D1	27-02-1997
		DE 69216663 T2	03-07-1997
		EP 0503803 A1	16-09-1992
		JP 3225075 B2	05-11-2001
		JP 4345208 A	01-12-1992

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/023081	03.02.2010	04.02.2009

International Patent Classification (IPC) or both national classification and IPC
INV. H03K17/22

Applicant
QUALCOMM Incorporated

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Santos, Paulo Telephone No. +49 89 2399-8359

Form PCT/ISA/237 (Cover Sheet) (July 2009)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5, 8, 9, 14, 18, 19, 24, 25, 27
	No:	Claims	1-4, 6, 7, 10-13, 15-17, 20-23, 26
Inventive step (IS)	Yes:	Claims	5, 14, 18
	No:	Claims	1-4, 6-13, 15-17, 19-27
Industrial applicability (IA)	Yes:	Claims	1-27
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:
D1 : US 6 646 844 B1 (MATTHEWS LLOYD P [US]) 11 November 2003 (2003-11-11)
D2 : US 2002/163364 A1 (MAJCHERCZAK SYLVAIN [FR] ET AL) 7 November 2002 (2002-11-07)

2 The present application does not meet the criteria of Article 33 (1) PCT, because the subject-matter of claims 1, 10, 20 and 26 is not new in the sense of Article 33(2) PCT.

2.1 Document D1 discloses (see figures 1 and 3; references in parenthesis relating to this document) a dual supply voltage device and corresponding method comprising:

- a core network (Fig. 1: 150) operative at a first supply voltage (V_{DD});
- a control network (Figs. 1 and 3: CONTROLLER 110) coupled to said core network wherein said control network is configured to transmit a control signal (Fig. 3: ENABLE OVERRIDE), said control network comprising:
- an up/down detector (Fig. 3: 310) configured to detect a power state of said core network (col. 4, lines 47-60);
- processing circuitry (Fig. 3: 320) coupled to said up/down detector and configured to generate said control signal based on said power state;
- one feedback circuit (Fig. 3: 330) coupled to said up/ down detector, said feedback circuit configured to provide a feedback signal to adjust a current capacity of said up/down detector (Fig. 3: transistor 330 and 314 both turned on when V_{DD}/POR is high).

The subject-matter of independent claims 1, 10, 20 and 26 consequently lacks novelty against the disclosure of D1 (Article 33(1)-(2) PCT).

2.2 Document D2 discloses (Figure 2) a dual supply voltage device and corresponding method comprising:

- a core network (Fig. 6: COEUR) operative at a first supply voltage (Vdd);
- a control network (Fig. 6: 1; Fig. 2) coupled to said core network wherein said control network is configured to transmit a control signal (Fig. 2: CORE-OFF), said control network comprising:
- an up/down detector (Fig. 2: E1) configured to detect a power state of said core network (paragraph [0025];
- processing circuitry (Fig. 2: E3) coupled to said up/down detector and configured to generate said control signal based on said power state (paragraph [0025]);
- one feedback circuit (Fig. 2: M6) coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector (Fig. 2: transistor M6 and M4 both turned on when V_{dd} is low).

The features of claims 1, 10, 20 and 26 are also anticipated by D2.

3 Dependent claims 2-4, 6-9, 11-13, 15-17, 19, 21-25, 27 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty or inventive step (Article 33(2) and (3) PCT), the reasons being as follows:

- the up/down detectors in both D1 and D2 comprise a first and a second transistor (D1: 312, 314; D2: M4, M5) with the functionality described in claims 2 and 11;
- D2 shows a first feedback transistor (M6) coupled in parallel with the first transistor (M4), as defined in claims 3, 12 and 16, while D1 shows a second feedback transistor (330) in parallel with the second transistor (314) as described in claims 4, 13 and 17;
- D1 discloses a comparator and a buffer (Fig. 3: 320) connected to the output of the up/down detector. The additional features of claim 6 are thus also known from D1;

- an input/output network operative at the higher supply voltage (claim 7) is described in D1 (Fig. 1: Driver 124) and D2 (Fig. 6: 9);
- the feature of claims 8 and 24 is merely one of several straightforward possibilities from which the skilled person would select, in accordance with circumstances, without the exercise of inventive skill, in order to implement an electronic system;
- the invention of claims 9, 19, 25 and 27 consists merely in the use of the circuits described in D1 and D2 in several consumer electronics devices. This use, however, does not involve more than employment of properties of the circuits which are also already known from D1 and D2. Hence, no inventive step is present in the subject-matter of claims 9, 19, 25 and 27;
- the features of claim 15 are implicit functional features of the N- and PMOS transistors comprised in the up/down detectors of D1 and D2;
- the feedback mechanism described in claims 21, 22 and 23 is also realized by the feedback transistors 330 of D1 and M6 of D2.

4 The combination of the features of dependent claims 5, 14, 18 are neither known from, nor rendered obvious by, the available prior art.

Re Item VII

Certain defects in the international application

5 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

Electronic Patent Application Fee Transmittal	
Application Number:	12365559
Filing Date:	04-Feb-2009
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS
First Named Inventor/Applicant Name:	Chang Ki Kwon
Filer:	Nicholas John Pauley/Joann Vachon
Attorney Docket Number:	072302
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	10385483
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Vachon
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	072302
Receipt Date:	24-JUN-2011
Filing Date:	04-FEB-2009
Time Stamp:	17:11:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	3960
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		072302_RCE-IDS_06-24-11.pdf	59719 d063d8e28216b90ac9296c63152534e87bf25bda	yes	5
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Request for Continued Examination (RCE)		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	5	
Warnings:					
Information:					
2	Non Patent Literature	072302_2010_05_08_WO_ISR.pdf	456119 751fc5749b719972edbf32819f6e4cf069de7d21	no	11
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30804 53fb1b98d39b8b3a47516fc728dd7e34b3b0bb50	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	546642		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

23696 7590 06/14/2011

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER
WHITE, DYLAN C

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

TITLE OF INVENTION: MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23696 7590 06/14/2011
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

TITLE OF INVENTION: MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
WHITE, DYLAN C	2819	326-082000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

23696 7590 06/14/2011

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
WHITE, DYLAN C	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 165 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 165 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/365,559	KWON ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/28/2011*.

2. ☒ The allowed claim(s) is/are *1,3-5,7-10 and 12-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Shawki S Ismail/
Supervisory Patent Examiner, Art Unit 2819

DETAILED ACTION

Response to Amendment

The Examiner acknowledges the applicants amendments to claims 1, 10, 16-18, and 20.

Allowable Subject Matter

Claims 1, 3-5, 7-10, 12-25 are allowed. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, A multiple supply voltage device comprising: a core network operative at a first supply voltage; and a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state; one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector; at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; ***at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being***

configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down; at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor, nor would it have been obvious to one of skill in the art. Claims 3-5, and 7-9 are also allowed as being dependent on claim 1.

Regarding claim 10, A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising: detecting a power-on of a second supply voltage while a first supply voltage is already on; ***decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection***; detecting a power-down of said second supply voltage while said first supply voltage is on; ***increasing said current capacity of said power on/off detector in response to said power-down detection;*** receiving a logic-high signal at a control gate of at least one first transistor, at least one second transistor and ***at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor***, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal, nor would it have been obvious to one of skill in the art. Claims 12-19 are also allowed as being dependent on claim 10.

Regarding claim 20, A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said system comprising: means for detecting a power-on of a second supply voltage while a first supply voltage is already on; means, ***responsive to said power-on detection, for decreasing a current capacity of a power on/off detector of said POC network***; means for detecting a power-down of said second supply voltage while said first supply voltage is on; means, ***responsive to said power-down detection, for increasing said current capacity of said power on/off detector***; means for receiving a logic-high signal at a control gate of at least one first transistor at least one second transistor and ***at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor***, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and means for transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal, nor would it have been obvious to one of skill in the art. Claims 21-25 are also allowed as being dependent on claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to power up and power down circuits and their methods of operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Shawki S Ismail/
Supervisory Patent Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/365,559	Applicant(s)/Patent Under Reexamination KWON ET AL.	
	Examiner DYLAN WHITE	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,577,166	06-2003	Lim, Kyu-Nam	327/77
*	B	US-5,723,990	03-1998	Roohparvar, Frankie F.	327/81
*	C	US-2008/0100341	05-2008	Kim, Min-Hwahn	326/63
*	D	US-2006/0044027	03-2006	Chen, Kuan-Yeu	327/143
*	E	US-2008/0218223	09-2008	Kimura, Hiroyuki	327/142
*	F	US-5,781,051	07-1998	Sandhu, Bal S.	327/143
*	G	US-5,495,453	02-1996	Wojciechowski et al.	365/185.18
*	H	US-2009/0027087	01-2009	Sukup et al.	327/72
*	I	US-6,900,666	05-2005	Kursun et al.	326/95
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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BIB DATA SHEET

CONFIRMATION NO. 6210

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/365,559	02/04/2009 RULE	326	2819	072302

APPLICANTS

Chang Ki Kwon, San Diego, CA;
Vivek Mohan, San Diego, CA;

DW

**** CONTINUING DATA ***************************

DW

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

02/12/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /DYLAN C WHITE/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	8	27	4

ADDRESS

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE

Multiple Supply-Voltage Power-Up/Down Detectors

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1674	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6	((power adj2 (up and down)) adj2 detection) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/05 11:57
S1	15	(detect$3 adj2 (power) with (on and off))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:31
S2	80695	(((voltage or power) adj2 (switch$3 or gat $3)) or (head$3 and foot$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:35
S3	41160	((voltage or power) adj (switch$3 or gat$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:36
S4	133254	((voltage or power) adj (detect$3 or (up and down)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:37
S5	2	("7253655").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:38
S6	6	("4859877" | "5381059" | "6172522" | "6233694" | "6498511" | "7116135").PN. OR ("7253655").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:42
S7	46	((voltage or power) adj (detect$3 with ((up and down) or (on and off))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45

S8	195	kwon-chang$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45
S9	19	S8 and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:46
S10	28	mohan-vivek$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:47
S11	5	("20040111649" | "20050117432" | "6611472" | "6650594" | "7372746").PN. OR ("7692998").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:56
S12	12	("4697097" | "5187389" | "5442312" | "5528182" | "5528184").PN. OR ("5781051").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:59
S13	65	("4683382" | "4975883" | "5193198" | "5301161" | "5305275" | "5331599" | "5339272" | "5412331" | "5414669").PN. OR ("5594360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:02
S14	4636	((voltage or power or level) adj (detect$3 or sens$3) with transistor) and feedback	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S15	628	S14 and core	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S16	74	S15 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:11
S17	859	S14 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S18	9901	(POC or (power adj (on adj off) adj control))	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S19	118	S18 and (feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22

S20	513	qualcomm.AS. and (((power or voltage) with control) and feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24
S21	123	qualcomm.AS. and (((power or voltage) with control) with feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24
S23	3959	((voltage or power or level) adj (detect$3 or sens$3) with feedback) and transistor	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S24	472	S23 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S25	0	(11/048260).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:14
S26	1	(10/339069).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:28
S27	5	("5629642" | "5774402" | "6011447" | "6111441").PN. OR ("6744295").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:29
S28	2	("20050140406" | "6163585").PN. OR ("7612588").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:37
S29	7	("5886567" | "5889664" | "6169426" | "6580312" | "6876246" | "7474140").PN. OR ("7605639").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:38
S30	11	("20060119417" | "4565977" | "5535160" | "5877651" | "6130829" | "6304469" | "6522558" | "6756827" | "6812776" | "6977828" | "7042774").PN. OR ("7429883").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:41
S31	11	("6307401" | "6433579" | "6437599" | "6518797" | "6590422" | "6664814" | "6664853" | "6731135" | "6847232").PN. OR ("7183805").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:44

S32	9	("5270584" | "5721510" | "5723990" | "6411157").PN. OR ("6577166").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:49
S33	36	("4961167" | "5189316" | "5315557" | "5337284" | "5557231" | "5602704" | "5633825" | "5673232" | "5856951" | "6031411").PN. OR ("6411157").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:01
S34	18	("5115150" | "5151620" | "5175448" | "5661419" | "5880604" | "6049245" | "6107869" | "6191615" | "6204696" | "6370052" | "6404269" | "6411157" | "6442086" | "6492837" | "6759873").PN. OR ("6900690").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:29
S35	7526	(input and output) and core and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S36	352	S35 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S37	389	(input and output) and (core adj2 voltage) and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S38	49	S37 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S39	0	(power adj ((on and off) or (up and down)) adj detect$3) and core and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:35

S40	9	(power adj ((on and off) or (up and down)) adj detect$3) and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:36
S41	1	(power adj ((on and off) or (up and down)) adj detect$3) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S42	2	(power adj ((on and off) or (up and down)) adj detect$3) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S43	40	("4234920" | "4473759" | "4746822" | "4882506" | "4902910" | "5039875" | "5063304" | "5066869" | "5081625" | "5087834" | "5103115" | "5103159" | "5120993" | "5157270" | "5159206" | "5164613" | "5166545" | "5168209" | "5181203" | "5220534" | "5233161" | "5270977" | "5297261" | "5347173").PN. OR ("6204701").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 15:38
S44	11869	((level or voltage) adj (shift$3 or translat$3)) and (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:40
S45	3036	S44 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S46	2898	S45 and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41

S48	920	((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S49	359	S48 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S51	3322	(((power or voltage) adj2 detect$3) with transistor) and inverter and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S52	930	S51 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S53	1130	(((power or voltage) adj2 detect$3) with transistor) and inverter and current and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S54	295	S53 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S55	5049	((power or (up and down)) adj2 detect$3) and feedback and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S56	405	S55 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S57	336	S56 not S54	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S58	5546	((level or voltage) adj (shift$3 or translat$3)) and feedback and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:49

S59	1712	S58 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:50
S60	430	(((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)) and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:52
S61	644	(((level or voltage) adj (shift$3 or translat$3)) with (feedback)) and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S62	283	S61 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S63	147	S61 and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:01
S64	15	("20020163364" | "20060103437" | "20070030039" | "5130569" | "6646844" | "2007091211").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:39
S66	1875	(voltage level) adj (shift $3 translat$3) and (transistor with series) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:10
S67	602	S66 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:11
S68	4569	(voltage level) adj (shift $3 translat$3) and (transistor with series) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:56
S69	1994	(voltage level) adj (shift $3 translat$3) and (transistor with series) and (feedback with current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:57

S70	918	(voltage level) adj (shift $3 translat$3) and (transistor near2 series) and (feedback with current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58
S71	312	S70 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58
S72	259	S71 not S67	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/03 10:58
S73	78	("3333113" | "4254501" | "4385394" | "4393494" | "4419594" | "4588941" | "4645948" | "4647912" | "4723108" | "4751404" | "4760292" | "4763021" | "4774422" | "4825402" | "4855622" | "4855623" | "4894561" | "4922140" | "4929941" | "4972106" | "4978905" | "4980579" | "5015888" | "5017813" | "5021684" | "5021691" | "5023487" | "5023488" | "5029728" | "5034632" | "5041743" | "5070256" | "5079456" | "5081380" | "5095231" | "5117130" | "5118971" | "5165046" | "5198701" | "5200654" | "5208492" | "5216292" | "5218239" | "5231315" | "5241221" | "5254883" | "5285116" | "5291071" | "5293082" | "5296756" | "5304861" | "5313118" | "5315174" | "5319258" | "5329184" | "5334882" | "5338987").PN. OR	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 14:06

		("5539341").URPN.				
S74	544	(MTCMOS or (power adj gating)) and ((current) with (increas $3 decreas$3))	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:38
S75	96	(MTCMOS or (power adj gating)) and ((current) with (increas $3 decreas$3)) and (transistor near2 series)	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:38
S76	505	(MTCMOS or (power adj gating)) and ((current) with (increas $3 decreas$3)) and (transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:39
S77	277	S76 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:39
S78	237	white-dylan$.XA.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:40
S79	19	("5973541" | "6049231" | "6429689" | "6522171" | "6580293").PN. OR ("6900666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/06/03 15:58

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	39	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2011/06/05 12:14
S50	37	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2010/09/10 09:16
S65	39	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2011/02/13 21:21

6/5/2011 12:15:10 PM
H:\East\Workspaces\12365559.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2010	02/11/2011	06/03/2011						
1	1	✓	✓	=						
-	2	O	-	-						
2	3	O	✓	=						
3	4	O	O	=						
4	5	O	O	=						
-	6	O	-	-						
5	7	✓	✓	=						
6	8	✓	✓	=						
7	9	✓	✓	=						
8	10	✓	✓	=						
-	11	O	-	-						
9	12	O	✓	=						
10	13	O	O	=						
11	14	O	O	=						
12	15	O	✓	=						
13	16	O	O	=						
14	17	O	O	=						
15	18	O	O	=						
16	19	✓	✓	=						
17	20	✓	✓	=						
18	21	✓	✓	=						
19	22	✓	✓	=						
20	23	✓	✓	=						
21	24	✓	✓	=						
22	25	✓	✓	=						
-	26	✓	-	-						
-	27	✓	-	-						

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	**Art Unit**
	DYLAN WHITE	2819

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED									
327	143	H	0	3	L	7 / 00 (2006.0)										
CROSS REFERENCE(S)		H	0	3	L	5 / 00 (2006.0)										
		H	0	3	K	5 / 153 (2006.0)										
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	H	0	3	K	19 / 094 (2006.0)										
327	72	333														
326	68															

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	14	17												
-	2	15	18												
2	3	16	19												
3	4	17	20												
4	5	18	21												
-	6	19	22												
5	7	20	23												
6	8	21	24												
7	9	22	25												
8	10	-	26												
-	11	-	27												
9	12														
10	13														
11	14														
12	15														
13	16														

/DYLAN WHITE/ Examiner.Art Unit 2819	6/3/2011	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	22	
/SHAWKI ISMAIL/ Supervisory Patent Examiner.Art Unit 2819	06/06/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	4

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	All	6/3/2011	DW
327	All	6/3/2011	DW

SEARCH NOTES		
Search Notes	Date	Examiner
See Attached EAST Notes	6/5/2011	DW
Inventor Search	9/9/2010	DW
Assignee Search	9/9/2010	DW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
All	All	6/3/2011	DW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln. No.: 12/365,559 Applicant: Kwon, et al. Filed: February 4, 2009 Examiner: Dylan C. White Art Unit: 2819 Customer No. 23696 Confirm. No.: 6210 Docket No.: 072302	**Certificate of Transmission/Mailing** I hereby certify that this correspondence is being transmitted to the USPTO, transmitted via the Office electronic filing system addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below: Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. 1.111

Sir:

In response to the Office Action dated February 22, 2011, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multiple supply voltage device comprising:

a core network operative at a first supply voltage; and

a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;

one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; ~~and~~

at least one second transistor coupled ~~to~~ in series with the at least one first transistor ~~in series~~ and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

2. (Cancelled)

3. (Previously Presented) The multiple supply voltage device of claim 1 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry, wherein

said one or more first feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

4. (Previously Presented) The multiple supply voltage device of claim 1 wherein said one or more feedback circuits comprise:

one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry, wherein said one or more second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

5. (Previously Presented) The multiple supply voltage device of claim 1 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry; and

one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry;

wherein said one or more first and second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

6. (Cancelled)

7. (Original) The multiple supply voltage device of claim 1 further comprising:

an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal.

8. (Original) The multiple supply voltage device of claim 1, in which the device is integrated into a semiconductor die.

9. (Original) The multiple supply voltage device of claim 8, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

10. (Currently Amended) A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising:

detecting a power-on of a second supply voltage while a first supply voltage is already on;

decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection;

detecting a power-down of said second supply voltage while said first supply voltage is on;

increasing said current capacity of said power on/off detector in response to said power-down detection;

receiving a logic-high signal at a control gate of at least one first transistor, ~~and~~ at least one second transistor and at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and

transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal.

11. (Cancelled)

12. (Previously Presented) The method of claim 10 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching off said one or more first feedback transistors in response to said first feedback signal.

13. (Previously Presented) The method of claim 10 wherein said decreasing said current capacity comprises:

receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

14. (Previously Presented) The method of claim 10 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;

switching off said one or more first feedback transistors in response to said first feedback signal;

receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

15. (Original) The method of claim 10 wherein said detecting said power-down comprises:

receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and

transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

16. (Currently Amended) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a ~~third~~ first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching on said one or more first feedback transistors in response to said ~~third~~ first feedback signal.

17. (Currently Amended) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a ~~fourth~~ second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said ~~fourth~~ second feedback signal.

18. (Currently Amended) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a ~~third~~ first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;

switching on said one or more first feedback transistors in response to said ~~third~~ first feedback signal;

receiving a ~~fourth~~ second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said ~~fourth~~ second feedback signal.

19. (Original) The method of claim 10, wherein the multiple supply voltage device is applied in an electronic device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device,

personal digital assistant (PDA), fixed location data unit, and a computer, into which a semiconductor device is integrated.

20. (Currently Amended) A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said system comprising:

means for detecting a power-on of a second supply voltage while a first supply voltage is already on;

means, responsive to said power-on detection, for decreasing a current capacity of a power on/off detector of said POC network;

means for detecting a power-down of said second supply voltage while said first supply voltage is on;

means, responsive to said power-down detection, for increasing said current capacity of said power on/off detector;

means for receiving a logic-high signal at a control gate of at least one first transistor, ~~and~~ at least one second transistor and at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and

means for transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal.

21. (Original) The system of claim 20 further comprising:

means for providing a feedback signal associated with at least one of: said detected power-on or said detected power-down, wherein said feedback signal is used in said means for decreasing and said means for increasing.

22. (Original) The system of claim 21 wherein said means for decreasing said current capacity comprises:

means, responsive to said feedback signal, for switching off one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

23. (Original) The system of claim 21 wherein said means for increasing said current capacity comprises:

means, responsive to said feedback signal, for switching on one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

24. (Original) The multiple supply voltage device of claim 20, in which the device is integrated into a semiconductor die.

25. (Original) The multiple supply voltage device of claim 24, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

26. - 27. (Cancelled)

REMARKS

Claims 1, 3-5, 7-10, and 12-25 are pending in the present application. Claims 2, 6, 11, 26 and 27 are previously canceled. Independent claims 1, 10, 16-18 and 20 are currently amended. Applicant respectfully submits that no new matter is added by the present amendment. Support for the claim amendments can be found in the original specification and drawings, for example in Figures 4 - 6.

Claim Objections

Claims 16-18 are objected to for informalities because the claims reference third and fourth feedback signals which the Examiner asserted are not in an embodiment shown in the drawings. Applicant respectfully submits that the embodiments claimed in claims 16-18 recite the "third feedback signals" and "fourth feedback signals" to distinguish "first feedback signals" and "second feedback signals" respectively that are recited in other claims. The third and fourth feedback signals are asserted on the same conductive paths as the first and second feedback signals on a different occasion, thus they are indeed disclosed in Figure 6, for example. Claims 16-18 do not recite that four separate feedback signals could be simultaneously asserted. Nonetheless, to avoid confusion, claims 16 to 18 are currently amended to label the "third" as "first" and "fourth" as "second" to describe the claimed feedback signals. None of the intervening claims recite a first or second feedback signal, so this change in nomenclature should overcome the informal objection without inadvertently affecting the claim scope. Reconsideration is respectfully requested.

Claim Rejections – 35 USC §102

Claims 1, 3,10, 12, 15 and 20-23 are rejected under 35 USC § 102 as being anticipated by U.S. Patent No. 5,723,990 to Roohpavar. Applicants have amended independent claims 1, 10 and 20 to recite "at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor." Applicant respectfully submits that in view of the present amendment, Roohpaver does not teach or suggest each element of any of the claims. This amendment does not add new matter because each embodiment of the application that is

shown in Figures 4 -6 includes at least three transistors in series with each other and having a commonly connected gate. For example, the at least one third transistor could be either M5 or M6 both according to the amended claims. Roohpaver does not teach or suggest a third transistor configured in series between the claimed at least one first transistor and the claimed at least one second transistor. For at least these reasons, Applicant respectfully submits that the rejection under 35 U.S.C. §102 has been overcome. Reconsideration is respectfully requested.

Claim Rejections – 35 USC §103

Claims 7-9, 19, 24 and 25 are rejected under 35 USC § 103 over U.S. Patent No. 5,723,990 to Roohpavar in view of U.S. Patent No. 6,577,166 to Lim. Applicants respectfully submit that the current amendments to independent claims 1, 10 and 20 overcome the rejections under 35 U.S.C. §103 for the reasons set forth above because no combination of Roohpavar and Lim teaches or suggests "at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor" as claimed. Reconsideration is respectfully requested.

Allowable Subject Matter

Applicant gratefully acknowledges the Examiner's indication that original claims 4, 5, 13 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicant respectfully submits that the current amendments should render each of the claims allowable in their present form. Further, Applicant submits that the current amendments to independent claims 1 and 10 should not detract from the allowability of claims 4, 5, 13 and 14. Reconsideration is respectfully requested.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: March 25, 2011

By: / Sam Talpalatsky /

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Electronic Acknowledgement Receipt	
EFS ID:	9747741
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	Multiple Supply-Voltage Power-Up/Down Detectors
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Vachon
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	072302
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	072302_OAR_03-28-11.pdf	126328 b55ccc6b516824e35c873cd3f2945eca15998060	no	11
Warnings:					
Information:					

Total Files Size (in bytes):	126328

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/365,559	02/04/2009	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/28/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 27	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***4	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JACQULYN L. WILLIAMS/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

23696 7590 02/22/2011

QUALCOMM INCORPORATED
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EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
02/22/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	12/365,559	KWON ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *2,6,11,26 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-10,12,15 and 19-25* is/are rejected.

7)☒ Claim(s) *4,5,13,14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/8/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Examiner acknowledges the applicants arguments with respect to claims 1, 3-5, 10, 12-14, and 20, as well as the cancellation of claims 2, 6, 11, 26 and 27.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

The indicated allowability of claims 2 and 11 which have been incorporated into claims 1, 10, and 20 has been withdrawn in view of the newly discovered reference(s) to Roohparvar (U.S. Pat. 5,723,990). Rejections based on the newly cited reference(s) follow.

Claim Objections

Claims 16-18 are objected to because of the following informalities: the claims reference third and/or fourth feedback signals from one of the signal processor or the output buffer of the POC network. The drawings do not disclose an embodiment of the invention in which there are third and fourth feedback signals to control one or more of the first and second transistors. The Examiner notes that this objection was in the first

Office Action was not addressed in the claim amendments or the applicants remarks.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 10, 12, 15, and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Roohparvar (U.S. Pat. 5,723,990).

Regarding claim 1, Roohparvar discloses a core network operative at a first supply voltage (voltage of enable signal @ Fig. 1); and a control network (Fig. 1) coupled to the core network wherein the control network is configured to transmit a control signal (HV detector output), the control network comprising: an up/down detector (transistors 6, 8, 10, and 21) configured to detect a power state of said core network (enable signal) ;processing circuitry (transistors 14 and 16, and logic 20) coupled to the up/down detector (transistors 6, 8, 10 and 21) and configured to generate the control signal (HV detector output) based on the power state (high/low; of enable signal); and one or more feedback circuits (transistors 14, 16, and 18) coupled to the up/down detector (transistors 6, 8, 10 and 21), the one or more feedback circuits (transistor 18) configured to provide feedback signals from node 24 to transistors 18) to adjust a current capacity (additional transistor 18) of said up/down detector (transistors 6, 8, 10

and 21); at least one first transistor (21) coupled to a second supply voltage (Vcc), the at least one more first transistor (21) being configured to switch on (conducting) when the first supply voltage (voltage of enable signal) is powered down (low/off) and to switch off (not conducting) when the first supply voltage is powered on (high/on); and at least one second transistor (6) coupled to the at least one first transistor (21) in series and coupled to the first supply voltage (voltage of enable signal), the at least one second transistor (6) being configured to switch on (conducting) when the first supply voltage is powered on (high/ on) and to switch off when the first supply voltage is powered down (low/off).

Regarding claim 3, Roohparvar discloses one or more first feedback transistors (18) coupled in parallel with the one or more first transistors (21) and coupled to receive feedback from the processing circuitry (transistors 14 and 16, and logic 20), wherein the one or more first feedback transistors (18) are configured to switch off (not conducting) when the processing circuitry (transistors 14 and 16, and logic 20) indicates that the first supply voltage (voltage of enable signal) is powered on (high/on).

Regarding claim 10, Roohparvar discloses detecting a power-on of a second supply voltage (voltage of enable signal @ Fig. 1) while a first supply voltage (Vcc) is already on; decreasing a current capacity (via transistor 18) of a power on/off detector (transistors 6, 8, 10 and 21) of said POC network in response to said power-on detection (col. 1, lines 64-67); detecting a power-down of the second supply voltage

(voltage of enable signal) while the first supply voltage (Vcc) is on; and increasing the current capacity (via transistor 18) of the power on/off detector (transistors 6, 8, 10 and 21) in response to said power-down detection (of enable signal); receiving a logic-high signal (logic high) at a control gate of at least one first transistor (21) and at least one second transistor (6), the at least one first transistor (21) being configured to switch off (not conducting) in response to the logic-high signal (logic high), and the at least one second transistor (6) being configured to switch on (conducting) in response to the logic-high signal (logic high); and transmitting a detection signal (at node 22) to a signal processor (transistors 14 and 16, and logic 20) from the at least one second transistor (6) based on said received logic-high signal (logic high).

Regarding claim 12, Roohparvar discloses receiving a first feedback signal (from node 24) from the signal processor (transistors 14 and 16, and logic 20) at one or more first feedback transistors (18) coupled in parallel with the one or more first transistors (21); and switching off (not conducting) the one or more first feedback transistors (18) in response to the first feedback signal (from node 24).

Regarding claim 15, Roohparvar discloses receiving a logic-low signal (logic 0) at the control gate of said one or more first (21) and second transistors (6), wherein the one or more first transistors (21) are configured to switch on (conducting) in response to the logic-low signal (logic 0), and wherein the one or more second transistors (6) are configured to switch off (not conducting) in response to said logic-low signal (logic 0);

and transmitting a detection signal (at node 22) to a signal processor (transistors 14 and 16, and logic 20) from the one or more first transistors (21) based on the received logic-low signal (logic 0).

Regarding claim 20, Roohparvar discloses means for detecting a power-on (transistors 6, 8, 10, and 21) of a second supply voltage (voltage of enable signal) while a first supply voltage (Vcc) is already on; means, responsive to the power-on detection (transistors 6, 8, 10, and 21), for decreasing a current capacity (via transistor 18) of a power on/off detector of the POC network; means for detecting a power-down (logic 0/off) of the second supply voltage (voltage of enable signal) while the first supply voltage (Vcc) is on; and means, responsive to the power-down detection (transistors 6, 8, 10, and 21), for increasing the current capacity (via transistor 18) of the power on/off detector (transistors 6, 8, 10, and 21); means for receiving a logic-high signal (logic 1) at a control gate of at least one first transistor (21) and at least one second transistor (6), the at least one first transistor (21) being configured to switch off (not conducting) in response to the logic-high signal (logic 1)(6), and the at least one second transistor (6) being configured to switch on (conducting) in response to the logic-high signal (logic 1); and means for transmitting a detection signal (via node 22)to a signal processor (transistors 14 and 16, and logic 20) from the at least one second transistor (6) based on the received logic-high signal (logic 1).

Regarding claim 21, Roohparvar discloses means for providing a feedback signal (via node 24) associated with at least one of: said detected power-on or said detected power-down (of enable signal voltage), wherein the feedback signal (via node 24) is used in the means for decreasing (turning off transistor 18)and the means for increasing (turning on transistor 18).

Regarding claim 22, Roohparvar discloses means, responsive to the feedback signal (via node 24), for switching off (not conducting) one or more transistors of a plurality of transistors (18), wherein the plurality of transistors define the current capacity (transistors 18 and 21) of said power on/off detector (transistors 6, 8, 10, and 21).

Regarding claim 23, Roohparvar discloses means, responsive to the feedback signal (via node 24), for switching on one or more transistors (18) of a plurality of transistors (18 and 21), wherein the plurality of transistors define the current capacity of said power on/off detector (transistors 6, 8, 10, and 21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar (U.S. Pat. 5,723,990) in view of Lim (U.S. Pat. 6,577,166).

Regarding claim 7, Roohparvar discloses that of claim 1, but fails to disclose an I/O network.

Lim discloses an input/output (I/O) network (memory output) operative at a second supply voltage (Vint), wherein the I/O network (output) is coupled to the core network (memory core) and the control network (Fig. 10), and wherein the I/O network (output) is configured to receive the control signal (Vpps; col. 1, lines 50-56), therefore it would have been obvious to one of skill in the art to use the voltage detection circuit disclosed by Roohparvar with the I/O network taught by Lim to stabalize output voltages through voltage level detection.

Regarding claims 8 and 24, the combination discloses in which the device (Fig. 10) is integrated into a semiconductor die (Lim; semiconductor memory device).

Regarding claims 9, 19, and 25, the combination discloses in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer (col. 8, lines 54-59, devices which use batteries).

Allowable Subject Matter

Claims 4, 5, 13, and 14, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 4, wherein said one or more feedback circuits comprise: one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry, wherein said one or more second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

Regarding claim 5, wherein said one or more feedback circuits comprise:
one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry; and one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry; wherein said one or more first and second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

Regarding claim 13, receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and switching off said one or more second feedback transistors in response to said second feedback signal.

Regarding claim 14, receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; switching off said one or more first feedback transistors in response to said first feedback signal; receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and switching off said one or more second feedback transistors in response to said second feedback signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refer to voltage or power detection circuitry and their methods of operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2819

/Dylan White/
Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/365,559	Applicant(s)/Patent Under Reexamination KWON ET AL.	
	Examiner DYLAN WHITE	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,577,166	06-2003	Lim, Kyu-Nam	327/77
*	B	US-5,723,990	03-1998	Roohparvar, Frankie F.	327/81
*	C	US-2008/0100341	05-2008	Kim, Min-Hwahn	326/63
*	D	US-2006/0044027	03-2006	Chen, Kuan-Yeu	327/143
*	E	US-2008/0218223	09-2008	Kimura, Hiroyuki	327/142
*	F	US-5,781,051	07-1998	Sandhu, Bal S.	327/143
*	G	US-5,495,453	02-1996	Wojciechowski et al.	365/185.18
*	H	US-2009/0027087	01-2009	Sukup et al.	327/72
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2010	02/11/2011	02/13/2011						
	1	✓	✓							
	2	O	-							
	3	O	✓							
	4	O	O							
	5	O	O							
	6	O	-							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	O	-							
	12	O	✓							
	13	O	O							
	14	O	O							
	15	O	✓							
	16	O	O							
	17	O	O							
	18	O	O							
	19	✓	✓							
	20	✓	✓							
	21	✓	✓							
	22	✓	✓							
	23	✓	✓							
	24	✓	✓							
	25	✓	✓							
	26	✓	-							
	27	✓	-							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	All	2/11/2011	DW
327	All	2/11/2011	DW

SEARCH NOTES		
Search Notes	Date	Examiner
See Attached EAST Notes	2/11/2011	DW
Inventor Search	9/9/2010	DW
Assignee Search	9/9/2010	DW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
All	All	2/11/2011	DW

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CONFIRMATION NO. 6210

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/365,559	02/04/2009 RULE	326	2819	072302

APPLICANTS

Chang Ki Kwon, San Diego, CA;
Vivek Mohan, San Diego, CA;

DW

**** CONTINUING DATA ***************************

DW

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

02/12/2009

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/DYLAN C WHITE/ Examiner's Signature	Initials	CA	8	27	4

ADDRESS

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE

Multiple Supply-Voltage Power-Up/Down Detectors

FILING FEE RECEIVED		
1674	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	15	(detect$3 adj2 (power) with (on and off))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:31
S2	80695	(((voltage or power) adj2 (switch$3 or gat $3)) or (head$3 and foot$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:35
S3	41160	((voltage or power) adj (switch$3 or gat$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:36
S4	133254	((voltage or power) adj (detect$3 or (up and down)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:37
S5	2	("7253655").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:38
S6	6	("4859877" | "5381059" | "6172522" | "6233694" | "6498511" | "7116135").PN. OR ("7253655").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:42
S7	46	((voltage or power) adj (detect$3 with ((up and down) or (on and off))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45
S8	195	kwon-chang$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45

S9	19	S8 and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:46
S10	28	mohan-vivek$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:47
S11	5	("20040111649" | "20050117432" | "6611472" | "6650594" | "7372746").PN. OR ("7692998").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:56
S12	12	("4697097" | "5187389" | "5442312" | "5528182" | "5528184").PN. OR ("5781051").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:59
S13	65	("4683382" | "4975883" | "5193198" | "5301161" | "5305275" | "5331599" | "5339272" | "5412331" | "5414669").PN. OR ("5594360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:02
S14	4636	((voltage or power or level) adj (detect$3 or sens$3) with transistor) and feedback	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S15	628	S14 and core	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S16	74	S15 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:11
S17	859	S14 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S18	9901	(POC or (power adj (on adj off) adj control))	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S19	118	S18 and (feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S20	513	qualcomm.AS. and (((power or voltage) with control) and feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24

S21	123	qualcomm.AS. and (((power or voltage) with control) with feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24
S23	3959	((voltage or power or level) adj (detect$3 or sens$3) with feedback) and transistor	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S24	472	S23 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S25	0	(11/048260).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:14
S26	1	(10/339069).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:28
S27	5	("5629642" | "5774402" | "6011447" | "6111441").PN. OR ("6744295").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:29
S28	2	("20050140406" | "6163585").PN. OR ("7612588").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:37
S29	7	("5886567" | "5889664" | "6169426" | "6580312" | "6876246" | "7474140").PN. OR ("7605639").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:38
S30	11	("20060119417" | "4565977" | "5535160" | "5877651" | "6130829" | "6304469" | "6522558" | "6756827" | "6812776" | "6977828" | "7042774").PN. OR ("7429883").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:41
S31	11	("6307401" | "6433579" | "6437599" | "6518797" | "6590422" | "6664814" | "6664853" | "6731135" | "6847232").PN. OR ("7183805").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:44
S32	9	("5270584" | "5721510" | "5723990" | "6411157").PN. OR ("6577166").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:49

S33	36	("4961167" | "5189316" | "5315557" | "5337284" | "5557231" | "5602704" | "5633825" | "5673232" | "5856951" | "6031411").PN. OR ("6411157").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:01
S34	18	("5115150" | "5151620" | "5175448" | "5661419" | "5880604" | "6049245" | "6107869" | "6191615" | "6204696" | "6370052" | "6404269" | "6411157" | "6442086" | "6492837" | "6759873").PN. OR ("6900690").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:29
S35	7526	(input and output) and core and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S36	352	S35 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S37	389	(input and output) and (core adj2 voltage) and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S38	49	S37 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S39	0	(power adj ((on and off) or (up and down)) adj detect$3) and core and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:35
S40	9	(power adj ((on and off) or (up and down)) adj detect$3) and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:36

S41	1	(power adj ((on and off) or (up and down)) adj detect$3) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S42	2	(power adj ((on and off) or (up and down)) adj detect$3) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S43	40	("4234920" | "4473759" | "4746822" | "4882506" | "4902910" | "5039875" | "5063304" | "5066869" | "5081625" | "5087834" | "5103115" | "5103159" | "5120993" | "5157270" | "5159206" | "5164613" | "5166545" | "5168209" | "5181203" | "5220534" | "5233161" | "5270977" | "5297261" | "5347173").PN. OR ("6204701").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 15:38
S44	11869	((level or voltage) adj (shift$3 or translat$3)) and (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:40
S45	3036	S44 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S46	2898	S45 and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S48	920	((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41

S49	359	S48 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S51	3322	(((power or voltage) adj2 detect$3) with transistor) and inverter and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S52	930	S51 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:04
S53	1130	(((power or voltage) adj2 detect$3) with transistor) and inverter and current and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S54	295	S53 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:06
S55	5049	((power or (up and down)) adj2 detect$3) and feedback and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S56	405	S55 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S57	336	S56 not S54	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 08:09
S58	5546	((level or voltage) adj (shift$3 or translat$3)) and feedback and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:49
S59	1712	S58 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:50

S60	430	(((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)) and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:52
S61	644	(((level or voltage) adj (shift$3 or translat$3)) with (feedback)) and transistor and inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S62	283	S61 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 10:53
S63	147	S61 and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:01
S64	15	("20020163364" | "20060103437" | "20070030039" | "5130569" | "6646844" | "2007091211").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/02/11 15:39

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	39	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2011/02/13 21:21
S50	37	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2010/09/10 09:16

2/13/2011 9:22:09 PM
H:\East\Workspaces\12365559.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12365559
	Filing Date	2009-02-04
	First Named Inventor	Chang Ki Kwon
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/DW/	1	6646844		2003-11-11	MATTHEWS LLOYD P	
/DW/	2	5130569		1992-07-14	GLICA STEPHEN J	
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/DW/	1	20020163364		2002-11-07	MAJCHERCZAK SYLVAIN	
/DW/	2	20070030039		2007-02-08	CHEN KER-MIN	
/DW/	3	20060103437		2006-05-18	KANG KHIL O	
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

Receipt date: 09/08/2010	Application Number	12365559 12365559 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-02-04
	First Named Inventor	Chang Ki Kwon
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

/DW/	1	2007091211	WO		2007-08-16	NXP BV		☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	~~INTERNATIONAL SEARCH REPORT-PCT/US2010/23081, INTERNATIONAL SEARCH AUTHORITY-EUROPEAN PATENT OFFICE-05-AUGUST-2010~~	☐
	2	~~WRITTEN OPINION-PCT/US2010/023081, INTERNATIONAL SEARCH AUTHORITY-EUROPEAN PATENT OFFICE-05-AUGUST-2010~~	☐

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EXAMINER SIGNATURE

Examiner Signature	/Dylan White/	Date Considered	02/11/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln. No.: 12/365,559 Applicant: Kwon, et al. Filed: February 4, 2009 Examiner: Dylan C. White Art Unit: 2819 Customer No. 23696 Confirm. No.: 6210 Docket No.: 072302	**Certificate of Transmission/Mailing** I hereby certify that this correspondence is being transmitted to the USPTO, transmitted via the Office electronic filing system addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below: Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. 1.111

Sir:

In response to the Office Action dated September 16, 2010, please amend the above-identified application as follows:

Amendments to the Specification are reflected in the replacement paragraphs beginning on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.

Amendments to the Specification:

Please delete the unnumbered paragraph beneath paragraph [0024] of the application as filed. A marked up version of the deleted paragraph is shown below.

~~FIG. 8 is a diagram illustrating an exemplary wireless communication system.~~

Please replace paragraphs [0037] - [0038] of the application (paragraphs [0038] and [0039] of the publication) with the following replacement paragraphs which are marked up to show changes relative to the immediate prior version.

[0038] ~~FIG. 8 is a diagram illustrating an exemplary wireless communication system. In some~~ Some embodiments of an exemplary wireless communication system~~, a system 800~~ include~~s~~ multiple remote units ~~820-824~~ and multiple base stations ~~850-852~~. It can be recognized that typical wireless communication systems may have many more remote units and base stations. The remote units ~~820-824~~ include multiple semiconductor devices ~~830-834~~ having power detection, as discussed above. ~~FIG. 8 shows a~~ Embodiments include forward link signals ~~880~~ from the base stations ~~850-852~~ and the remote units ~~820-824~~ and ~~a~~ reverse link signals ~~890~~ from the remote units ~~820-824~~ to the base stations ~~850-852~~.

[0039]In other embodiments, ~~FIG. 8 the~~ a remote unit ~~820~~ is ~~shown as~~ a mobile telephone, ~~the~~ another remote unit ~~822~~ is ~~shown as~~ a portable computer, and ~~the~~ another remote unit ~~824~~ is ~~shown as~~ a fixed location remote unit in a wireless local loop system. For example, the remote units may be mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, navigation devices (e.g., GPS enabled devices,) set-top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Although ~~FIG. 8~~ these embodiments illustrate~~s~~ remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. The disclosed device may be suitably employed in any device which includes a semiconductor device.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multiple supply voltage device comprising:

a core network operative at a first supply voltage; and

a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising:an up/down (up/down) detector configured to detect a power state of said core network;processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state; ~~and~~

one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; and

at least one second transistor coupled to the at least one first transistor in series and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down.

2. (Cancelled)

3. (Currently Amended) The multiple supply voltage device of claim [2] 1 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry, wherein said one or more first feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

4. (Currently Amended) The multiple supply voltage device of claim [2] 1 wherein said one or more feedback circuits comprise:

one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry, wherein said one or more second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

5. (Currently Amended) The multiple supply voltage device of claim [2] 1 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry; andone or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry;wherein said one or more first and second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

6. (Cancelled)

7. (Original) The multiple supply voltage device of claim 1 further comprising:

an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal.

8. (Original) The multiple supply voltage device of claim 1, in which the device is integrated into a semiconductor die.

9. (Original) The multiple supply voltage device of claim 8, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

10. (Currently Amended) A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising:

detecting a power-on of a second supply voltage while a first supply voltage is already on;

decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection;

detecting a power-down of said second supply voltage while said first supply voltage is on; ~~and~~

increasing said current capacity of said power on/off detector in response to said power-down detection;

receiving a logic-high signal at a control gate of at least one first transistor and at least one second transistor, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and

transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal.

11. (Cancelled)

12. (Currently Amended) The method of claim ~~11~~ 10 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching off said one or more first feedback transistors in response to said first feedback signal.

13. (Currently Amended) The method of claim ~~11~~ 10 wherein said decreasing said current capacity comprises:

receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

14. (Currently Amended) The method of claim ~~11~~ 10 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;

switching off said one or more first feedback transistors in response to said first feedback signal

;receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

15. (Original) The method of claim 10 wherein said detecting said power-down comprises:

receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and

transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

16. (Original) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a third feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching on said one or more first feedback transistors in response to said third feedback signal.

17. (Original) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a fourth feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said fourth feedback signal.

18. (Original) The method of claim 15 wherein said increasing said current capacity comprises:

receiving a third feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;switching on said one or more first feedback transistors in response to said third feedback signal;

receiving a fourth feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said fourth feedback signal.

19. (Original) The method of claim 10, wherein the multiple supply voltage device is applied in an electronic device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer, into which a semiconductor device is integrated.

20. (Currently Amended) A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said system comprising:

means for detecting a power-on of a second supply voltage while a first supply voltage is already on;

means, responsive to said power-on detection, for decreasing a current capacity of a power on/off detector of said POC network;

means for detecting a power-down of said second supply voltage while said first supply voltage is on; ~~and~~

means, responsive to said power-down detection, for increasing said current capacity of said power on/off detector;

means for receiving a logic-high signal at a control gate of at least one first transistor and at least one second transistor, the at least one first transistor being configured to switch off in response to said logic-high signal, and the at least one second transistor being configured to switch on in response to said logic-high signal; and

means for transmitting a detection signal to a signal processor from the at least one second transistor based on said received logic-high signal.

21. (Original) The system of claim 20 further comprising:

means for providing a feedback signal associated with at least one of: said detected power-on or said detected power-down, wherein said feedback signal is used in said means for decreasing and said means for increasing.

22. (Original) The system of claim 21 wherein said means for decreasing said current capacity comprises:

means, responsive to said feedback signal, for switching off one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

23. (Original) The system of claim 21 wherein said means for increasing said current capacity comprises:

means, responsive to said feedback signal, for switching on one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

24. (Original) The multiple supply voltage device of claim 20, in which the device is integrated into a semiconductor die.

25. (Original) The multiple supply voltage device of claim 24, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

26. - 27. (Cancelled)

REMARKS

Claims 1, 3-5, 7-10, and 12-25 are pending in the present application. Claims 2, 6, 11, 26 and 27 have been canceled. Independent claims 1 and 10 are presently amended to claim the subject matter of original claims 2 and 11 which the Examiner has deemed allowable. Independent claim 20 is presently amended to means for performing the method of original claim 11 which the Examiner has deemed allowable. Applicant respectfully submits that no new matter is added by the present amendment. Support for the new claims and amendments can be found in the original claims, for example.

Drawings

The drawings are objected to because Figure 8 was not filed with the original disclosure. The present amendments to the specification remove all references to Figure 8. Applicant respectfully submits that the present amendments to the specification overcome the drawing objections by rendering them moot. Reconsideration is respectfully requested.

Claim Objections

Claims 6 is objected to for lack of support in the specification or drawings. The objection to claim 6 is moot in view of the current cancellation of claim 6.

Claim Rejections – 35 USC § 112

Claims 26 and 27 are rejected under 35 U.S.C. §112 second paragraph for indefiniteness. ort in the specification or drawings. The rejection of claims 26 and 27 are moot in view of the current cancellation of claims 26 and 27.

Claim Rejections – 35 USC §102

Claims 1, 7-10, and 19-25 are rejected under 35 USC § 102 as being anticipated by U.S. Patent No. 6,577,166 to Lim. Applicants have amended the above claims to overcome the rejection of claims 1, 7-10 and 19 by amending the elements of claim 2, which the Examiner has deemed allowable into independent claim 1, and by amending the elements of claim 11, which the Examiner has deemed allowable into independent claim 10. Applicant respectfully submits

that the rejection of claims 20 - 25 are also overcome by amending independent claim 20 to include means for performing the steps of claim 11 which the Examiner has deemed allowable. Reconsideration is respectfully requested.

Allowable Subject Matter

Applicant gratefully acknowledges the Examiner's indication that original claims 2 - 5 and 11 - 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant respectfully submits that independent claim 1 is amended to include all of the limitations of original claim 2, and independent claim 10 is amended to include all of the limitations of original claim 11. Independent claim 20 is also amended to include means for performing the steps of independent claim 11. Applicant respectfully submits that each of the pending claims are in condition for allowance. Reconsideration is respectfully requested.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: December 2, 2010

By: / Sam Talpalatsky /
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Electronic Acknowledgement Receipt

EFS ID:	8959057
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	Multiple Supply-Voltage Power-Up/Down Detectors
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Vachon
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	072302
Receipt Date:	03-DEC-2010
Filing Date:	04-FEB-2009
Time Stamp:	07:51:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	072302_OAR_12-03-10.pdf	120791 0c2ab02e1aad7d64931981c0c9bd2f2162775a1c	no	12

Warnings:	
Information:	

Total Files Size (in bytes):	120791

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/365,559	02/04/2009	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	12/03/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 22	Minus	** 27	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/PATRICIA F. LEWIS/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/365,559	02/04/2009	Chang Ki Kwon	072302	6210

23696 7590 09/16/2010

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
09/16/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	12/365,559	KWON ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-10 and 19-27* is/are rejected.

7)☒ Claim(s) *2-6 and 11-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2009* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/4/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because Figure 8 was not filed with the original disclosure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the processing

circuitry comprising a comparator" (per claim 6) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 6 is objected to because of the following informalities: there is not support in the specification or the drawings for the limitations of claim 6 "the processing circuitry comprising a comparator configured to output a detection signal based on an input

signal received from said adjustable current power up/down detector". Appropriate correction is required.

Claims 16-18 are objected to because of the following informalities: the claims reference third and/or fourth feedback signals from one of the signal processor or the output buffer of the POC network. The drawings do not disclose an embodiment of the invention in which there are third and fourth feedback signals to control on or more of the first and second transistors.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 26 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 26, the language states “detecting a power-on of a second supply voltage while a first supply is already on; decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection; detecting a power-down of said second supply voltage while said first supply voltage is on; and increasing said current capacity of said power on/off detector in response to said power-down detection”.

The Examiner believes the claims to be indefinite because the applicant's invention does not decrease a current capacity in response to the power-on detection. The applicant's invention (Fig. 6) discloses where Vcore is detected on and the transistors M6, M7, and M10 begin conducting. The inverting signal processor circuit then inverts the low signal at the input to a high signal at the output which turns transistor M8 off, however since transistors M4 and M5 are already turned off with Vcore signal being high there is no decrease in current capacity because transistors M4 and M5 have already been turned off and there is no current flowing through them.

Regarding claim 27, it is rejected as being a dependent of claim 26.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-10, and 19-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim (U.S. Pat. 6,577,166).

Regarding claim 1, Lim discloses a core network (memory core; col. 1, lines 16-21) operative at a first supply voltage (Vpp @ Fig. 10); and a control network coupled to the core network wherein the control network (Fig. 10) is configured to transmit a control signal (Vpps), the control network comprising: an up/down detector (P6, N11, N13)

configured to detect a power state of the core network signal (Vpp); processing circuitry (AMP1) coupled to the up/down detector (P6, N11, N13) and configured to generate the control signal (Vpps) based on said power state (on or off); and one or more feedback circuits (N12) coupled to the up/down detector (P6, N11, N13), the one or more feedback circuits (N12) configured to provide feedback signals (from Vout1 node) to adjust a current capacity (transistor N12 conducting or not) of said up/down detector (P6, N11, N13).

Regarding claim 7, Lim discloses an input/output (I/O) network (memory output) operative at a second supply voltage (Vint), wherein the I/O network (output) is coupled to the core network (memory core) and the control network (Fig. 10), and wherein said I/O network (output) is configured to receive the control signal (Vpps; col. 1, lines 50-56).

Regarding claim 8, Lim discloses in which the device (Fig. 10) is integrated into a semiconductor die (semiconductor memory device).

Regarding claim 9, Lim discloses in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer (col. 8, lines 54-59; devices which use batteries).

Regarding claim 10, Lim discloses detecting a power-on of a second supply voltage (Vpp) while a first supply voltage is already on (Vint); decreasing a current capacity (by turning off transistor N12) of a power on/off detector (P6, N11-N13) of the POC network (Fig. 10) in response to said power-on detection (of voltage Vpp); detecting a power-down of the second supply voltage (Vpp) while the first supply voltage is on (Vint); and increasing the current capacity (turning on transistor N12) of the power on/off detector (P6, N11-N13) in response to the power-down detection (Fig. 10).

Regarding claim 19, Lim discloses wherein the multiple supply voltage device is applied in an electronic device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer, into which a semiconductor device is integrated (col. 8, lines 54-59; devices which use batteries).

Regarding claim 20, Lim discloses means for detecting (N11) a power-on of a second supply voltage (Vpp) while a first supply voltage (Vint) is already on; means (Amp1), responsive to the power-on detection, for decreasing a current capacity (N12 not conducting) of a power on/off detector (P6, N11, N13) of said POC network (Fig. 10); means for detecting (N11) a power-down of the second supply voltage (Vpp) while the first supply voltage is on (Vint); and means, responsive to the power-down detection

(P6, N11, N13), for increasing said current capacity (N12 conducting) of said power on/off detector (P6, N11, N13).

Regarding claim 21, Lim discloses means for providing a feedback signal (at node 306) associated with at least one of: the detected power-on or the detected power-down (P6, N11, N13), wherein the feedback signal (node 306) is used in the means for decreasing (N12 not conducting) and the means for increasing (N12 conducting).

Regarding claim 22, Lim discloses wherein the means for decreasing the current capacity (N12 not conducting) comprises: means, responsive to the feedback signal (from node 306), for switching off one or more transistors (N12) of a plurality of transistors, wherein the plurality of transistors define the current capacity (N12 conducting) of the power on/off detector (P6, N11, N13).

Regarding claim 23, Lim discloses wherein the means for increasing the current capacity (N12 conducting) comprises: means, responsive to the feedback signal (from node 306), for switching on (N12 conducting) one or more transistors of a plurality of transistors (N12 & N13), wherein the plurality of transistors define the current capacity of said power on/off detector (P6, N11, N13).

Regarding claim 24, Lim discloses in which the device is integrated into a semiconductor die (semiconductor memory device).

Regarding claim 25, Lim discloses in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer integrated (col. 8, lines 54-59; devices which use batteries).

Allowable Subject Matter

Claims 2-5 and 11-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 2, wherein said up/down detector comprises: one or more first transistors coupled to a second supply voltage, wherein said one or more first transistors are configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; and one or more second transistors coupled to said one or more first transistors in series and coupled to said first supply voltage, wherein said one or more second transistors are configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down.

Regarding claims 3-5, as being dependent on claim 2.

Regarding claim 11, wherein said detecting said power-on comprises: receiving a logic-high signal at a control gate of one or more first transistors and one or more second transistors, wherein said one or more first transistors are configured to switch off in response to said logic-high signal, and wherein said one or more second transistors are configured to switch on in response to said logic-high signal; and transmitting a detection signal to a signal processor from said one or more second transistors based on said received logic-high signal.

Regarding claims 12-14, as being dependent on claim 11.

Regarding claim 15, wherein said detecting said power-down comprises: receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to voltage or power detection circuitry and their methods of operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2819

/Dylan White/
Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/365,559	Applicant(s)/Patent Under Reexamination KWON ET AL.	
	Examiner DYLAN WHITE	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,577,166	06-2003	Lim, Kyu-Nam	327/77
*	B	US-5,723,990	03-1998	Roohparvar, Frankie F.	327/81
*	C	US-2008/0100341	05-2008	Kim, Min-Hwahn	326/63
*	D	US-2006/0044027	03-2006	Chen, Kuan-Yeu	327/143
*	E	US-2008/0218223	09-2008	Kimura, Hiroyuki	327/142
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2010								
	1	✓								
	2	O								
	3	O								
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	23	✓								
	24	✓								
	25	✓								
	26	✓								
	27	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12365559	KWON ET AL.
	Examiner	Art Unit
	DYLAN WHITE	2819

SEARCHED			
Class	Subclass	Date	Examiner
326	All	9/9/2010	DW
327	All	9/9/2010	DW

SEARCH NOTES		
Search Notes	Date	Examiner
See Attached EAST Notes	9/9/2010	DW
Inventor Search	9/9/2010	DW
Assignee Search	9/9/2010	DW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
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CONFIRMATION NO. 6210

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/365,559	02/04/2009 RULE	713	2819	072302

APPLICANTS

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Vivek Mohan, San Diego, CA;

DW

**** CONTINUING DATA ***************************

DW

**** FOREIGN APPLICATIONS ***************************

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02/12/2009

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/DYLAN C WHITE/ Examiner's Signature	Initials	CA	8	27	4

ADDRESS

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE

Multiple Supply-Voltage Power-Up/Down Detectors

FILING FEE RECEIVED		
1674	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	15	(detect$3 adj2 (power) with (on and off))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:31
S2	80695	(((voltage or power) adj2 (switch$3 or gat $3)) or (head$3 and foot$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:35
S3	41160	((voltage or power) adj (switch$3 or gat$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:36
S4	133254	((voltage or power) adj (detect$3 or (up and down)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:37
S5	2	("7253655").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:38
S6	6	("4859877" | "5381059" | "6172522" | "6233694" | "6498511" | "7116135").PN. OR ("7253655").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:42
S7	46	((voltage or power) adj (detect$3 with ((up and down) or (on and off))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45
S8	195	kwon-chang$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:45

S9	19	S8 and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:46
S10	28	mohan-vivek$.IN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/08 15:47
S11	5	("20040111649" | "20050117432" | "6611472" | "6650594" | "7372746").PN. OR ("7692998").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:56
S12	12	("4697097" | "5187389" | "5442312" | "5528182" | "5528184").PN. OR ("5781051").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 15:59
S13	65	("4683382" | "4975883" | "5193198" | "5301161" | "5305275" | "5331599" | "5339272" | "5412331" | "5414669").PN. OR ("5594360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:02
S14	4636	((voltage or power or level) adj (detect$3 or sens$3) with transistor) and feedback	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S15	628	S14 and core	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:10
S16	74	S15 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:11
S17	859	S14 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S18	9901	(POC or (power adj (on adj off) adj control))	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S19	118	S18 and (feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:22
S20	513	qualcomm.AS. and (((power or voltage) with control) and feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24

S21	123	qualcomm.AS. and (((power or voltage) with control) with feedback and transistor)	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:24
S23	3959	((voltage or power or level) adj (detect$3 or sens$3) with feedback) and transistor	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S24	472	S23 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/08 16:42
S25	0	(11/048260).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:14
S26	1	(10/339069).APP.	USPAT; USOCR	OR	ON	2010/09/09 07:28
S27	5	("5629642" | "5774402" | "6011447" | "6111441").PN. OR ("6744295").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:29
S28	2	("20050140406" | "6163585").PN. OR ("7612588").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:37
S29	7	("5886567" | "5889664" | "6169426" | "6580312" | "6876246" | "7474140").PN. OR ("7605639").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:38
S30	11	("20060119417" | "4565977" | "5535160" | "5877651" | "6130829" | "6304469" | "6522558" | "6756827" | "6812776" | "6977828" | "7042774").PN. OR ("7429883").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:41
S31	11	("6307401" | "6433579" | "6437599" | "6518797" | "6590422" | "6664814" | "6664853" | "6731135" | "6847232").PN. OR ("7183805").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:44
S32	9	("5270584" | "5721510" | "5723990" | "6411157").PN. OR ("6577166").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 07:49

S33	36	("4961167" | "5189316" | "5315557" | "5337284" | "5557231" | "5602704" | "5633825" | "5673232" | "5856951" | "6031411").PN. OR ("6411157").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:01
S34	18	("5115150" | "5151620" | "5175448" | "5661419" | "5880604" | "6049245" | "6107869" | "6191615" | "6204696" | "6370052" | "6404269" | "6411157" | "6442086" | "6492837" | "6759873").PN. OR ("6900690").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 08:29
S35	7526	(input and output) and core and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S36	352	S35 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:49
S37	389	(input and output) and (core adj2 voltage) and ((voltage or power) adj (detect$3 or sens$3)) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S38	49	S37 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 10:50
S39	0	(power adj ((on and off) or (up and down)) adj detect$3) and core and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:35
S40	9	(power adj ((on and off) or (up and down)) adj detect$3) and ((I adj O) or (input adj output))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:36

S41	1	(power adj ((on and off) or (up and down)) adj detect$3) and core	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S42	2	(power adj ((on and off) or (up and down)) adj detect$3) and feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/09 15:37
S43	40	("4234920" | "4473759" | "4746822" | "4882506" | "4902910" | "5039875" | "5063304" | "5066869" | "5081625" | "5087834" | "5103115" | "5103159" | "5120993" | "5157270" | "5159206" | "5164613" | "5166545" | "5168209" | "5181203" | "5220534" | "5233161" | "5270977" | "5297261" | "5347173").PN. OR ("6204701").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/09/09 15:38
S44	11869	((level or voltage) adj (shift$3 or translat$3)) and (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:40
S45	3036	S44 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S46	2898	S45 and current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41
S48	920	((level or voltage) adj (shift$3 or translat$3)) with (feedback and transistor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41

S49	359	S48 and ("326" or "327").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 06:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	37	(power and (detecting or detection) and feedback and transistor and voltage and core and control). CLM.	USPAT; UPAD	OR	ON	2010/09/10 09:16

9/10/2010 9:17:14 AM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Chang Ki Kwon et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

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Receipt date: 02/04/2009	Application Number	12365559 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	
	First Named Inventor	Chang Ki Kwon et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

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Examiner Signature	/Dylan White/	Date Considered	09/10/2010

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PTO/SB/08a (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12365559
	Filing Date	2009-02-04
	First Named Inventor	Chang Ki Kwon
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6646844		2003-11-11	MATTHEWS LLOYD P	
	2	5130569		1992-07-14	GLICA STEPHEN J	
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020163364		2002-11-07	MAJCHERCZAK SYLVAIN	
	2	20070030039		2007-02-08	CHEN KER-MIN	
	3	20060103437		2006-05-18	KANG KHIL O	
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12365559
	Filing Date	2009-02-04
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	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

	1	2007091211	WO		2007-08-16	NXP BV		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	INTERNATIONAL SEARCH REPORT-PCT/US2010/23081, INTERNATIONAL SEARCH AUTHORITY-EUROPEAN PATENT OFFICE 05-AUGUST-2010	☐
	2	WRITTEN OPINION-PCT/US2010/023081, INTERNATIONAL SEARCH AUTHORITY-EUROPEAN PATENT OFFICE 05-AUGUST-2010	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12365559
	Filing Date	2009-02-04
	First Named Inventor	Chang Ki Kwon
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/ Sam Talpalatsky /	Date (YYYY-MM-DD)	2010-09-08
Name/Print	Sam Talpalatsky	Registration Number	35380

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
072302WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2010/023081	03/02/2010	04/02/2009
Applicant		
QUALCOMM Incorporated		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 3B
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/22
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 646 844 B1 (MATTHEWS LLOYD P [US]) 11 November 2003 (2003-11-11) figures 1,3	1,2,4, 6-11,13, 15,17, 19-27
X	US 2002/163364 A1 (MAJCHERCZAK SYLVAIN [FR] ET AL) 7 November 2002 (2002-11-07) figure 2	1-3, 7-12,15, 16,19-27
X	US 2007/030039 A1 (CHEN KER-MIN [TW]) 8 February 2007 (2007-02-08) figure 3	1,2, 6-11,15, 19-22, 24-27

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2010	05/08/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Santos, Paulo

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/103437 A1 (KANG KHIL O [KR]) 18 May 2006 (2006-05-18) figure 3	1,6, 8-10, 19-27
A	WO 2007/091211 A2 (NXP BV [NL]; WESTENDORP JOEN [NL]; HOEFNAGEL LOUW [NL]) 16 August 2007 (2007-08-16) figure 3	1-27
A	US 5 130 569 A (GLICA STEPHEN J [US]) 14 July 1992 (1992-07-14) figure 1	1-27

1

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/023081

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6646844 B1	11-11-2003	NONE	
US 2002163364 A1	07-11-2002	EP 1249707 A1	16-10-2002
		FR 2822956 A1	04-10-2002
US 2007030039 A1	08-02-2007	NONE	
US 2006103437 A1	18-05-2006	JP 2006148858 A	08-06-2006
		KR 20060054612 A	23-05-2006
WO 2007091211 A2	16-08-2007	CN 101379406 A	04-03-2009
		JP 2009526461 T	16-07-2009
		US 2009002034 A1	01-01-2009
US 5130569 A	14-07-1992	DE 69216663 D1	27-02-1997
		DE 69216663 T2	03-07-1997
		EP 0503803 A1	16-09-1992
		JP 3225075 B2	05-11-2001
		JP 4345208 A	01-12-1992

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

AUG 10 2010

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To:
Talpalatsky, Sam
QUALCOMM INCORPORATED
5775 Morehouse Drive
San Diego, CA 92121-1714
ETATS-UNIS D'AMERIQUE

	Date of mailing *(day/month/year)* 5 August 2010 (05-08-2010)
Applicant's or agent's file reference 072302WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2010/023081	International filing date *(day/month/year)* 3 February 2010 (03-02-2010)
Applicant QUALCOMM Incorporated	

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	GHILINI, Marie Tel: +49 (0)89 2399-6121

Form PCT/ISA/220 (July 2009) *(See notes on accompanying sheet)*

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Annex B).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, International Phase, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet or sheets containing a complete set of claims in replacement of all the claims previously filed must be submitted.

Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively in Arabic numerals (Section 205(a)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide*, National Chapters.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 072302WO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2010/023081	International filing date *(day/month/year)* 03/02/2010	(Earliest) Priority Date *(day/month/year)* 04/02/2009
Applicant QUALCOMM Incorporated		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 3B
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/22
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 646 844 B1 (MATTHEWS LLOYD P [US]) 11 November 2003 (2003-11-11) figures 1,3	1,2,4, 6-11,13, 15,17, 19-27
X	US 2002/163364 A1 (MAJCHERCZAK SYLVAIN [FR] ET AL) 7 November 2002 (2002-11-07) figure 2	1-3, 7-12,15, 16,19-27
X	US 2007/030039 A1 (CHEN KER-MIN [TW]) 8 February 2007 (2007-02-08) figure 3	1,2, 6-11,15, 19-22, 24-27

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2010	05/08/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Santos, Paulo

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/023081

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/103437 A1 (KANG KHIL O [KR]) 18 May 2006 (2006-05-18) figure 3	1,6, 8-10, 19-27
A	WO 2007/091211 A2 (NXP BV [NL]; WESTENDORP JOEN [NL]; HOEFNAGEL LOUW [NL]) 16 August 2007 (2007-08-16) figure 3	1-27
A	US 5 130 569 A (GLICA STEPHEN J [US]) 14 July 1992 (1992-07-14) figure 1	1-27

1

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/023081

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6646844 B1	11-11-2003	NONE	
US 2002163364 A1	07-11-2002	EP 1249707 A1	16-10-2002
		FR 2822956 A1	04-10-2002
US 2007030039 A1	08-02-2007	NONE	
US 2006103437 A1	18-05-2006	JP 2006148858 A	08-06-2006
		KR 20060054612 A	23-05-2006
WO 2007091211 A2	16-08-2007	CN 101379406 A	04-03-2009
		JP 2009526461 T	16-07-2009
		US 2009002034 A1	01-01-2009
US 5130569 A	14-07-1992	DE 69216663 D1	27-02-1997
		DE 69216663 T2	03-07-1997
		EP 0503803 A1	16-09-1992
		JP 3225075 B2	05-11-2001
		JP 4345208 A	01-12-1992

Form PCT/ISA/210 (patent family annex) (April 2005)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/023081	03.02.2010	04.02.2009

International Patent Classification (IPC) or both national classification and IPC
INV. H03K17/22

Applicant
QUALCOMM Incorporated

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Santos, Paulo Telephone No. +49 89 2399-8359

Form PCT/ISA/237 (Cover Sheet) (July 2009)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5, 8, 9, 14, 18, 19, 24, 25, 27
	No:	Claims	1-4, 6, 7, 10-13, 15-17, 20-23, 26
Inventive step (IS)	Yes:	Claims	5, 14, 18
	No:	Claims	1-4, 6-13, 15-17, 19-27
Industrial applicability (IA)	Yes:	Claims	1-27
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:
D1 : US 6 646 844 B1 (MATTHEWS LLOYD P [US]) 11 November 2003 (2003-11-11)
D2 : US 2002/163364 A1 (MAJCHERCZAK SYLVAIN [FR] ET AL) 7 November 2002 (2002-11-07)

2 The present application does not meet the criteria of Article 33 (1) PCT, because the subject-matter of claims 1, 10, 20 and 26 is not new in the sense of Article 33(2) PCT.

2.1 Document D1 discloses (see figures 1 and 3; references in parenthesis relating to this document) a dual supply voltage device and corresponding method comprising:

- a core network (Fig. 1: 150) operative at a first supply voltage (V_{DD});
- a control network (Figs. 1 and 3: CONTROLLER 110) coupled to said core network wherein said control network is configured to transmit a control signal (Fig. 3: ENABLE OVERRIDE), said control network comprising:
- an up/down detector (Fig. 3: 310) configured to detect a power state of said core network (col. 4, lines 47-60);
- processing circuitry (Fig. 3: 320) coupled to said up/down detector and configured to generate said control signal based on said power state;
- one feedback circuit (Fig. 3: 330) coupled to said up/ down detector, said feedback circuit configured to provide a feedback signal to adjust a current capacity of said up/down detector (Fig. 3: transistor 330 and 314 both turned on when V_{DD}/POR is high).

The subject-matter of independent claims 1, 10, 20 and 26 consequently lacks novelty against the disclosure of D1 (Article 33(1)-(2) PCT).

2.2 Document D2 discloses (Figure 2) a dual supply voltage device and corresponding method comprising:

- a core network (Fig. 6: COEUR) operative at a first supply voltage (Vdd);
- a control network (Fig. 6: 1; Fig. 2) coupled to said core network wherein said control network is configured to transmit a control signal (Fig. 2: CORE-OFF), said control network comprising:
- an up/down detector (Fig. 2: E1) configured to detect a power state of said core network (paragraph [0025];
- processing circuitry (Fig. 2: E3) coupled to said up/down detector and configured to generate said control signal based on said power state (paragraph [0025]);
- one feedback circuit (Fig. 2: M6) coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector (Fig. 2: transistor M6 and M4 both turned on when V_{dd} is low).

The features of claims 1, 10, 20 and 26 are also anticipated by D2.

3 Dependent claims 2-4, 6-9, 11-13, 15-17, 19, 21-25, 27 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty or inventive step (Article 33(2) and (3) PCT), the reasons being as follows:

- the up/down detectors in both D1 and D2 comprise a first and a second transistor (D1: 312, 314; D2: M4, M5) with the functionality described in claims 2 and 11;
- D2 shows a first feedback transistor (M6) coupled in parallel with the first transistor (M4), as defined in claims 3, 12 and 16, while D1 shows a second feedback transistor (330) in parallel with the second transistor (314) as described in claims 4, 13 and 17;
- D1 discloses a comparator and a buffer (Fig. 3: 320) connected to the output of the up/down detector. The additional features of claim 6 are thus also known from D1;

- an input/output network operative at the higher supply voltage (claim 7) is described in D1 (Fig. 1: Driver 124) and D2 (Fig. 6: 9);
- the feature of claims 8 and 24 is merely one of several straightforward possibilities from which the skilled person would select, in accordance with circumstances, without the exercise of inventive skill, in order to implement an electronic system;
- the invention of claims 9, 19, 25 and 27 consists merely in the use of the circuits described in D1 and D2 in several consumer electronics devices. This use, however, does not involve more than employment of properties of the circuits which are also already known from D1 and D2. Hence, no inventive step is present in the subject-matter of claims 9, 19, 25 and 27;
- the features of claim 15 are implicit functional features of the N- and PMOS transistors comprised in the up/down detectors of D1 and D2;
- the feedback mechanism described in claims 21, 22 and 23 is also realized by the feedback transistors 330 of D1 and M6 of D2.

4 The combination of the features of dependent claims 5, 14, 18 are neither known from, nor rendered obvious by, the available prior art.

Re Item VII

Certain defects in the international application

5 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

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16 August 2007 (16.08.2007)

PCT

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(30) Priority Data:
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(72) Inventors; and

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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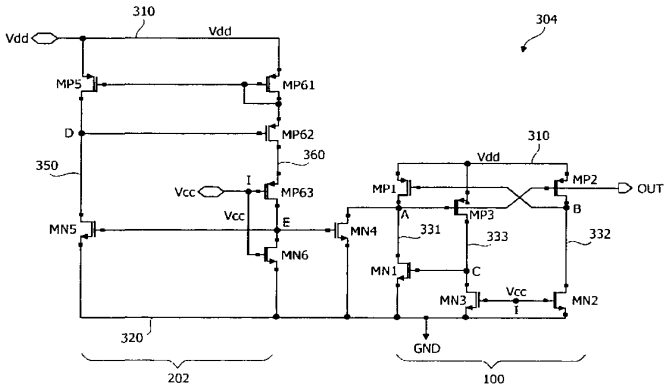
Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CIRCUIT ARRANGEMENT AND METHOD FOR DETECTING A POWER DOWN SITUATION OF A VOLTAGE SUPPLY SOURCE



(57) Abstract: Circuit arrangement for detecting a power down situation of a second voltage comprising a first conductor, adapted the be connected to a first voltage, a second conductor, adapted the be connected to a reference voltage, an input node, adapted the be connected to the second voltage, and two output nodes, a first output node and a second output node. The output nodes are interconnected in such a manner, that (a) when the second voltage is higher than the reference voltage, the first output node is at the first voltage level and the second output node is at the reference voltage level, and (b) when the second voltage is equal to the reference voltage, the first output node is at the reference voltage level and the second output node is at the first voltage level. The circuit arrangement further comprises an inverter section arranged in between the two conductors, wherein the input node represents an inverter section input and wherein an inverter section output node is formed representing the inverter section output.

WO 2007/091211 A2

DESCRIPTION

CIRCUIT ARRANGEMENT AND METHOD FOR DETECTING A POWER DOWN SITUATION OF A VOLTAGE SUPPLY SOURCE

The present invention relates to the field of electronic circuits for detecting a voltage level of a voltage supply source. In particular, the present invention relates to a circuit arrangement for detecting a power down situation of a voltage level provided by a voltage supply source. Further, the present invention relates to a method for detecting a power down situation of a second voltage level (Vcc) with a circuit arrangement as described above.

In many electronic devices, e.g. in computers and in particular in main boards of computers there are electronic circuits comprising a plurality of different electronic components. Frequently, some components and/or circuit portions are operated at a first supply voltage level wherein other components and/or circuit portions are operated at a second supply voltage level, which is different from the first supply voltage level.

In order to prevent an irreversible damage of such electronic devices there are known so-called voltage level shifters, which may be used in a modified way such that they can indicate when a power supply voltage passes over into a power down situation.

US 2004/0207450 discloses a voltage level shifter, which comprises a level changer and an output circuit. The level changer has a current block and a first transistor. A high voltage power supply higher than the potential of the low voltage power supply or the current block is connected to a source or a drain of the first transistor. The level changer outputs a potential of the high voltage power supply or a reference potential by a potential of an input signal inputted into the first transistor. The output circuit outputs an output signal having amplitude between the reference potential and the potential of the high voltage power supply when a signal from an output end of the level changer is inputted thereto. However, the state of the output is not determined if one of the two

voltage supplies removed. Therefore, the disclosed circuit is not suitable for detecting a power down situation of one of the supply voltage sources.

There may be a need for a circuit arrangement and a method for detecting a power down situation of a voltage supply source.

This need may be met by a circuit arrangement for detecting a power down situation of a second voltage level as set forth in claim 1. According to a first aspect of the invention the circuit arrangement comprises a first conductor, adapted the be connected to a first voltage level, a second conductor, adapted the be connected to a reference voltage level, an input node, adapted the be connected to the second voltage level, and two output nodes, a first output node and a second output node, which are interconnected within the circuit arrangement. The two output nodes are interconnected in such a manner, that (a) when the second voltage level is higher than the reference voltage level, the first output node is at the first voltage level and the second output node is at the reference voltage level, and (b) when the second voltage level is equal to the reference voltage level, the first output node is at the reference voltage level and the second output node is at the first voltage level. The circuit arrangement further comprises an inverter section arranged in between the first conductor and the second conductor, wherein the input node represents an inverter section input and wherein an inverter section output node is formed representing the inverter section output.

This aspect of the invention is based on the idea that a so-called level shifter circuit may be advantageously used as a power down detection circuit, if the level shifter circuit is modified. The modification includes the replacement of a conventional inverter, which is usually included in a level shifter circuit, with an inverter section arranged in between the first and the second conductor. This may provide the advantage that the power down detection is also working reliable when a voltage source providing the second voltage level is completely down, i.e. when the second voltage level is zero volts.

It has to be pointed out that all voltage levels, which are mentioned above and which will be mentioned later in this description might differ slightly from the stated voltage levels due to one or more so-called voltage drops. Such voltage drops may be generated e.g. by pn-transitions in any diode like semiconductor component.

According to an embodiment of the present invention as set forth in claim 2, the reference voltage level is at ground level. This has the advantage that the circuit arrangement might be used in electronic devices, which do not comprise a third voltage level. In particular if the first and the second supply voltage level are positive with respect to the ground level, there is no need for a negative supply voltage for operating the circuit arrangement for power down detection. This makes the circuit arrangement to be operable very easily such that the described power down detection might be applicable in many different electronic devices.

According to a further embodiment of the invention as set forth in claim 3, the second voltage level is lower than the first voltage level. Since many electronic devices require two supply voltage levels, e.g. approximately 3,6 Volt and 1,1 Volt, the described circuit arrangement may be useful for improving the robustness and the life cycle of such devices.

According to a further embodiment of the invention as set forth in claim 4, the circuit arrangement further comprises two first switching elements arranged in series in between the first conductor and the second conductor whereby the first output node is formed in between these two first switching elements and whereby the inverter section output node is connected with one switching element out of these two first switching elements, which switching element is arranged in between the first output node and the second conductor.

Preferably, the two first switching elements are Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) whereby one MOSFET is a so-called p-channel MOSFET (pmos device) and the other MOSFET is a so-called n-channel MOSFET

(nmos device). Since both MOSFET devices are used in a complementary way the switching elements are also called CMOS switching elements.

CMOS switching elements provide the advantage that only a very small stationary current flows from the first conductor to the second conductor when at least one switching element arranged in each branch between the two conductors is closed. Therefore, electronic devices with a very low power consumption may be built up.

According to a further embodiment of the invention as set forth in claim 5, the circuit arrangement further comprises two second switching elements arranged in series in between the first conductor and the second conductor whereby the second output node is formed in between these two second switching elements. Preferably, also the second switching elements are also so-called CMOS switching elements having the advantage that a only a very low stationary current flows from the first conductor to the second conductor.

According to a further embodiment of the invention as set forth in claim 6, the inverter section comprises two third switching elements arranged in series in between the first conductor and the second conductor whereby the inverter section output node is formed in between these two third switching elements. This embodiment has the advantage that the inverter may be built up very easy such the production costs of such a power down situation detecting device may be reduced.

Further, apart from the first voltage level the presence of the second voltage level is not needed in order to make the power down detection of the second voltage level working reliably. As has already been mentioned above, preferably CMOS switching elements may be used for the third switching elements having the above described advantage of a low static current.

According to a further embodiment of the invention as set forth in claim 7, the circuit arrangement further comprises a fourth switching element. The fourth switching

element is connected in between the first output node and the second conductor in such a manner that the first output node is capable of being at least partially discharged when the second voltage level accomplishes a shift from the voltage level higher than the reference voltage level to the reference voltage level. The fourth switching element, which preferably is arranged in parallel to the third switching element, may allow for a faster discharging of the first output node in the event of an abrupt power down situation of the second voltage. This may provide the advantage that the power down detection becomes faster and more reliable.

In this context it is stated that the discharging may further be speeded up due to a discharge amplification effect provided by a loop formed by the second conductor and the inverter section and in particular by the second conductor and the inverter section output node.

According to a preferred embodiment of the invention as set forth in claim 8, the circuit arrangement further comprises a current mirror section, wherein a first current mirror node of the current mirror section is connected with the fourth switching element. This may have the advantage that the current mirror provides a stable and reliable control for the fourth switching element.

In this embodiment of the invention a modified level shifter circuit and a current mirror circuit are combined in an advantageous way. This has the advantage that the circuit arrangement always is in an electronically defined state (i.e. no floating nodes) even when the supply source of the second voltage supply level is completely failed and the second voltage level is at ground level.

According to a further embodiment of the invention as set forth in claim 9, the current mirror section comprises a first branch and a second branch whereby both branches are arranged in between the first conductor and the second conductor. Therefore, the set up of the current mirror section corresponds to the well-known current mirror setup.

According to a further embodiment of the invention as set forth in claim 10, two fifth switching elements are arranged in series within the first branch and a second current mirror node is formed in between these two fifth switching elements. Again, preferably CMOS switching elements may be used for the fifth switching elements such that a small stationary current may be generated leading to a low power consumption and, as a consequence, to a low heat development within an electronic device which includes the described circuit arrangement for a reliably power down detection.

According to a further embodiment of the invention as set forth in claim 11, at least two sixth switching elements are arranged in series within the second branch and the first current mirror node is formed in between these two sixth switching elements.

According to a further embodiment of the invention as set forth in claim 12, four sixth switching elements are arranged within the second branch whereby three sixth switching elements out of these four sixth switching elements are arranged in series in between the first conductor and the first current mirror node and one sixth switching element out of these four sixth switching elements is arranged in between the first current mirror node and the second conductor. This may provide the advantage that a middle switching element out of these three sixth switching elements arranged in series in between the first conductor and the first current mirror node effectively represents a current limiter. Therefore, the stationary current flowing through the second branch is reduced significantly leading to the above-mentioned beneficial properties of the entire power down detection circuit. Since in the current mirror the stationary current flowing through the first branch has the same reduced amperage the total power dissipated by the current mirror may be reduced by a factor of two.

According to a further embodiment of the invention as set forth in claim 13, two sixth switching elements, which both are directly connected to the first current mirror node are controlled by the second voltage level. The connections between the second voltage level and these two switching elements, respectively, may have the advantage that in case of an abrupt voltage drop of the second voltage level down to ground voltage level

the voltage level of the first current mirror node will be enhanced and, as a consequence, the fourth switching element will open leading to a discharge current flowing from the first output node to ground. Therefore, the temporal coarse of the voltage level being present at the first output node will follow the temporal coarse of second voltage level more quickly and in a more reliably way. As a consequence, the entire power down detection will be faster and more reliably.

The above-mentioned need may further be met by a method as set forth in claim 14. According to this aspect of the invention there is provided a method for detecting a power down situation of a second voltage level with any of the circuit arrangements, which have been described above. The method comprises the following characteristic steps:

(a) changing the voltage level of the first output node from the first voltage level to the reference voltage level and (b) changing the voltage level of the second output node from the reference voltage level to the first voltage level

when the second voltage level accomplishes a shift from a voltage level higher than the reference voltage level to the reference voltage level, and

(a) changing the voltage level of the first output node from the reference voltage level to the first voltage level and (b) changing the voltage level of the second output node from the first voltage level to the reference voltage level

when the second voltage level accomplishes a shift from the reference voltage level to a voltage level higher than the reference voltage level. The method advantageously allows for a reliable power down detection with a low power consumption. The low power consumption is related to low static currents within the circuit.

According to an embodiment of the invention as set forth in claim 15, the first output node is at least partially discharged, when the second voltage level accomplishes a shift from the voltage level higher than the reference voltage level to the reference voltage level. The discharging is assisted by of a fourth switching element, which is connected in between the first output node and the second conductor.

The fourth switching element, which preferably is arranged in parallel to the third switching element, may allow for a faster discharging of the first output node. Therefore, a power down detection of the second voltage level is much faster and much more reliable because the output signal at the first output node can follow a change of the input signal much faster. Therefore, the power down detection is both faster and more reliable.

It has to be noted that certain embodiments of the invention have been described with reference to circuit arrangements and other embodiments of the invention have been described with reference to methods for detecting a power down situation. However, a person skilled in the art will gather from the above and the following description that, unless other notified, in addition to any combination of features belonging to one category of claims also any combination between features of the method claims and features of the circuit claims is possible and is disclosed with this application.

The aspects defined above and further aspects of the present invention are apparent from the examples of embodiment to be described hereinafter and are explained with reference to the examples of embodiment. The invention will be described in more detail hereinafter with reference to examples of embodiment but to which the invention is not limited.

Fig. 1 shows an extended level shifter adapted to detect a power down situation of a second supply voltage Vcc.

Fig. 2 shows a current mirror including a current limiting switching element, which current mirror is adapted to be combined with the extended level shifter shown in Fig. 1 in order to build up an even more reliable circuit for detecting a power down situation.

Fig. 3 shows a circuit diagram of an improved power down detection circuit arrangement.

Fig. 4 shows diagrams depicting the temporal behavior of the output shown in Fig. 3 when the voltage level Vcc is varied in a stepwise manner.

The illustration in the drawing is schematically. It is noted that in different drawings, similar or identical elements are provided with the same reference signs or with reference signs, which are different from the corresponding reference signs only within the first digit.

Fig. 1 shows a power down detection circuit arrangement 100 according to an embodiment of the invention. The setup of the circuit arrangement 100 is based on a so-called conventional level-shifter. The circuit 100 comprises a first conductor 110, which is connected to a voltage supply source (not shown) providing a first supply voltage Vdd. The circuit 100 further comprises a second conductor 120, which is connected to ground GND.

In between the first conductor 110 and the second conductor 120 there are formed three branches, a left branch 131, a right branch 132 and a middle branch 133. The left branch 131 comprises a pmos switch MP1 and an nmos switch MN1, which are arranged in series with respect to each other. In between these two switches MP1 and MN1 there is formed a first output node A. The right branch 132 comprises a pmos switch MP2 and an nmos switch MN2, which are also arranged in series with respect to each other. In between these two switches MP2 and MN2 there is formed a second output node B.

The source contacts of the two pmos switches MP1 and MP2, respectively, are both connected to the first conductor 110. As can be seen from Fig. 1 the gate contacts and the drain contacts of the two pmos switches MP1 and MP2, respectively, are coupled in a cross wise manner with each other. Therefore, the gate of MP1 is connected with the second output node B and the gate of MP2 is connected with the first output node A.

The middle branch 133 comprises a pmos switch MP3 and an nmos switch MN3. In between these two switches MP3 and MN3 there is formed a node C. This node C is denoted an inverter section second output node because the two switches MP3 and MN3 effectively form an inverter section, which comprises the gate of MN3 as an input and

the node C as an output. The inverter formed by MP3 and MN3 will be described later on.

The gates of MN3 and MN2 are both connected to an input node I, which itself is connected to a voltage supply source (not shown) providing a second supply voltage Vcc. The gate of MP3 is connected with the first output node A and with the gate of MP2, respectively.

In order to detect the power situation of the voltage supply source providing Vcc, Vcc is applied to the input node I of the circuit 100. As one can be see from the forthcoming description the voltage levels of the first output node A and the second output node B, respectively, indicate the power situation of Vcc. Therefore, in order to understand the power down detection modus of the circuit 100 one has to become clear what happens when Vcc is toggled.

At this point the typical behavior of pmos and nmos switches in digital electronics is briefly recapitulated in a simplified manner: A pmos switch is open when a low voltage state is applied to its gate and the pmos switch is closed when a high voltage state is applied to its gate. Accordingly, an nmos switch is closed when a low voltage state is applied to the gate of the nmos device and the nmos switch is open when a high voltage state is applied to its gate.

If the voltage source supplying Vcc is working, i.e. the voltage level Vcc is well above ground, the two nmos switches MN2 and MN3 will be in the opened state. Therefore, the second output node B and the inverter section output node C will be pulled low to ground level GND. The low state of node C will cause a charging of the first output node A until this node A is at a voltage level of Vdd. The cross coupled configuration of the pmos switches MP1 and MP2 ensures that the voltage level of the second output node B is always the inverted voltage level of the voltage level of the first output node A. Therefore, when Vcc is well above ground GND the voltage level of the second output node B is low. This approves the low state of node B, which already has been

defined as low because of the open state of MN2. Therefore, the depicted cross coupling of MP1 and MP2 makes the output states to defined more decided.

If the voltage source supplying Vcc has a failure, i.e. the voltage level Vcc drops to a voltage level corresponding to ground GND, the nmos switches MN2 and MN3 will shut off allowing node B and node C to rise to Vdd. This will cause the nmos device MN1 to open which in turn causes the first output node A to drop to zero volts such that node A is at ground level GND.

In the circuit arrangement 100 the pmos device MP3 and the nmos device MN3 represent an inverter. Thereby, node I is the inverter input and node C is the inverter output.

If Vcc is well above ground level GND, MN2 will be open such that node B is at a low voltage state. This causes the pmos device MP1 to be open such that node A will be at Vdd. Further, Node A is connected to the gate of the pmos switch MP3. Therefore, MP3 will be closed. Furthermore, MN3 is open because Vcc is well above ground level GND. As a consequence of a closed MP3 and an open MN3 the voltage level at node C is low.

On the other hand, if Vcc is at ground level GND, MN2 will be closed such that node B is at a high voltage state. This causes the pmos device MP1 to be closed such that node A will be at ground level GND. Node A is connected to the gate of the pmos switch MP3. Therefore, MP3 will be opened. Further, MN3 is closed because Vcc is at ground level GND. As a consequence of an open MP3 and a closed MN3 the voltage level at node C is high.

As can be seen from the above given description of the switching states of the pmos and the nmos devices included in the circuit 100, in each of the branches 131, 132 and 133 there is always at least one closed switch. This rule applies independent of the power situation of the voltage supply source providing Vcc. As a consequence, the circuit 100

allows only very small static currents flowing from the first conductor 110 to the second conductor 120. This has the advantage that the overall power consumption of the power down detecting circuit is very low. Therefore the circuit 100 can be implemented in a variety of different applications such that the corresponding electronic devices become more reliable and less error-prone because a failure of a voltage supply source providing Vcc can be detected reliably.

Fig. 2 shows a circuit 202 representing a modified current mirror section. As will be seen in the forthcoming description of a further improved power down detection circuit 304 depicted in Fig. 3 the current mirror section 202 will be useful in order to build up such an improved circuit 304.

The current mirror section 202 comprises a first conductor 210, which is connected to a voltage supply source (not shown) providing a first supply voltage Vdd. The circuit 202 further comprises a second conductor 220, which is connected to ground GND.

In between the first conductor 210 and the second conductor 220 there are formed two branches, a first branch 250 and a second branch 260. The first branch 250 comprises a pmos switch MP5 and an nmos switch MN5, which are arranged in series with respect to each other. In between these two switches MP5 and MN5 there is formed a second current mirror node D. The second branch 260 comprises three pmos switches MP61, MP62 and MP63 and one nmos switch MN6. The devices MP61, MP62, MP63 and MN6 are arranged in series. In between the two switches MP63 and MN6 there is formed a first current mirror node E.

The gate of MP62 is connected with node D. The gate of MN5 is connected with node E. The gate of MP63 and the gate of MN6 are both connected to Vcc.

As can be seen from Fig. 2, the source of MP5 and the source of MP61 are both connected to Vdd. Further, the gate of MP5, the gate of MP61 and the drain of MP61 are connected with each other. Therefore, the top portion of the current mirror section

202 including the two pmos devices represents a simple current mirror, which is well known by common textbooks teaching the art of electronics. Since with MOSFET devices the currents flowing through the gates of the switches MP5, MN5, MP61, MP62, MP63 and MN6 are negligible, the current mirror ensures that the current flowing through the first branch 250 has exactly the same amperage as the current flowing through the second branch 260. Thereby, the current flowing through the second branch 260 serves as a reference current.

However, the circuit 202 does not only represent a current mirror. The circuit also represents an inverter. Thereby, Vcc, which is supplied to the gates of MP63 and MN6, is the input and node E is the output. If Vcc is well above ground level GND, MN6 will be open and MP63 will be closed. Therefore, node E is at ground level GND. If Vcc is at ground level GND, MN6 will be closed and MP63 will be opened. In that case, the node E will be at a high voltage level.

In order to guarantee a small static current flowing through both branches 250 and 260, a current limiting is provided. The current limiting can be understood from the following description, where it is assumed that Vdd is equal to approximately 3,6 Volt and Vcc is equal to approximately 1,1 Volt.

If Vcc is present at the gate of MN6, this nmos switch MN6 is open causing node E to be at ground level GND. This causes MN5 to be closed. Therefore, no current will flow through any of the two branches 250 and 260, because there is no voltage difference between node E and ground GND. This means that apart from voltage drops caused by the semiconductor devices MP61 and MP62 a node X, which is located between MP62 and MP63, is almost at a voltage level of 3,6 Volts.

However, MP63 will open at least partially because Vcc is too small to completely close MP63. This causes a current to flow through the second branch 260 to ground GND (MN6 is still open). This current is mirrored to the first branch 250. Since E is still at GND also MN5 is closed. This leads to a charging of node D such that the voltage level

at node D will rise. This voltage level increase at node D will cause MP62 to close at least partially such that the current flowing through branch 260 will be reduced. After a static current situation has been established the pmos switch MP62 represents a current limiter. As a consequence, the static currents flowing through both branches 250 and 260 are reduced significantly.

Fig. 3 shows an improved power down detection circuit arrangement 304, which comprises a power down detection circuit arrangement 100 as depicted in Fig. 1 and a current mirror section 202 as depicted in Fig. 2. Although depicted as separate conductors, the circuit 304 comprises a common first conductor 310 providing a first supply voltage Vdd for both circuits 202 and 100. Further, the circuit 304 comprises a second conductor 320 providing a common ground GND.

It has to be noted that the denotation of the various MOSFET devices and the various nodes correspond to the denotation of the MOSFET devices and the nodes shown in Figs. 1 and 2, respectively.

The circuit arrangement 304 further comprises a common node I for applying the second supply voltage Vcc to the gates of MP63, MN6, MN3 and MN2, respectively. Since a power down detection of the second supply voltage Vcc is carried out by the circuit arrangement 304, the separately depicted nodes I represent a common input to the power down detection circuit 304.

The improved power down detection circuit 304 further comprises an nmos switching device MN4, which is arranged in between the two circuits 202 and 100. Thereby, the drain contact of MN4 is connected to the first output node A known from Fig. 1, the gate of MN4 is connected to the first current mirror node E known from Fig. 2 and the source of MN4 is connected to ground GND. The influence of the nmos switch MN4 will be described later on.

For detecting the power situation of Vcc the circuit comprises an output OUT, which is connected to the gate of MP2, to the gate of MP3, to the first output node A and to the drain of MN4. As has already been elucidated in the description of the circuit 100 (shown in Fig. 1), if the second supply voltage is well above GND, the voltage level at node A and at the output OUT will be Vdd, respectively. By contrast thereto, if Vcc is at ground level GND, the node A and the output OUT will be at GND level, respectively.

In this paragraph the influence of the switching device MN4 will be explained: When Vcc accomplishes an abrupt shift from a voltage level significant higher than ground level GND (e.g. Vcc = 1,1 V) down to ground level GND, both nmos switches MN3 and MN2 will be closed. Therefore, neither node B nor node C can be discharged. However, as has already been elucidated in the description of the circuit 202 (shown in Fig. 2), if Vcc drops down to ground level GND, MN6 will be closed and MP63 will be opened. In that case, the node E will be at a high voltage level. Therefore, the nmos device NM4 will open such that the first output node A and also the output OUT will be discharged such that the corresponding voltage level decreases. In addition to this, if the voltage at node A falls below the switching voltage of the inverter formed by MP3 and MN4 such that the pmos switch MP3 opens, node C will be charged up to Vdd. This will cause MN1 to pass over in an open state such that the discharging of the first output node A is accelerated.

Therefore, the nmos device MN4 driven by node E of the current mirror section 202 and arranged parallel to the nmos switch MN1 of the circuit 100, allows for a faster discharging of the first output node A in the event of an abrupt power down situation of Vcc. This has the advantage that the power down detection of the improved power down detection circuit 304 is even faster and more reliable compared to the power down detection circuit 100.

The improved power down detection circuit 304 has the advantage that independent of the presence of Vcc in each of the five branches 331, 332, 333, 350 and 360 there is

always at least one switching device closed. Therefore, the static current flowing from the first conductor 310 to the second conductor is very low. This behavior has been verified with Direct Current (DC) simulations. The simulations apply for MOSFET devices, which have been produced be means of a so-called 350 nm diffusion process wherein gates with a length of 350 nm are formed. The results of these simulations, which have been carried out for different combinations of Vdd and Vdd, are shown in Table 1.

Vdd [V]	0			1.1			3.6		
Vcc [V]	0	1.1	3.6	0	1.1	3.6	0	1.1	3.6
I (Vdd) [nA]	0	0	0	2.1	1.0	3.6	8.9	1.0	3.6
I (Vcc) [nA]	0	0	0	0	0	0	0	0	0

Table 1: DC simulation of the improved power down detection circuit 304 as a function of different supply voltages Vdd and Vcc.

Thereby, I (Vdd) represents the current drawn from Vdd given in 10^{-9} ampere (nA). I (Vcc) represents the current drawn from Vcc also given in nA. One can see, that in any case I (Vcc) is below 1 nA. It has been found out that I (Vcc) is in the range of 10^{-15} ampere (fA). The reason for this low static current I (Vcc) is that the second supply voltage Vcc is connected only to gates of nmos and pmos devices, which are electrically isolated from the source and the drain contacts of these devices, respectively.

Fig. 4 shows the results of transient simulations of the behavior of the output OUT when the input signal Vcc is ramped up and down. Different voltage levels are plotted versus the time. The scale unit of the voltage-axis is Volt (V). The scale unit of the time-axis is 10^{-6} seconds (μs). Two different situations are depicted: The dashed line shows the behavior of the output OUT for a first supply voltage level Vdd equal 3,6 V and abrupt changes of Vcc between 0 V and 1,1 V. The full line shows the OUT signal for Vdd equal 1,1 V and abrupt changes of Vcc between 0 V and 3,1 V.

As one can see from the depicted transients, if the Vcc is ramped up, the output OUT is also ramped up. If Vcc is removed, the output OUT goes also to a low voltage level

state. The voltage level of the output OUT never exceeds the voltage level of the first supply voltage Vdd. This holds even when the Vcc is ramped up to a voltage level higher than Vdd (see dashed lines).

It has to be pointed out that the improved power down detection circuit 304 is able to put all outputs, in particular the output OUT into an high-impedance mode if the second supply voltage level Vcc passes over to ground level GND.

The improved power down detection circuit 304 can be used generally in any electronic device with two supply voltage sources providing different supply voltages Vdd and Vcc wherein some action is needed depending on the presence of these supply voltages.

It should be noted that the invention is not limited to the exemplary examples shown in the figures. In particular, it is clear for a person skilled in the art that the invention may be realized also with other switching devices like ordinary transistors or other types of Field Effect Transistors (FET), e.g. Junction FET. It is also clear that the invention can also be realized when, in the circuits 100, 202 and 304 shown in Fig. 1, Fig. 2 and Fig. 3, respectively, a pmos device is replaced by an nmos devise and vice versa.

It should be further noted that the term "comprising" does not exclude other elements or steps and the "a" or "an" does not exclude a plurality. Also elements described in association with different embodiments may be combined. It should also be noted that reference signs in the claims should not be construed as limiting the scope of the claims.

LIST OF REFERENCE SIGNS:

100	power down detection circuit arrangement
110	first conductor
120	second conductor
131	left branch
132	right branch
133	middle branch
Vdd	first supply voltage
Vcc	second supply voltage
GND	Ground
I	input node
A	first output node
B	second output node
C	inverter section output node
MP1	pmos switch
MN1	nmos switch
MP2	pmos switch
MN2	nmos switch
MP3	pmos switch
MN3	nmos switch

202	current mirror section
210	first conductor
220	second conductor
250	first branch
260	second branch
Vdd	first supply voltage
Vcc	second supply voltage
GND	Ground

E	first current mirror node
D	second current mirror node
X	node
MP5	pmos switch
MN5	nmos switch
MP61	pmos switch
MP62	pmos switch
MP63	pmos switch
MN6	nmos switch

304	improved power down detection circuit arrangement
310	first conductor
320	second conductor
331	left branch of circuit 100
332	right branch of circuit 100
333	middle branch of circuit 100
350	first branch
360	second branch
Vdd	first supply voltage
Vcc	second supply voltage
GND	Ground
I	input node
A	first output node
OUT	output
B	second output node
C	inverter section output node
E	first current mirror node
D	second current mirror node
MP1	pmos switch
MN1	nmos switch
MP2	pmos switch

	MN2	n-CMOS switch
	MP3	pmos switch
	MN3	nmos switch
	MN4	nmos switch
5	MP5	pmos switch
	MN5	nmos switch
	MP61	pmos switch
	MP62	pmos switch
	MP63	pmos switch
10	MN6	nmos switch

CLAIMS:

1. Circuit arrangement for detecting a power down situation of a second voltage level (Vcc), the circuit arrangement comprising

a first conductor (110), adapted the be connected to a first voltage level (Vdd),

a second conductor (120), adapted the be connected to a reference voltage level (GND),

an input node (I), adapted the be connected to the second voltage level (Vcc),

a first output node (A) and a second output node (B), which are interconnected within the circuit arrangement in such a manner, that

- when the second voltage level (Vcc) is higher than the reference voltage level (GND), the first output node (A) is at the first voltage level (Vdd) and the second output node (B) is at the reference voltage level (GND), and

- when the second voltage level (Vcc) is equal to the reference voltage level (GND), the first output node (A) is at the reference voltage level (GND) and the second output node (B) is at the first voltage level (Vdd), and

an inverter section arranged in between the first conductor (110) and the second conductor (120),

wherein the input node (I) represents an inverter section input and

wherein an inverter section output node (C) is formed representing the inverter section output.

2. Circuit arrangement according to claim 1, wherein the reference voltage level is at ground level (GND).

3. Circuit arrangement according to claim 1, wherein the second voltage level (Vcc) is lower than the first voltage level (Vdd)

4. Circuit arrangement according to claim 1, further comprising

two first switching elements (MP1, MN1) arranged in series in between the first conductor (110) and the second conductor (120)

whereby the first output node (A) is formed in between these two first switching elements (MP1, MN1) and

whereby the inverter section output node (C) is connected with one switching element (MN1) out of these two first switching elements (MP1, MN1), which switching element (MN1) is arranged in between the first output node (A) and the second conductor (120).

5. Circuit arrangement according to claim 1, further comprising

two second switching elements (MP2, MN2) arranged in series in between the first conductor (110) and the second conductor (120)

whereby the second output node (B) is formed in between these two second switching elements (MP2, MN2).

6. Circuit arrangement according to claim 1, wherein the inverter section comprises

two third switching elements (MP3, MN3) arranged in series in between the first conductor (110) and the second conductor (120) whereby

the inverter section output node (C) is formed in between these two third switching elements (MP3, MN3).

7. Circuit arrangement according to claim 1, further comprising

a fourth switching element (MN4), which is connected in between the first output node (A) and the second conductor (320) in such a manner that

the first output node (A) is capable of being at least partially discharged when the second voltage level (Vcc) accomplishes a shift from the voltage level higher than the reference voltage level (GND) to the reference voltage level (GND).

8. Circuit arrangement according to claim 7, further comprising

a current mirror section (300), wherein a first current mirror node (E) of the current mirror section (300) is connected with the fourth switching element (MN4).

9. Circuit arrangement according to claim 8, wherein

the current mirror section (200) comprises a first branch (250) and a second branch (260) whereby both branches (250, 260) are arranged in between the first conductor (210) and the second conductor (220).

10. Circuit arrangement according to claim 9, wherein

two fifth switching elements (MP5, MN5) are arranged in series within the first branch (250) and

a second current mirror node (D) is formed in between these two fifth switching elements (MP5, MN5).

11. Circuit arrangement according to claim 9, wherein

at least two sixth switching elements (MP61, MN6) are arranged in series within the second branch (260) and

the first current mirror node (E) is formed in between these two sixth switching elements (MP61, MN6).

12. Circuit arrangement according to claim 11, wherein

four sixth switching elements (MP61, MP62, MP63, MN6) are arranged within the second branch (260) whereby

three sixth switching elements (MP61, MP62, MP63) out of these four sixth switching elements (MP61, MP62, MP63, MN6) are arranged in series in between the first conductor (210) and the first current mirror node (E) and

one sixth switching element (MN6) out of these four sixth switching elements (MP61, MP62, MP63, MN6) is arranged in between the first current mirror node (E) and the second conductor (210).

13. Circuit arrangement according to claim 12, wherein

two sixth switching elements (MP63, MN6) which both are directly connected to the first current mirror node (E) are controlled by the second voltage level (Vcc).

14. Method for detecting a power down situation of a second voltage level (Vcc) with a circuit arrangement according to any one of the claims 1 to 13, the method comprising the steps of

when the second voltage level (Vcc) accomplishes a shift from a voltage level higher than the reference voltage level to the reference voltage level

- changing the voltage level of the first output node (A) from the first voltage level (Vdd) to the reference voltage level (GND) and
- changing the voltage level of the second output node (B) from the reference voltage level (GND) to the first voltage level (Vdd) and

when the second voltage level (Vcc) accomplishes a shift from the reference voltage level to a voltage level higher than the reference voltage level

- changing the voltage level of the first output node (A) from the reference voltage level (GND) to the first voltage level (Vdd) and
- changing the voltage level of the second output node (B) from the first voltage level (Vdd) to the reference voltage level (GND).

15. Method according to claim 14, wherein

when the second voltage level (Vcc) accomplishes a shift from the voltage level higher than the reference voltage level (GND) to the reference voltage level (GND) the first output node (A) is at least partially discharged by means of a fourth switching element (MN4), which is connected in between the first output node (A) and the second conductor (320).

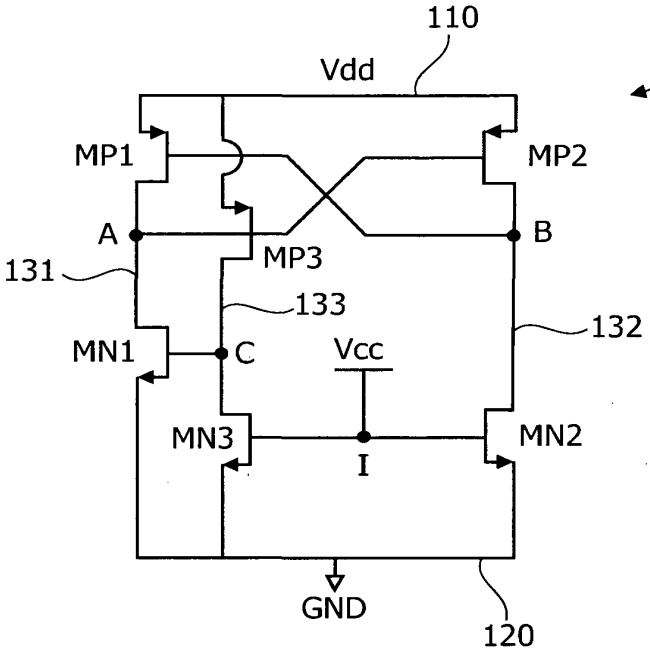


FIG. 1

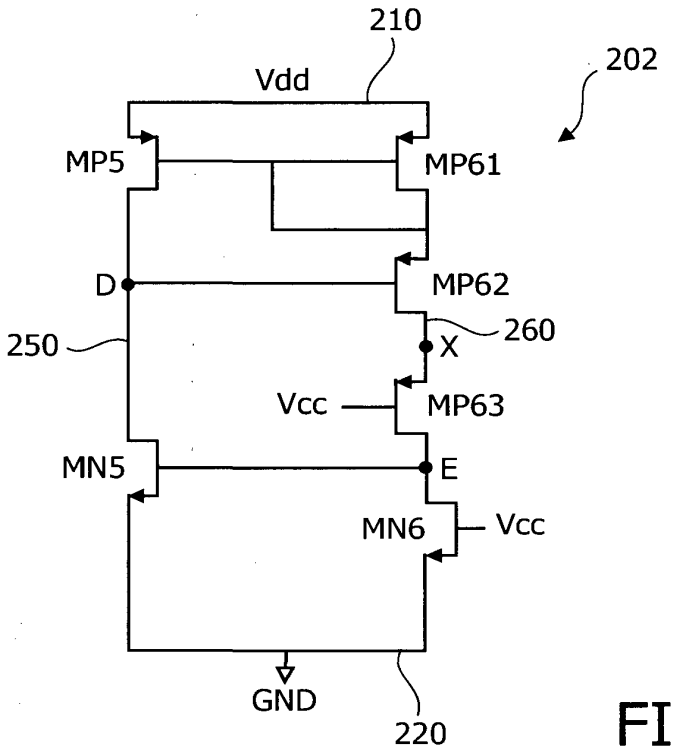


FIG. 2

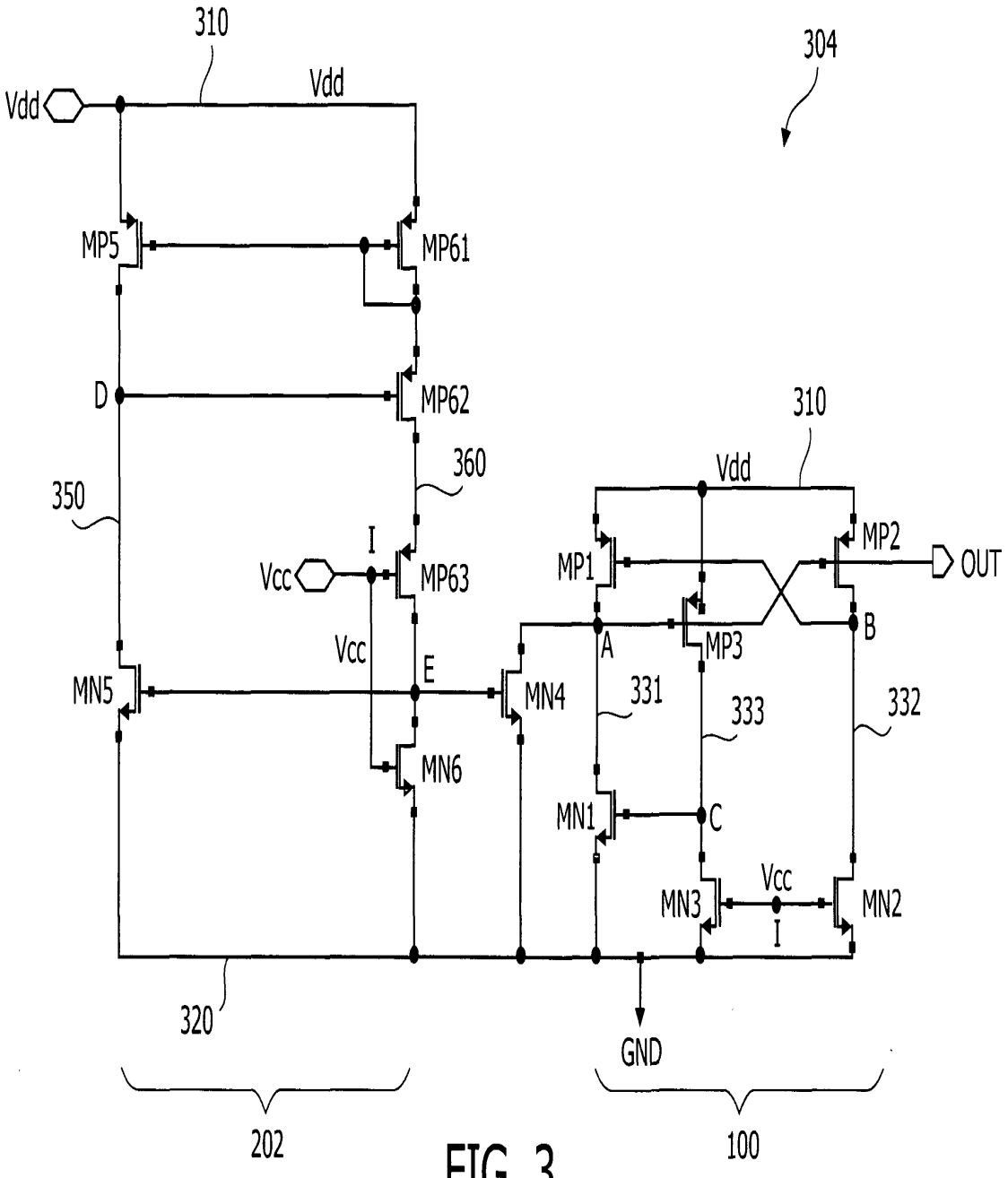


FIG. 3

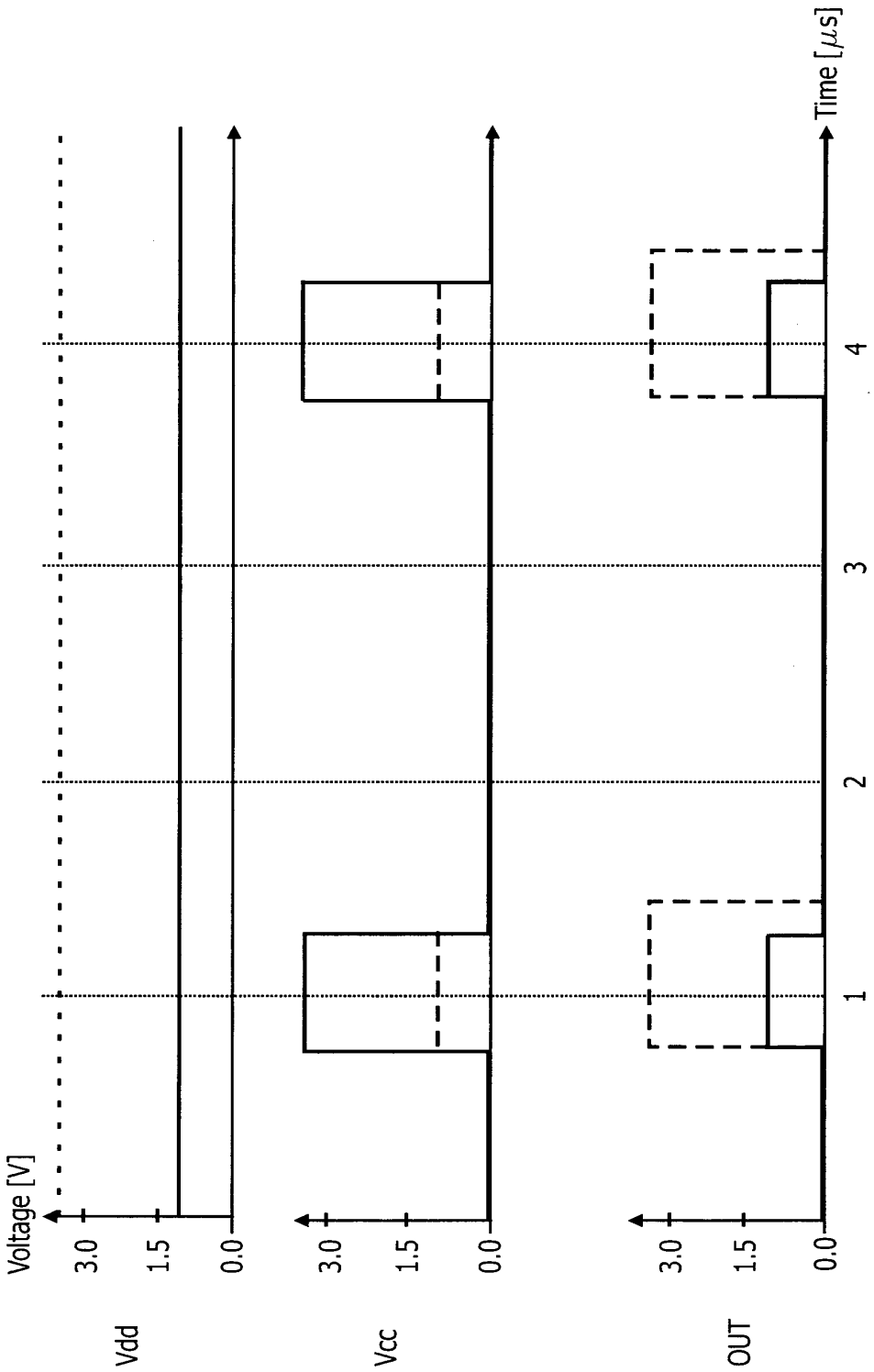


FIG. 4

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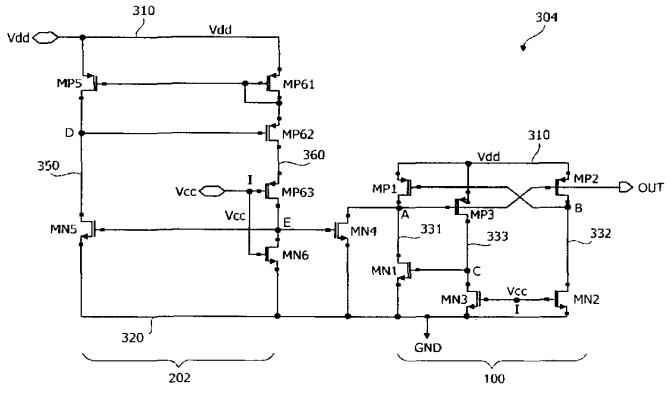
(54) Title: CIRCUIT ARRANGEMENT AND METHOD FOR DETECTING A POWER DOWN SITUATION OF A VOLTAGE SUPPLY SOURCE



(57) Abstract: Circuit arrangement for detecting a power down situation of a second voltage comprising a first conductor, adapted the be connected to a first voltage, a second conductor, adapted the be connected to a reference voltage, an input node, adapted the be connected to the second voltage, and two output nodes, a first output node and a second output node. The output nodes are interconnected in such a manner, that (a) when the second voltage is higher than the reference voltage, the first output node is at the first voltage level and the second output node is at the reference voltage level, and (b) when the second voltage is equal to the reference voltage, the first output node is at the reference voltage level and the second output node is at the first voltage level. The circuit arrangement further comprises an inverter section arranged in between the two conductors, wherein the input node represents an inverter section input and wherein an inverter section output node is formed representing the inverter section output.

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INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2007/050383

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 532 436 A (BISMARCK OTTO H [US]) 30 July 1985 (1985-07-30) abstract column 2, line 59 - column 6, line 49; figure 2	1-3,14
A		4-13,15
X	US 2004/140842 A1 (LEE YUN-WOO [KR] ET AL) 22 July 2004 (2004-07-22) abstract page 2, paragraph 19 - paragraph 26; figure 2	1-3,14
A		4-13,15

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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International application No
PCT/IB2007/050383

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/237099 A1 (TACHIBANA SUGURU [JP] ET AL) 27 October 2005 (2005-10-27) abstract page 4, paragraph 39 page 12, paragraph 144 - page 14, paragraph 163; figures 12,13	1-15
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INTERNATIONAL SEARCH REPORT

International application No
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Electronic Acknowledgement Receipt	
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Application Number:	12365559
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First Named Inventor/Applicant Name:	Chang Ki Kwon
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	072302_IDS_09-08-10.pdf	31772 d7fa32a77f745edc285d03f917ef70f562515638	no	4
Warnings:					
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2	NPL Documents	072302_PCT_ISR_08-05-10.pdf	152716 177eac60284b1724b8f78c73e02397230c23a474	no	4
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3	NPL Documents	072302_PCT_WOPN_08-05-10.pdf	699690 c7fbda3067215f6e8484ec16e4b18f7cd463b576	no	14
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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CONFIRMATION NO. 6210

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

PUBLICATION NOTICE

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Title: Multiple Supply-Voltage Power-Up/Down Detectors

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/365,559	02/04/2009	2115	1674	072302	27	4

CONFIRMATION NO. 6210

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

FILING RECEIPT

OC000000034538592

Date Mailed: 02/25/2009

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Applicant(s)

Chang Ki Kwon, San Diego, CA;
Vivek Mohan, San Diego, CA;

Assignment For Published Patent Application

QUALCOMM INCORPORATED, San Diego, CA

Power of Attorney: The patent practitioners associated with Customer Number 23696

Domestic Priority data as claimed by applicant

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If Required, Foreign Filing License Granted: 02/12/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/365,559**

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Early Publication Request: No

Title

Multiple Supply-Voltage Power-Up/Down Detectors

Preliminary Class

713

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MULTIPLE SUPPLY-VOLTAGE POWER-UP/DOWN DETECTORS

TECHNICAL FIELD

[0001] The present disclosure is related, in general, to integrated circuit devices and, more particularly, to power up/down detectors for multiple supply voltages devices.

BACKGROUND

[0002] As technology has advanced there has been an increased ability to include more and more devices and components within integrated circuits. Semiconductor fabrication techniques have allowed these embedded devices to become smaller and have lower voltage requirements, while still operating at high-speeds. However, because these new integrated devices often interface with older technology devices or legacy products, input/output (I/O) circuits within the integrated circuit have remained at higher operating voltages to interface with the higher voltage requirements of these older systems. Therefore, many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.

[0003] Core devices and applications communicate with operations outside of the integrated component through the I/O devices. In order to facilitate communication between the core and I/O devices, level shifters are employed. Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down. Powering down or power collapsing is a common technique used to save power when no device operations are pending or in progress. For example, if the core network is power collapsed, it is possible that the level shifters, whether through stray currents or the like, could send a signal to the I/O devices for transmission. The I/O devices assume that the core devices have initiated this communication, and will, therefore, transmit the erroneous signal into the external environment.

[0004] It has been found useful to have the I/O devices in a known state when the core networks are powered down. In order to guarantee these known states, solutions have included the addition of hardware or software for managing additional

external signals to control the I/O circuitry. By using these external signals, the I/O circuitry can be controlled (e.g., placed in a known state) whenever the core power is collapsed. However, whether implementing this external signal management system using hardware or software, a considerable amount of delay is added to the operation of the integrated device. Although hardware is slightly faster than software controls, , hardware solutions may have problems caused by significant additional power leakage on the I/O device side.

[0005] One hardware solution currently in use provides power-up/down detectors to generate a power-on/off-control (POC) signal internally. The POC signal instructs the I/O devices when the core devices are shut down. FIGURE 1 is a circuit diagram illustrating standard POC system 10 for multiple supply voltage devices. POC system 10 is made up of three functional blocks: power-up/down detector 100, signal amplifier 101, and output stage 102. Power-up/down detector 100 has PMOS transistor M1 and NMOS transistors M2 – M3. The gate terminals for each of M1-M3 are connected to core power supply 103, V_{core}. When core power supply 103 is power collapsed, M2 and M3 are switched off while M1 is switched on, pulling up the input node to amplifier 105 to $V_{I/O}$, i.e., I/O power supply 104. A "high" signal is input into amplifier 105 which inverts the output to a "low" signal. In output stage 102, the low signal from amplifier 105 is processed in output buffer 106 and again inverted to a high signal for POC 107. The high signal for POC 107 is transmitted to the I/O circuitry indicating that core power supply 103 has been shut down.

[0006] When core power supply 103, V_{core}, is on, M1 becomes very weak and M2 and M3 both switch strongly on, pulling the input node to amplifier 105 to V_{SS}, i.e., core power supply 103. V_{SS} is considered the logical low signal. Therefore, amplifier 105 inverts it to a high signal which is then processed in output buffer 106 and inverted again to a low signal. This signal detection process operates acceptably when either I/O power supply 104 is on and core power supply 103 is power collapsed or when core power supply 103 is powered-up before I/O power supply 104 is powered-up. However, when I/O power supply 104 is powered-up before core power supply 103 powers-up, substantial current leakage may occur in the power up/down detector 100 or in the POC 10.

[0007] In the situation where I/O power supply 104 is on and core power supply 103 is off, M1 is switched on with M2 and M3 switched off. When core power supply 103 is then powered up, M2 and M3 switch on, and M1 becomes very weak. However, before M1 can switch completely off, there is a period in which all three transistors within power up/down detector 100 are on. Thus, a virtual short is created to ground causing a significant amount of current to flow from I/O power supply 104 to ground. This "glitch" current consumes unnecessary power.

[0008] In order to reduce this stray power consumption, one solution may be adopted to decrease the sizes of transistors M1-M3. By reducing the size of M1-M3, the actual amount of current that can pass through the transistors is physically limited. However, because the transistors are now smaller, their switching speeds are also reduced. The reduced switching speed translates into less sensitivity in detecting power-up/down of core supply voltage 103 or longer processing time for power-up/down events.

[0009] FIGURE 2 is an illustration of diagram 20 presenting the signal interactions in POC circuit 10 of FIGURE 1. Diagram 20 includes power supply diagram 21 and POC diagram 22. As I/O power supply 104 is powered up, there is a steady increase until it reaches $V_{I/O}$. POC 107 follows I/O power supply 104 as it powers up to reach the high level. Similarly, when I/O power supply 104 maintains steady at $V_{I/O}$ at time 200, POC 107 remains steady at the high signal. When core power supply 103 begins to power on at time 201 power up/down detector 100 (FIGURE 1) takes a little time to actually detect this new power level. Once detected, at time 202, POC 107 is switched to the low value. POC 107 should, thereafter, remain at the low level until core power supply 103 is power collapsed, between times 203 and 205. Again, because power up/down detector 100 (FIGURE 1) takes a little time to actually detect the new power level, POC 107 remains in the low state until time 204, when the powering down is actually detected by power up/down detector 100. This low state time, between time 202 and 204 is referred to as the normal operation region. Once core power supply 103 is completely off or power collapsed at time 205, the input to amplifier 105 (FIGURE 1) is again pulled up to the high signal. POC 107 will then follow I/O power supply 104 as it also powers down between times 206 and 207.

[0010] The leakage current between I/O power supply 104 and ground can be lessened because of the smaller transistor size. Thus, during the time between times 201 and 205 any leakage that occurs is reduced. However, this reduced leakage comes at the price of faster detection. If POC circuit 10 may include the lower-threshold or bigger transistors, switching/detecting times would be faster. For example, as core power supply 103 begins to power up at time 201, the lower-threshold or bigger transistors of power up/down detector 100 would detect the power-up at time 208, instead of time 202. Moreover when core power supply 103 begins powering down at time 203, the power up/down detector 100 would detect the power-down at time 209, instead of time 204. This increase may be represented by the difference between the time periods of time 202 to 204 vs. time 208 to 209. Therefore, the conventional solutions still have problems with leakage and switching times.

SUMMARY

[0011] Various representative embodiments of the disclosure relate to integrated devices having multiple supply voltages. Further representative embodiments of the present disclosure relate to methods for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device. Additional representative embodiments of the present disclosure relate to systems for reducing power consumption in a POC network of a multiple supply voltage device.

[0012] A multiple supply voltage device includes a core network operative at a first supply voltage and a control network coupled to the core network. The control network is configured to transmit a control signal. The control network includes an up/down (up/down) detector configured to detect a power state of the core network. The control network further includes processing circuitry coupled to the up/down detector and is configured to generate the control signal based on the power state. The control network further includes one or more feedback circuits coupled to the up/down detector. The one or more feedback circuits are configured to provide feedback signals to adjust a current capacity of said up/down detector.

[0013] A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device includes detecting a power-on of a second supply voltage while a first supply voltage is already on, decreasing a current capacity of a power on/off detector of the POC network in response to the power-on detection, detecting a power-down of the second supply voltage while the first supply voltage is on, and increasing the current capacity of the power on/off detector in response to the power-down detection.

[0014] A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device includes a means for detecting a power-on of a second supply voltage while a first supply voltage is already on. The system further includes means for decreasing a current capacity of a power on/off detector of the POC network responsive to the power-on detection. The system further includes means for detecting a power-down of the second supply voltage while the first supply voltage is on, and means for increasing the current capacity of the power on/off detector responsive to the power-down detection.

[0015] The foregoing has outlined rather broadly the features and technical advantages of the present embodiments in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the embodiments will be described hereinafter which form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims. The novel features which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] For a more complete understanding of the present disclosure, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

[0017] FIGURE 1 is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices.

[0018] FIGURE 2 is an illustration of a diagram presenting the signal interactions in the POC circuit of FIGURE 1.

[0019] FIGURE 3A is a block diagram illustrating an integrated circuit (IC) device having a power on control (POC) network configured according to the teachings of the present disclosure.

[0020] FIGURE 3B is a block diagram illustrating a POC network configured according to the teachings of the present disclosure.

[0021] FIGURE 4 is a circuit diagram illustrating another POC network configured according to the teachings of the present disclosure.

[0022] FIGURE 5 is a circuit diagram illustrating a further POC network configured according to the teachings of the present disclosure.

[0023] FIGURE 6 is a circuit diagram illustrating still another POC network configured according to the teachings of the present disclosure.

[0024] FIGURE 7 is a flowchart illustrating process blocks for implementing one embodiment according to the teachings of the present disclosure.

FIGURE 8 is a diagram illustrating an exemplary wireless communication system.

DETAILED DESCRIPTION

[0025] Turning now to FIGURE 3A, a block diagram is presented illustrating an integrated circuit (IC) device 30 having a power on control (POC) network 305 configured according to one embodiment of the present disclosure. The IC

device 30 is an integrated circuit that includes embedded components powered by multiple power supplies, such as the $V_{I/O}$ 300 and the V_{core} 301. The$V_{I/O}$ 300 and the V_{core} 301 supply several different voltage level power supplies to different components and networks within the IC device 30. Two such embedded networks are the I/O network 302 and the core network 303. The I/O network 302 operates at a voltage level provided by the $V_{I/O}$ 300. The Core network 303 operates at a voltage level provided by the V_{core} 301, which is usually a lower voltage than that provided by the $V_{I/O}$ 300. Because the I/O network 302 and the core network 303 operate at different voltages, they are coupled together through level shifters 304 for communication. The level shifters 304 essentially shift the voltage levels of any communications that occur between the I/O network 302 and the core network 303.

[0026] POC network 305 senses the status of the core network 303 and transmits a POC signal to the I/O network 302 and level shifters 304. The POC signal either turns them on or off. This prevents stray signals received by the I/O network 302 from being mistakenly transmitted to devices or components external to the IC device 30.

[0027] FIGURE 3B is a block diagram illustrating a POC network 305 configured according to one embodiment of the present disclosure. The POC network 305 includes a power up/down detector 306, processing circuitry 307, and feedback network 310. The processing circuitry 307 is made up of a signal processor 308 and an output buffer 309. When the $V_{I/O}$ 300 is on and the V_{core} 301 is off, the power up/down detector 306 provides a detection signal to the signal processor 308, which processes the detection signal and transmits the processed signal to the output buffer 309. The output buffer 309 then conditions the processed signal into a POC signal 311, which is then transmitted to an I/O network 302. Along the way, a feedback network 310 receives feedback from the signal processor 308 and feeds that signal back to the power up/down detector 306. The power up/down detector 306 uses the feedback signal to adjust its current capacity. While the V_{core} 301 is in an off or low state, the feedback signal allows the power up/down detector 306 to select a maximum current capacity. This maximum current capacity state makes the power up/down detector 306 more sensitive to detecting when the V_{core} 301 either powers-up or powers-down, or both, depending on the circuit configuration of the power up/down detector 306.

[0028] When the V_{core} 301 powers-up while the $V_{I/O}$ 300 is on, the power up/down detector 306 detects the power-up and changes the value of the detection signal transmitted to the signal processor 308. The process detection signal is then conditioned by the output buffer 309 into the changed POC signal 311 and transmitted to the I/O network 302. With the changing signals being processed through the signal processing circuitry 307, the feedback network 310 receives the new feedback signal that, when input into power the up/down detector 306, causes the current capacity within the power up/down detector 306 to decrease. This decrease in current capacity will limit and reduce the amount of leakage current that may be dissipated through the power up/down detector 306 because of its connections to the $V_{I/O}$ 300 and the V_{core} 301.

[0029] FIGURE 4 is a circuit diagram illustrating a POC network 40 configured according to one embodiment of the present disclosure. The POC network 40 has similar processing regions as the POC network 305 (FIGURE 3A and 3B), i.e., a power up/down detector 306, a signal processor 308, an output buffer 309, and a feedback network 310. The POC network 40 also generates a POC signal 311 and is coupled to a $V_{I/O}$ 300 and a V_{core} 301. As shown in the embodiment illustrated in FIGURE 4, the power up/down detector 306 comprises multiple transistors M4-M7 coupled in series together. Each gate of the transistors M4-M7 is coupled to the V_{core} 301, while the source terminal of the transistor M4 is coupled to the $V_{I/O}$ 300. The transistors M4 and M5 are p-type transistors and the transistors M6 and M7 are n-type transistors. Therefore, when the V_{core} 301 is off, i.e., in a low state, the transistors M4 and M5 are switched on, while the transistors M6 and M7 are switched off.

[0030] In contrast, when the V_{core} 301 is on, i.e., in a high state, transistors M4 and M5 become very weak while transistors M6 and M7 are strongly switched on. M6 and M7 turning on pulls the voltage of the input to inverting amplifier to V_{SS}, which is a logical low signal compared with $V_{I/O}$. V_{SS} is designed as the logical low signal and may comprise ground, 0 V, or some other selected voltage level that represents the logical low symbol. Thus, when the V_{core} 301 is off, the transistors M4 and M5 pull up the voltage level at the input to an inverting amplifier 400 to the $V_{I/O}$ 300. Therefore, the input to the inverting amplifier 400 is high when the V_{core} 301 is off and low when the V_{core} 301 is on. The inverting amplifier 400 then amplifies and inverts the detection

signal before transmitting it to the inverting buffer 401 for conditioning and inverting for the POC signal 311.

[0031] The feedback network 310 comprises a transistor M8 connected in parallel to the transistor M4. The transistor M8 is also configured as a p-type transistor, such that when the feedback signal from the inverting amplifier 400 is high, the transistor M8 is switched off, and when the feed back signal is low, the transistor M8 is switched on. Thus, when the V_{core} 301 is off, producing a high detection signal, the inverting amplifier 400 inverts that signal to a logic low which causes the transistor M8 to switch on. As the V_{core} 301 is powered-on, the detection signal changes to a logic low, which changes the feedback signal from the inverting amplifier 400 to a logic high, which, in turn, turns the transistor M8 off. While the transistor M8 is off, the power up/down detector 306 has a decreased current capacity, i.e., smaller current will flow through the transistor M8 because of the amplified low signal. The voltage level caused by the V_{core} 301 on the gate terminals of M4 and M5 could in some glitch or stray signal situations, cause leakage through M4 and M5. Because the feedback signal for the transistor M8 is received from the inverting amplifier 400, when the V_{core} 301 powers-down, the feedback signal will switch quickly from a logic high to a logic low, which will then switch the transistor M8 on. Thus, in the circuit configuration depicted in FIGURE 4, the power up/down detector 40 will detect the V_{core} 301 powering down more quickly than the existing POC networks.

[0032] FIGURE 5 is a circuit diagram illustrating a POC network 50 configured according to one embodiment of the present disclosure. The POC network 50 comprises multiple transistors M4-M7 in the power up/down detector 306 coupled together in a fashion similar to the POC network 40 (FIGURE 4) with each gate coupled to a V_{core} 301, and the source terminal of the transistor M4 coupled to a $V_{I/O}$ 300. A signal processor 308 comprises an inverting amplifier 400, and an output buffer 309 includes an inverting buffer 401. The POC network 50 generates a POC signal 311, which will be transmitted to the I/O network to which the POC network 50 is coupled. In the POC network 50, a feedback network 310 is configured with the transistors M9 and M10 coupled in parallel with the transistor M7. The transistors M6, M7, M10, are the same type, n-type or can be low-threshold n-type transistors to speed up the power-

on detection. The transistor M9 receives its feedback signal from the output of the inverting buffer 401, while the gate of the transistor M10 is connected to the V_{core} 301.

[0033] In operation, when the $V_{I/O}$ 300 is on and the V_{core} 301 is off, the inverting amplifier 400 receives a logic high signal by virtue of the $V_{I/O}$ 300, which, when amplified and inverted by the inverting amplifier 400 and then conditioned and inverted by the inverting buffer 401, provides a logic high feedback signal. This high signal would normally switch M9 in the feedback network 310 on. However, because M6, M7, and M10 are all off, there is no channel formation within the transistor M9 to switch it on. When the V_{core} 301 powers on, M4 and M5 become very weak, while M6, M7, and M10 switch on, which immediately causes M9 to switch on because its gate is already connected to a logic high input. M6 and M7 switching on pulls the input to the inverting amplifier 400 down to a logical low signal, i.e., V_{SS}. The low detection signal input to the inverting amplifier 400 is amplified and inverted and then conditioned and inverted again at the inverting buffer 401. Once the inverting buffer 401 outputs a low signal, the feedback of that low to the transistor M9 will switch M9 off, which, because switching M9 off stops the channel formation in the transistor M10, causes the transistor M10 to also switch off. Thus, the configuration of the POC network 50, as illustrated in FIGURE 5, operates to detect the V_{core} 301 powering on faster than the existing POC networks, while still reducing the amount of leakage current while the V_{core} 301 is on. The feedback signal used by the transistor M9 allows the power up/down detector 306 to adjust its current capacity, which reduces the leakage current at the same time as the detection speed is improved.

[0034] FIGURE 6 is a circuit diagram illustrating a POC network 60 configured according to one embodiment of the present disclosure. The POC network 60 includes a feedback network 310 configured according to the circuit arrangements of both the POC network 40 (FIGURE 4) and the POC network 50 (FIGURE 5). As such, multiple transistors M4-M7 make up the power up/down detector 306. The feedback network 310 includes transistor M8, coupled in parallel to the transistor M4, and the transistors M9 and M10, coupled in parallel with the transistor M7. The detection signal from the power up/down detector 306 provides input to an inverting amplifier 400 of a signal processor 308, which amplifies and inverts the detection signal for input to an inverting buffer 401 of an output buffer 309. The conditioned and inverted POC

signal 311 is then transmitted to the appropriate I/O and level shifter network of the system. The feedback transistor M8 obtains its feedback signal from the output of the inverting amplifier 400, while the feedback transistor M9 obtains its feedback signal from the output of the inverting buffer 401. Using these feedback signals, as described with respect to the POC network 40 (FIGURE 4) and the POC network 50 (FIGURE 5), the POC network 60 is able to increase the speed that the V_{core} 301 is quickly detected both in the power-on and power-off stages. At the same time, because the feedback network 310 provides the capability of the POC network 60 to adjust the current capacity of the power up/down detector 306, the unwanted leakage current can also be reduced during the V_{core} 301 normal operation periods.

[0035] It should be noted that each of the embodiments described with respect to the POC network 40 (FIGURE 4), the POC network 50 (FIGURE 5), and the POC network 60 (FIGURE 6) has its own advantages. For example, the POC network 50 (FIGURE 5) is able to have a considerably improved performance characteristic with the addition of very small thin-oxide circuitry to the overall silicon. Thus, each of the illustrated embodiments, as well as the various additional and/or alternative embodiments of the present disclosure represent improvements over the existing systems and methods.

[0036] FIGURE 7 is a flowchart illustrating process blocks for implementing one embodiment of the present disclosure. In block 700, a power-on of a second supply voltage is detected while a first supply voltage is already on. At block 701 a current capacity of a power on/off detector of the POC network is decreased responsive to the power-on detection. At block 702 a power-down of the second supply voltage is detected while the first supply voltage is on. At block 703 the current capacity of the power on/off detector is increased responsive to the power-down detection.

[0037] Figure 8 is a diagram illustrating an exemplary wireless communication system. In some embodiments, a system 800 includes multiple remote units 820-824 and multiple base stations 850-852. It can be recognized that typical wireless communication systems may have many more remote units and base stations. The remote units 820-824 include multiple semiconductor devices 830-834 having power detection, as discussed above. Figure 8 shows a forward link signals 880 from the base

stations 850-852 and the remote units 820-824 and a reverse link signals 890 from the remote units 820-824 to the base stations 850-852.

[0038] In other embodiments, Figure 8 the remote unit 820 is shown as a mobile telephone, the remote unit 822 is shown as a portable computer, and the remote unit 824 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, navigation devices (e.g., GPS enabled devices,) set-top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Although Figure 8 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. The disclosed device may be suitably employed in any device which includes a semiconductor device.

[0039] Although specific circuitry has been set forth, it will be appreciated by those skilled in the art that not all of the disclosed circuitry is required to practice the disclosure. Moreover, certain well known circuits have not been described so as to maintain focus on the disclosure. Similarly, although the description refers to logical "0" or "low" and logical "1" or "high" in certain locations, one skilled in the art appreciates that the logical values can be switched, with the remainder of the circuit adjusted accordingly, without affecting operation of the present disclosure.

[0040] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the embodiments of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present

disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A multiple supply voltage device comprising:

a core network operative at a first supply voltage; and

a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising:

an up/down (up/down) detector configured to detect a power state of said core network;

processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state; and

one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector.

2. The multiple supply voltage device of claim 1 wherein said up/down detector comprises:

one or more first transistors coupled to a second supply voltage, wherein said one or more first transistors are configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on; and

one or more second transistors coupled to said one or more first transistors in series and coupled to said first supply voltage, wherein said one or more second transistors are configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down.

3. The multiple supply voltage device of claim 2 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry, wherein said one or more first feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

4. The multiple supply voltage device of claim 2 wherein said one or more feedback circuits comprise:

one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry, wherein said one or more second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

5. The multiple supply voltage device of claim 2 wherein said one or more feedback circuits comprise:

one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry; and

one or more second feedback transistors coupled in parallel with said one or more second transistors and coupled to receive feedback from said processing circuitry;

wherein said one or more first and second feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on.

6. The multiple supply voltage device of claim 1 wherein said processing circuitry comprises:

a comparator configured to output a detection signal based on an input signal received from said adjustable current power up/down detector; and

an output buffer configured to process said detection signal into said control signal.

7. The multiple supply voltage device of claim 1 further comprising:
an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal.

8. The multiple supply voltage device of claim 1, in which the device is integrated into a semiconductor die.

9. The multiple supply voltage device of claim 8, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

10. A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising:

detecting a power-on of a second supply voltage while a first supply voltage is already on;

decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection;

detecting a power-down of said second supply voltage while said first supply voltage is on; and

increasing said current capacity of said power on/off detector in response to said power-down detection.

11. The method of claim 10 wherein said detecting said power-on comprises:

receiving a logic-high signal at a control gate of one or more first transistors and one or more second transistors, wherein said one or more first transistors are configured to switch off in response to said logic-high signal, and wherein said one or more second transistors are configured to switch on in response to said logic-high signal; and

transmitting a detection signal to a signal processor from said one or more second transistors based on said received logic-high signal.

12. The method of claim 11 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching off said one or more first feedback transistors in response to said first feedback signal.

13. The method of claim 11 wherein said decreasing said current capacity comprises:

receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

14. The method of claim 11 wherein said decreasing said current capacity comprises:

receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;

switching off said one or more first feedback transistors in response to said first feedback signal;

receiving a second feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching off said one or more second feedback transistors in response to said second feedback signal.

15. The method of claim 10 wherein said detecting said power-down comprises:

receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and

transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

16. The method of claim 15 wherein said increasing said current capacity comprises:

receiving a third feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and

switching on said one or more first feedback transistors in response to said third feedback signal.

17. The method of claim 15 wherein said increasing said current capacity comprises:

receiving a fourth feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said fourth feedback signal.

18. The method of claim 15 wherein said increasing said current capacity comprises:

receiving a third feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors;

switching on said one or more first feedback transistors in response to said third feedback signal;

receiving a fourth feedback signal from an output buffer of said POC network at one or more second feedback transistors coupled in parallel with said one or more second transistors; and

switching on said one or more second feedback transistors in response to said fourth feedback signal.

19. The method of claim 10, wherein the multiple supply voltage device is applied in an electronic device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer, into which a semiconductor device is integrated.

20. A system for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said system comprising:

means for detecting a power-on of a second supply voltage while a first supply voltage is already on;

means, responsive to said power-on detection, for decreasing a current capacity of a power on/off detector of said POC network;

means for detecting a power-down of said second supply voltage while said first supply voltage is on; and

means, responsive to said power-down detection, for increasing said current capacity of said power on/off detector.

21. The system of claim 20 further comprising:

means for providing a feedback signal associated with at least one of: said detected power-on or said detected power-down, wherein said feedback signal is used in said means for decreasing and said means for increasing.

22. The system of claim 21 wherein said means for decreasing said current capacity comprises:

means, responsive to said feedback signal, for switching off one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

23. The system of claim 21 wherein said means for increasing said current capacity comprises:

means, responsive to said feedback signal, for switching on one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector.

24. The multiple supply voltage device of claim 20, in which the device is integrated into a semiconductor die.

25. The multiple supply voltage device of claim 24, in which the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer.

26. A method for reducing power consumption in a power on/off control (POC) network of a multiple supply voltage device, said method comprising the steps of:

detecting a power-on of a second supply voltage while a first supply voltage is already on;

decreasing a current capacity of a power on/off detector of said POC network in response to said power-on detection;

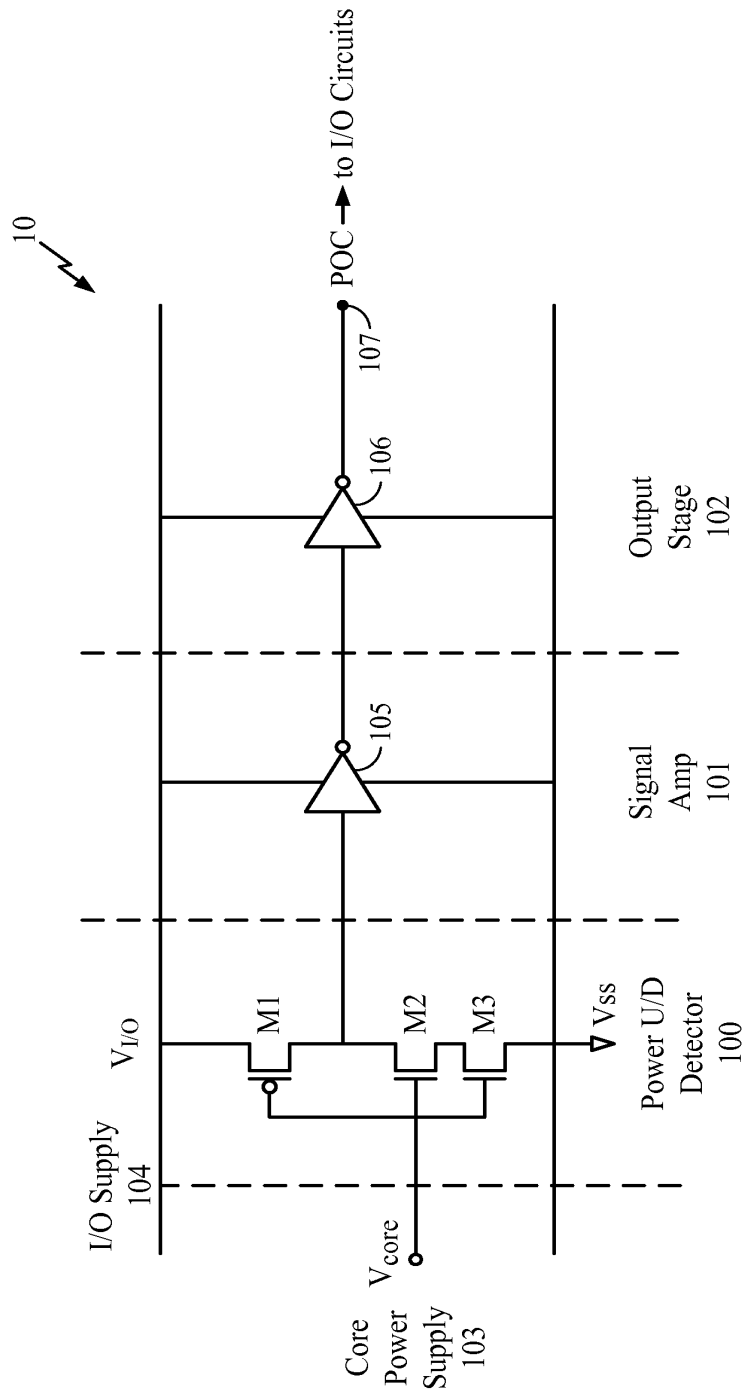
detecting a power-down of said second supply voltage while said first supply voltage is on; and

increasing said current capacity of said power on/off detector in response to said power-down detection.

27. The method of claim 26, wherein the multiple supply voltage device is applied in an electronic device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer, into which a semiconductor device is integrated.

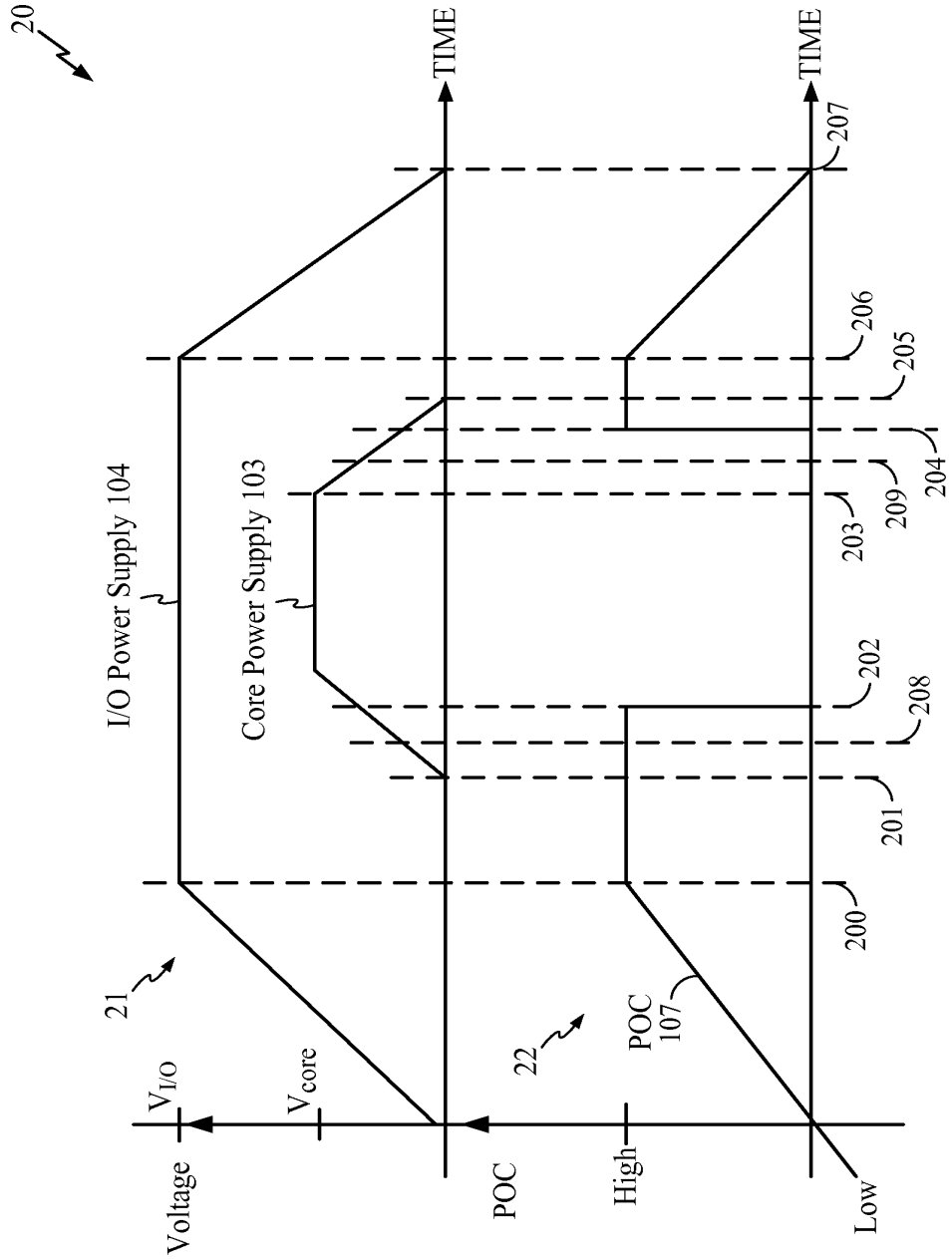
ABSTRACT

A multiple supply voltage device includes an input/output (I/O) network operative at a first supply voltage, a core network coupled to the I/O network and operative at a second supply voltage, and a power-on-control (POC) network coupled to the I/O network and the core network. The POC network is configured to transmit a POC signal to the I/O network and includes an adjustable current power up/down detector configured to detect a power state of the core network. The POC network also includes processing circuitry coupled to the adjustable current power up/down detector and configured to process the power state into the POC signal, and one or more feedback circuits. For reducing the leakage current while also improving the power-up/down detection speed, the feedback circuit(s) are coupled to the adjustable current power up/down detector and configured to provide feedback signals to adjust a current capacity of the adjustable current power up/down detector.



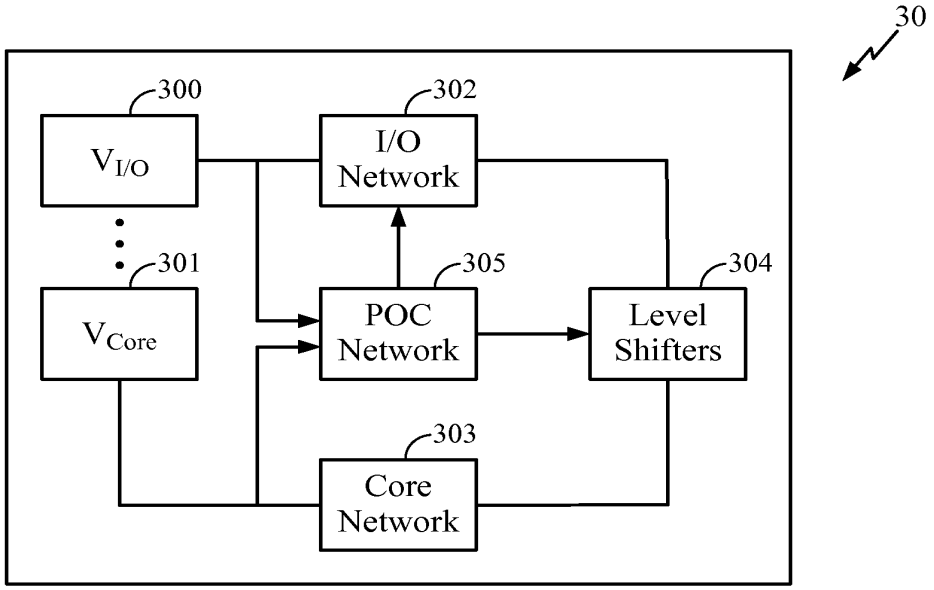
(PRIOR ART)

FIG. 1



(PRIOR ART)

FIG. 2


30
300
302
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I/O Network
301
305
304
V_{Core}
POC Network
Level Shifters
303
Core Network

FIG. 3A

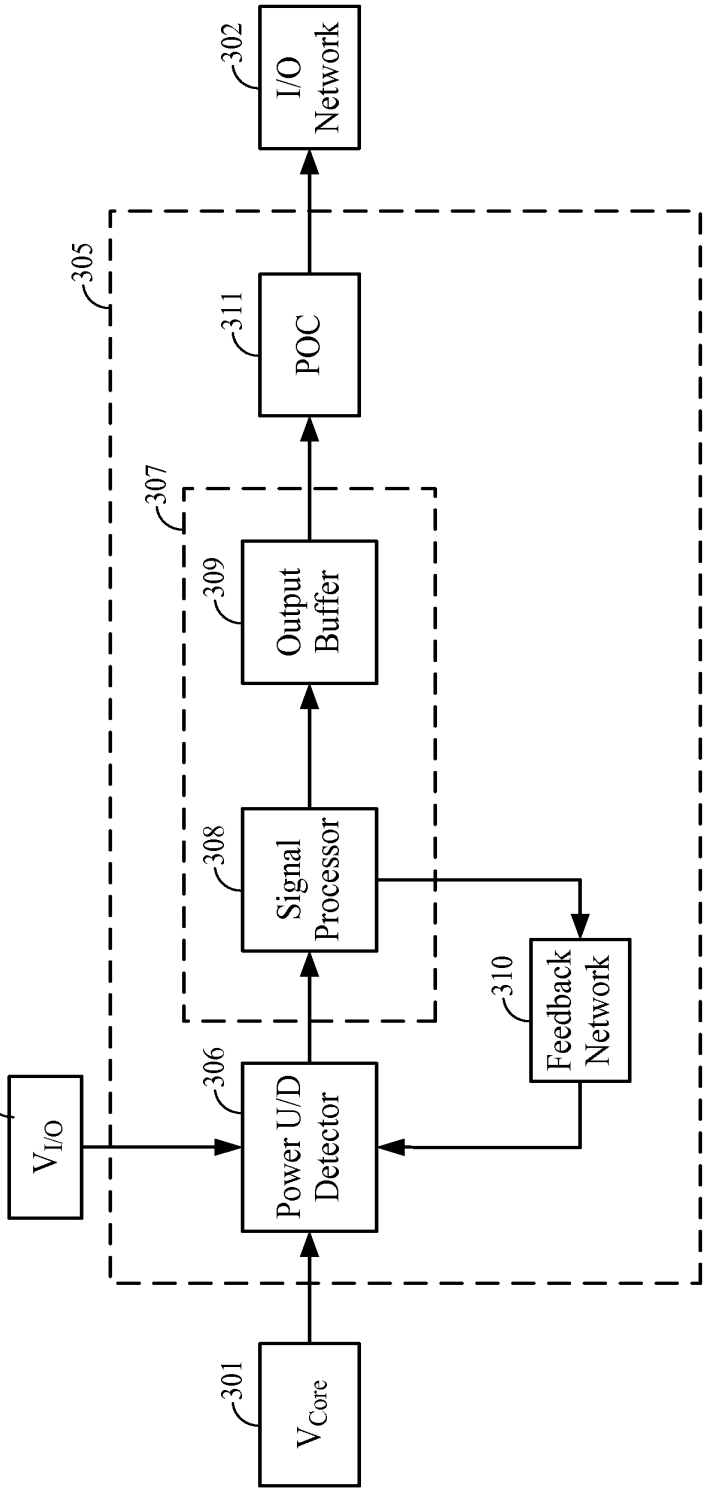
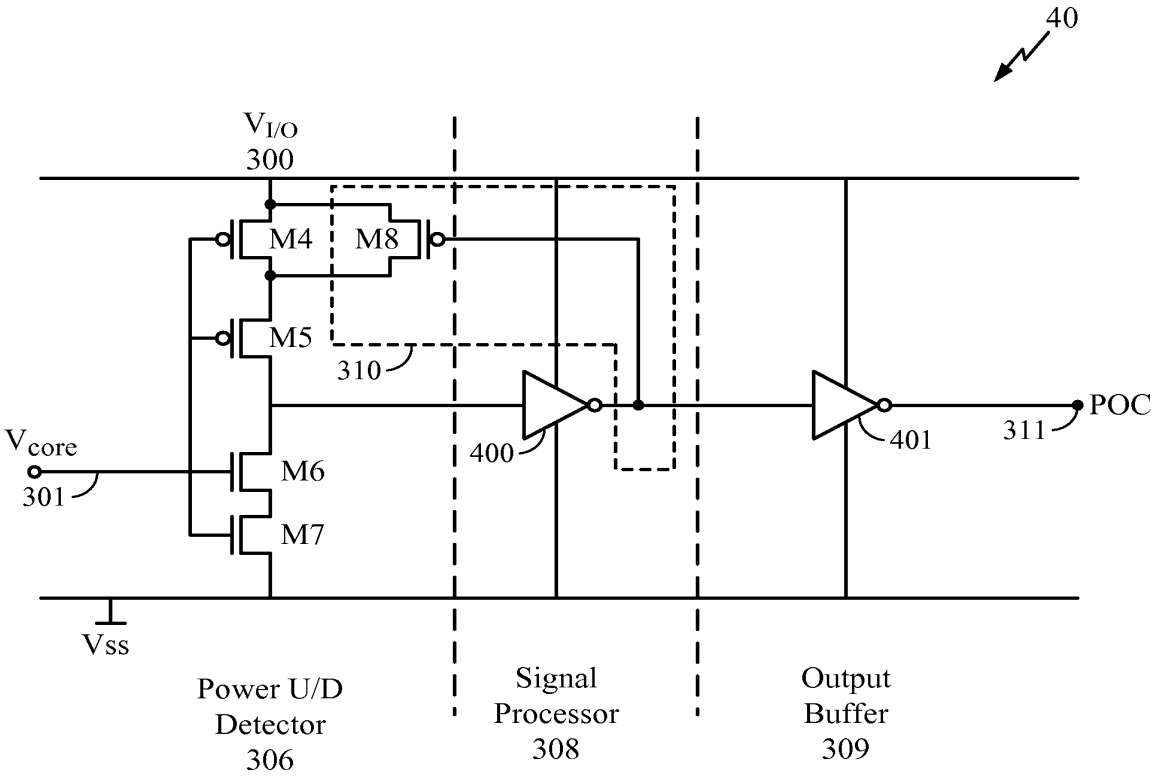

302
I/O Network
305
311
POC
307
309
Output Buffer
308
Signal Processor
310
Feedback Network
300
$V_{I/O}$
306
Power U/D Detector
301
V_{Core}

FIG. 3B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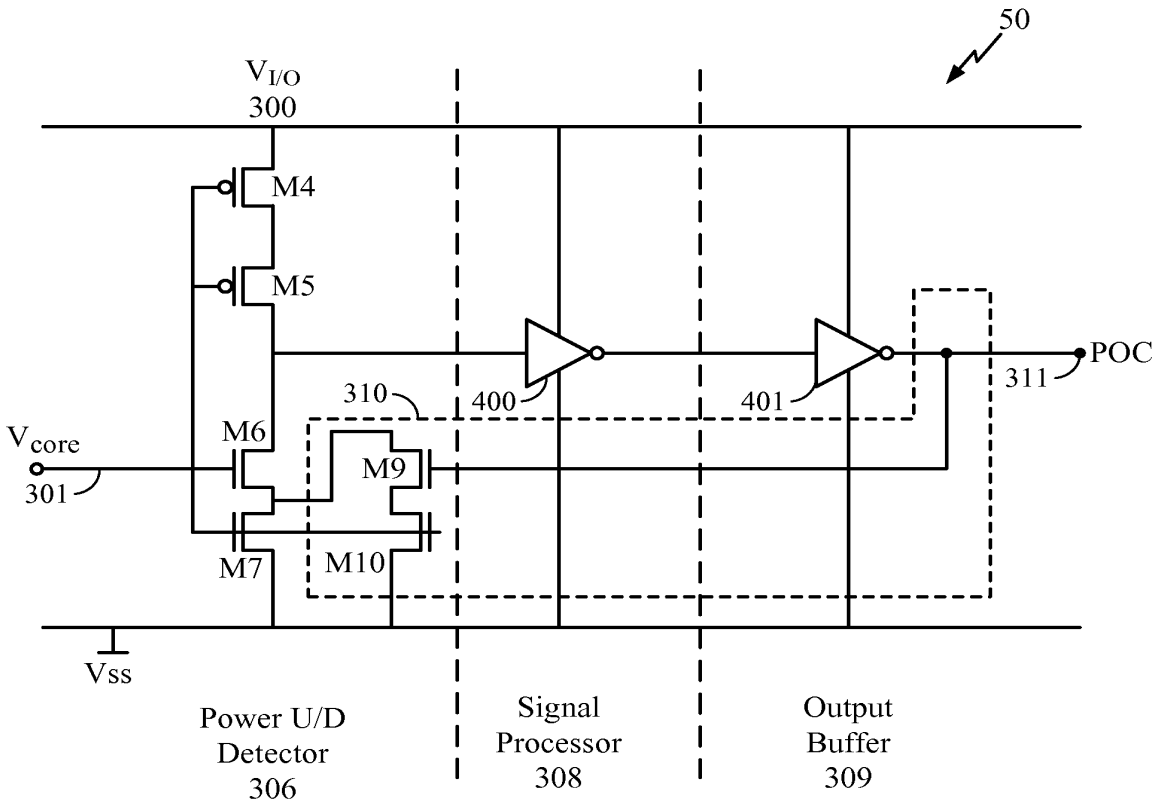
$V_{I/O}$
300
M4
M8
M5
310
V_{core}
301
M6
M7
Vss
400
401
311
POC
Power U/D
Detector
306
Signal
Processor
308
Output
Buffer
309

FIG. 4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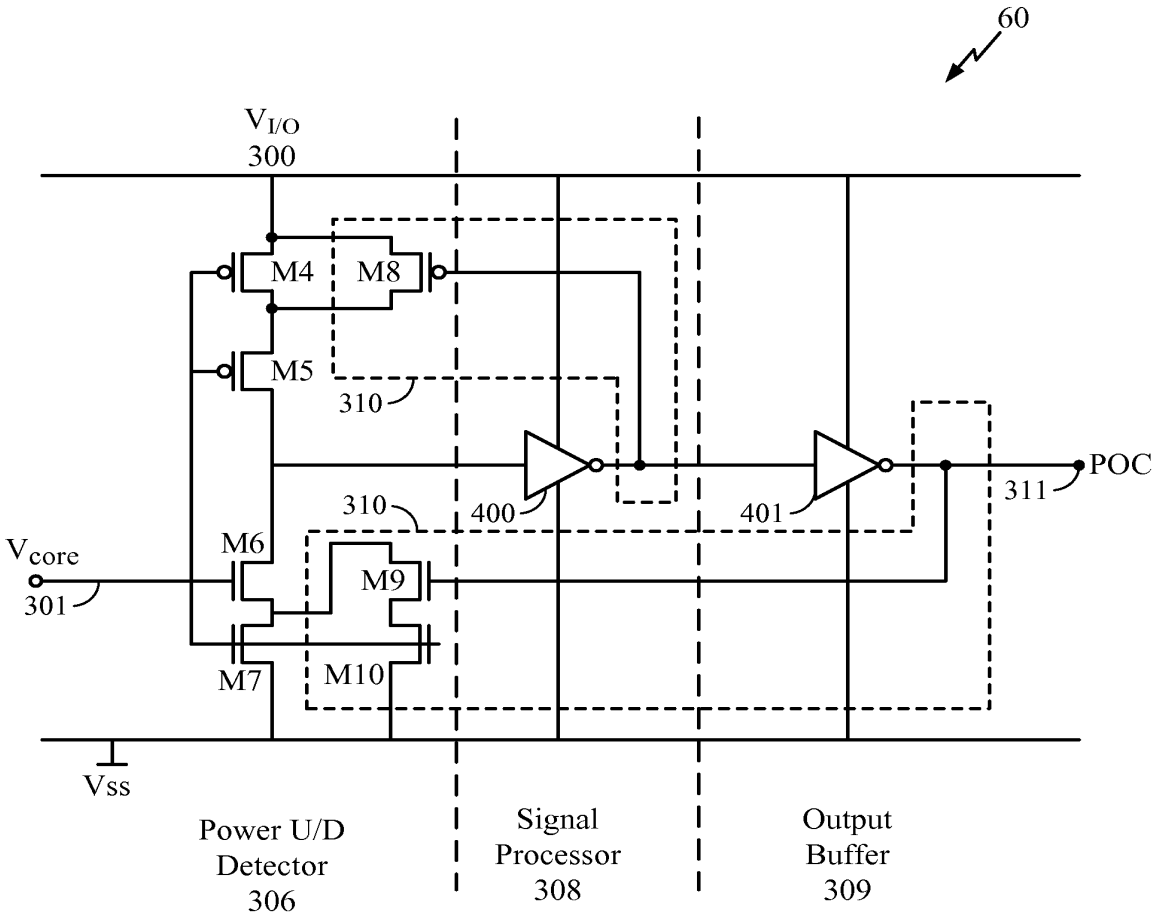
$V_{I/O}$
300
M4
M5
310
400
401
311
POC
V_{core}
301
M6
M9
M7
M10
Vss
Power U/D
Detector
306
Signal
Processor
308
Output
Buffer
309

FIG. 5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$V_{I/O}$
300
M4
M8
M5
310
310
400
401
311
POC
V_{core}
301
M6
M9
M7
M10
Vss
Power U/D
Detector
306
Signal
Processor
308
Output
Buffer
309

FIG. 6

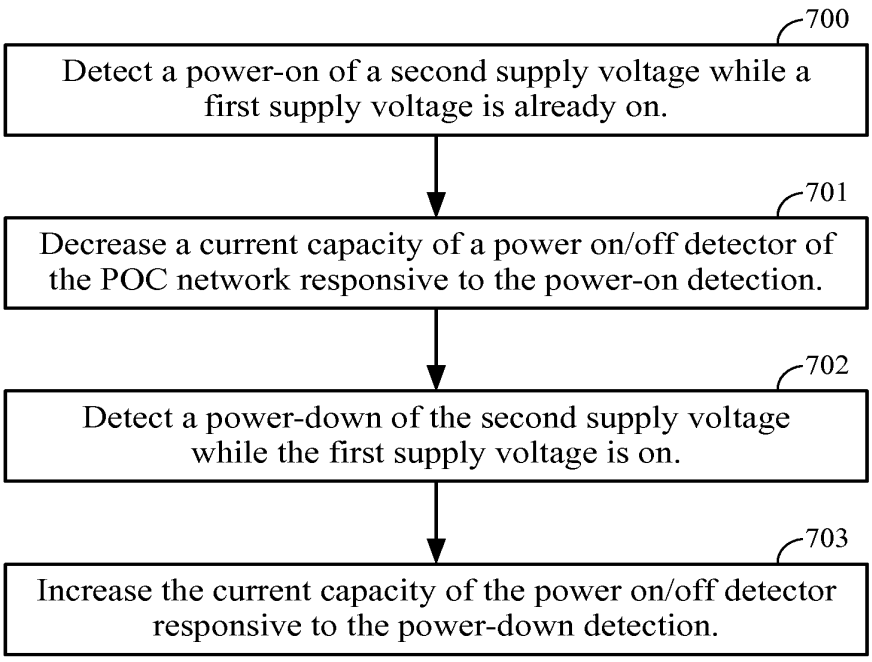
700
Detect a power-on of a second supply voltage while a first supply voltage is already on.
701
Decrease a current capacity of a power on/off detector of the POC network responsive to the power-on detection.
702
Detect a power-down of the second supply voltage while the first supply voltage is on.
703
Increase the current capacity of the power on/off detector responsive to the power-down detection.

FIG. 7

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	072302
	Application Number	
Title of Invention	Multiple Supply-Voltage Power-Up/Down Detectors	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chang	Ki	Kwon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence [i]	US

Citizenship under 37 CFR 1.41(b) [i] KR

Mailing Address of Applicant:

Address 1	8399 Katherine Claire Lane
Address 2	

City	San Diego	State/Province	CA
Postal Code	92127	Country[i]	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vivek		Mohan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence [i]	US

Citizenship under 37 CFR 1.41(b) [i] US

Mailing Address of Applicant:

Address 1	11756 Springside Road
Address 2	

City	San Diego	State/Province	CA
Postal Code	92128	Country[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	072302
	Application Number	
Title of Invention	Multiple Supply-Voltage Power-Up/Down Detectors	

Customer Number	23696		
Email Address	us-docketing@qualcomm.com	Add Email	Remove Email
Email Address	nc.docketing@qualcomm.com	Add Email	Remove Email

Application Information:

Title of the Invention	Multiple Supply-Voltage Power-Up/Down Detectors		
Attorney Docket Number	072302	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	08	**Suggested Figure for Publication (if any)**	3B

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23696		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	072302
	Application Number	
Title of Invention	Multiple Supply-Voltage Power-Up/Down Detectors	

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◯ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	QUALCOMM Incorporated		
Mailing Address Information:			
Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Country [i]	US	Postal Code	92121
Phone Number	(858) 658-5787	Fax Number	(858) 658-2502
Email Address	us-docketing@qualcomm.com; nc.docketing@qualcomm.com		

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Sam Talpalatsky/			Date (YYYY-MM-DD)	2009-02-03
First Name	Sam	Last Name	Talpalatsky	Registration Number	35380

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Multiple Supply-Voltage Power-Up/Down Detectors
First Named Inventor/Applicant Name:	Chang Ki Kwon
Filer:	Nicholas John Pauley/Joann Denbow
Attorney Docket Number:	072302

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	7	52	364
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1674**

Electronic Acknowledgement Receipt	
EFS ID:	4734637
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	Multiple Supply-Voltage Power-Up/Down Detectors
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	072302
Receipt Date:	04-FEB-2009
Filing Date:	
Time Stamp:	16:13:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1674
RAM confirmation Number	1626
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		072302_APP_02-04-09.pdf	124914 7b9ab52e70865ba83804180d6e225e9e3ba1c683	yes	21

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	13
Claims	14	20
Abstract	21	21

Warnings:					
Information:					
2	Oath or Declaration filed	072302_DEC_02-04-09.pdf	427200 a298959790fb007cc634c1e21ad148aac906d538	no	2
Warnings:					
Information:					
3	Drawings-only black and white line drawings	072302_FMLDWG_02-04-09.pdf	144673 0775e64bfc9293dfe76951ca31bcb5a6621e42f0	no	8
Warnings:					
Information:					
4	Application Data Sheet	072302_ADS_02-04-09_ST.pdf	764808 490e97c8af923d0acdc4b428c4fa9e21c9be4dee	no	4
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	37560 a6a4630670e8b8bb0f0466727e9a01bc19f55268	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1499155		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Chang Ki Kwon et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7253655		2007-08-07	Kwon et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Chang Ki Kwon et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chang Ki Kwon et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	072302

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Sam Talpalatsky/	Date (YYYY-MM-DD)	2009-02-03
Name/Print	Sam Talpalatsky	Registration Number	35380

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	4735029
Application Number:	12365559
International Application Number:	
Confirmation Number:	6210
Title of Invention:	Multiple Supply-Voltage Power-Up/Down Detectors
First Named Inventor/Applicant Name:	Chang Ki Kwon
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	072302
Receipt Date:	04-FEB-2009
Filing Date:	
Time Stamp:	16:34:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	072302_IDS_PTOSB08_02-03-09_ST.pdf	521580 f9db55b472fb94ea6af51d8e2600a69f1dd2c26f	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	521580

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

COMBINED DECLARATION / POWER OF ATTORNEY

AS BELOW NAMED INVENTOR, I HEREBY DECLARE THAT: This Declaration is of the following type:

☒ Original ☐ Supplemental ☐ Continuation-In-Part ☐ Divisional
☐ Continuation ☐ National Stage of PCT

My residence, post office address and citizenship are as stated below next to my name: I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention "Multiple Supply-Voltage Power-Up/Down Detectors" the specification of which:

☒ is attached hereto.
☐ was filed on as Serial No.
☐ was amended on (if applicable).
☐ was described and claimed in PCT International Application No. filed on and as amended under PCT Article 19 on

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to be material to patentability of this application in accordance with 37 CFR 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 of any foreign application(s) for patent or inventor's certificate or of any PCT International application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

			Priority Claimed	
(Country)	(Application No.)	(Day/Month/Year/Filed)	(Yes)	(No)

I hereby claim the benefit under Title 35 USC 119(e) of any United States provisional application(s) listed below:

(Serial No.)	(Filing Date)

I hereby claim the benefit under Title 35 USC 120 of the United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 USC 112, I acknowledge the duty to disclose all information known to be material to patentability of this application in accordance with 37 CFR 1.56 which occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status)

I, the undersigned, hereby appoint the attorneys and/or agents associated with Customer No. 23696 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith. Please direct all telephone calls to Kelly Scanlan at (858) 845-4265 and address all correspondence to: QUALCOMM Incorporated, Patent Department/Central Administration, 5775 Morehouse Drive, San Diego, California 92121-1714.

I, the undersigned, hereby declare under penalty of perjury that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Joint Inventor	Inventor Signature	Date
Chang Ki Kwon		Nov. 5, 2008
Residence		Citizenship
8399 Katherine Claire Lane, San Diego, CA 92127		Korea
Post Office Address		

I, the undersigned, hereby appoint the attorneys and/or agents associated with Customer No. 23696 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith. Please direct all telephone calls to Kelly Scanlan at (858) 845-4265 and address all correspondence to: QUALCOMM Incorporated, Patent Department/Central Administration, 5775 Morehouse Drive, San Diego, California 92121-1714.

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Full Name of Joint Inventor	Inventor Signature	Date
Vivek Mohan	Vivek Mohan	Nov 5th 08
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PTO/SB/06 (12-04)

Filing Date: 02/04/09

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/365,559

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**27** minus 20 =	**7**	x$26		OR	x$52	**364**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**4** minus 3 =	* **1**	x$110			x$220	**220**
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL			TOTAL	**1674**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.