UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01315
Patent 8,063,674

DECLARATION OF DR. MASSOUD PEDRAM

I, Massoud Pedram, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorporated ("Qualcomm" or "Patent Owner") in the matter of the *Inter Partes* Review of U.S. Patent No. 8,063,674 ("the '674 patent").

2. I am being compensated for my work in this matter at my standard hourly rate of $900 for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. In preparing this Declaration, I considered the following materials:

   a. The '674 patent (Ex. 1001) and its file history (Ex. 1002);

b. Petition for *Inter Partes* Review of U.S. Patent No. 8,063,674, IPR2018-01315 (Paper 2) ("the Petition");

c. Declaration of Dr. Robert W. Horst (Ex. 1003);

d. U.S. Patent No. 7,279,943 to Steinacker (Ex. 1005) ("Steinacker");

e. U.S. Patent No. 4,717,836 to Doyle (Ex. 1006) ("Doyle");

f. Jun Cheol Park and Vincent J. Mooney, Sleepy Stack Leakage Reduction, 14 IEEE Transactions On Very Large Scale Integration (VLSI) Systems 1251 (2006) (Ex. 1007) ("Park");

g. U.S. Patent Pub. No. 2002/0163364 to Majcherczak (Ex. 1008) ("Majcherczak");

h. U.S. Patent No. 6,646,844 to Matthews (Ex. 1009) ("Matthews");

i. Qualcomm's Patent Owner Preliminary Response (Paper 6) ("POPR");

j. Decision - Institution of *Inter Partes* Review (Paper 7) ("the Decision"); and

k. Any other materials referenced herein.

I. Professional Background

4. I am a Professor of Electrical Engineering and Charles Lee Powell Chair in Electrical Engineering and Computer Science in the Viterbi School of Engineering at the University of Southern California (USC). From 2013 until early 2017 I held the Stephen and Etta Varra Professorship in the Viterbi School of Engineering at USC.

5. I am an expert on electronic design automation (EDA), Very Large Scale Integration (VLSI) design including digital integrated circuits and semiconductor memory, energy efficient design, hybrid electrical energy storage systems (HEESS), and power/thermal modeling and management in integrated circuits and systems including multiple-supply-voltage designs and power collapsing techniques and voltage regulation. I also have expertise in building, validating, and delivering voltage regulation and conversion and management circuits and, more generally, nano-electronic circuits and system-on-chip designs targeting applications ranging from high performance computing to low-power embedded computing.

6. I earned by B.S. in Electrical Engineering from the California Institute of Technology in 1986. I earned my M.S. in Electrical Engineering and Computer Sciences from the University of California at Berkeley in 1989. During my Masters and Doctoral degree programs, I was a Graduate Student Researcher in the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley from 1986-1991. Concurrently I held a part-time Research Position, at the Xerox Palo Alto Research Center ("Xerox PARC") from 1987-1989. I then earned my Ph.D. in Electrical Engineering and Computer Sciences from the University of California at Berkeley in 1991.

7. After receiving my doctorate, I was an Assistant Professor in the Department of Electrical Engineering at USC from 1991-1996. I was then an Associate Professor in the Department of Electrical Engineering at USC from 1996-2000. After that I have been a Professor of Electrical Engineering and Computer Science in the Viterbi School of Engineering at the University of Southern California (USC).

8. I am a named inventor on ten U.S. patents and a U.S. patent application. These patents relate to topics ranging from novel address bus encoding techniques to charge recycling based multi-threshold CMOS design, and from low leakage SRAMs to dynamic backlight scaling for power minimization. The recently-filed patent application focuses on design and implementation of a superconductive Field Programmable Gate Array (FPGA) fabric.

9. I have (co-) published four books and more than 650 archival and conference papers and book chapters. My research ranges from computer-aided design techniques and tools targeting VLSI circuit and system design to FPGA fabric design and FPGA synthesis, from low power electronics and battery-powered embedded system design to power distribution, conversion and regulation. For this research, my students and I have received ten conference and journal Best Paper awards.

10. In addition to my work at Xerox PARC, I have been a member of multiple technical and scientific advisory boards for high-tech companies, including EPIC Design, Magma Design Automation, and Atrenta Inc., all of which went on to have successful initial public offerings (IPOs) or were acquired.

11. I have served as the (lead) principal investigator on many US government (including the National Science Foundation, the Defense Advanced Research Projects Agency, U.S. Department of Defense, and the Intelligence Advanced Research Projects Activity) and private industry (including the Semiconductor Research Corporation) research projects, for some of which I have been the lead investigator of a team comprised of tens of faculty, students, and industry collaborators.

12. I was a recipient of the 1996 Presidential Early Career Award for Scientists and Engineers, and in 2000 I was selected as a Fellow of the IEEE and in 2008 named as an ACM Distinguished Scientist.

13. I received the 2015 IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award for my contributions to modeling and design of lower power VLSI circuits and systems, and energy efficient computing.

14. I was recognized as the Third Most Cited Author at the 50th anniversary of the Design Automation Conference, Austin, TX, in June 2013. I received a Top Three Author Award at the 20th Anniversary Asia and South

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