John D. Villasenor

Education

1986 – 1989 **Stanford University**
Ph.D. in Electrical Engineering

1985 – 1986 **Stanford University**
M.S. in Electrical Engineering

1982 – 1985 **University of Virginia**
B.S. in Electrical Engineering

Appointments

Since 1992 **University of California, Los Angeles** **Los Angeles, CA**
Current Position: Professor of Electrical Engineering, Public Policy, and Management
Visiting Professor of Law
Conducting research on innovative communications, networking, security, signal and image processing, and computing technologies and their broader implications. Recent applications have included cybersecurity, robotics (including drones and driverless cars), digital financial services, and privacy. Teach classes in the UCLA schools of engineering (relating to information processing), public affairs (relating to technology policy), law (the "Digital Technologies and the Constitution" course), and management (the course on "Intellectual Property for Technology Entrepreneurs"). See http://johnvillasenor.com for more information, including publications.

Since 2011 **The Brookings Institution** **Washington, DC**
Nonresident Senior Fellow, Governance Studies Program
Examining a broad range of issues at the intersection of technology, policy, and law, generally related to the topics listed above. See https://www.brookings.edu/experts/john-villasenor/

Since 2014 **Stanford University** **Stanford, CA**
National Fellow (2014-2016), Visiting Fellow (since 2016), The Hoover Institution
Affiliate, Center for International Security and Cooperation (CISAC)
See http://cisac.fsi.stanford.edu/people/john_villasenor

1990 – 1992 **Jet Propulsion Laboratory** **Pasadena, CA**
Developed new techniques for imaging and mapping the earth from space.

Other Professional Activities

- Member, Council on Foreign Relations
- Have led a Department of Homeland Security-supported project aimed at improving cybersecurity in U.S. critical infrastructure. See http://cisac.fsi.stanford.edu/docs/cybersecurity-assurance-for-critical-infrastructure

- Appointed in 2012 (term ended mid-2014) by the World Economic Forum to the Global Agenda Council on the Intellectual Property System. From 2013 to 2014, vice chair of the council.
- Mid-2014 to mid-2016: Member of the World Economic Forum's Global Agenda Council on Cybersecurity
- Have contributed to international standards organizations and industry consortia for the development of new communications standards.
- Have provided expert testimony in multiple intellectual property matters in Federal District Court, at the U.S. International Trade Commission in Washington, and before the U.S. Patent and Trademark Office.
- Have provided congressional testimony before the House Judiciary Committee in 2013 and 2014, before the Senate Commerce Committee in 2015 and 2017, and before the House Energy and Commerce Committee in 2015. See http://johnvillasenor.com/publications/congressional-testimony/
- Served as Vice Chair of the International Center for Missing and Exploited Children's Digital Economy Task Force
- Developed and implemented an online intellectual property training program covering patents, copyright, trademarks, and trade secrets. The program was adopted and implemented by the University of California. See https://techtransfer.universityofcalifornia.edu/IPAwareness/story.html
- Active in early stage technology venture capital since the 1990s
- Participant in the Uniform Law Commission's study committees on 1) state regulation of driverless cars and 2) vehicle event data recorders

Patents

- Approximately 20 issued U.S. patents in areas including communications, information processing, and cybersecurity.

Publications

- Nearly 200 academic papers published in venues including engineering journals, conference proceedings, and law reviews (see below; see also http://johnvillasenor.com). "H-index" of 49 (as of mid-2017). Articles and commentary also published in broader interest venues including the *Atlantic*, *Billboard*, the *Chronicle of Higher Education*, *Fast Company*, *Forbes*, the *Huffington Post*, the *Los Angeles Times*, the *New York Times*, *Scientific American*, *Slate*, and the *Washington Post*.

Technical Papers Published In Academic Journals; Book Chapters

1. Jason Jaskolka and John Villasenor, "An approach for identifying and analyzing implicit interactions in distributed systems," IEEE Transactions on Reliability, Vol. 66, No. 2, pp. 529-546, June 2017.

2. Lok-Won Kim and John Villasenor, "Dynamic function verification for system-on-chip security against hardware-based attacks," IEEE Transactions on Reliability, Vol. 64, No. 4, pp. 1229-1242, November 2015.

3. Jerry Lien, Laura Hughes, Jorge Kina, and John Villasenor, "Mobile money solutions for a smartphone-dominated world," Journal of Payments Strategy & Systems, Vol. 9, No. 3, pp. 341-350, Fall, 2015. Available at SSRN: http://ssrn.com/abstract=2632372

4. Lok-Won Kim and John Villasenor, "Automated iterative pipelining for ASIC design," ACM Transactions on Design Automation of Electronic Systems, Vol. 20, No. 2, February 2015.

5. Lok-Won Kim and John Villasenor, "Dynamic function replacement for system-on-chip security in the presence of hardware-based attacks," IEEE Transactions on Reliability, Vol. 63, No. 2, pp. 661-675, June 2014.

6. Przemyslaw Pawelczak, Shaunak Joshi, Sateesh Addepalli, John Villasenor, Danijela Cabric, "Impact of the connection admission process on the direct retry load balancing algorithm in cellular networks," IEEE Transactions on Mobile Computing, Vol. 12, No. 9, pp. 1681-1696, September 2013.

7. Jianwen Chen, Jason Cong, Luminita A. Vese, John Villasenor, Ming Yan, and Yi Zou, "A hybrid architecture for compressive sensing 3D CT reconstruction," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Special Issue: Circuits, Systems and Algorithms for Compressive Sensing, Vol. 2, No. 3, pp. 616-625, Oct. 2012.

8. Jianwen Chen, Jianhua Zheng, Feng Xu, and John Villasenor, "Adaptive frequency weighting for high-performance video coding," IEEE Transactions on Circuits and Systems for Video Technology, Vol. 22, No. 7, pp. 1027-1036, July 2012.

9. W. Hu, J. Wen, W. Wu, Y. Han, S. Yang, and J. Villasenor, "Highly scalable parallel arithmetic coding on muti-core processors using LDPC codes," IEEE Transactions on Communications, Vol. 60, No. 2, pp. 289-194, February 2012.

10. J. Chen, F. Xu, Y. He, J. Villasenor, Y. Han, Y. Xu, Y. Rong, C. Reader, and J. Wen, "Efficient video coding using legacy algorithmic approaches," IEEE Transactions on Multimedia, Vol. 14, No. 1, pp. 111-120, February, 2012.

11. D. Lee, L. Kim, and J. Villasenor, "Precision-aware, self-quantizing hardware architectures for the discrete wavelet transform," IEEE Transactions on Image Processing, Vol. 21, No. 2, pages 768-777, February 2012.

12. L.W. Kim and J.D. Villasenor, "A system-on-chip bus architecture for thwarting integrated circuit Trojan horses," IEEE Transactions on VLSI Systems, vol. 19, no. 10, pp. 1921-1926, October 2011.

13. Y. Han, J. Wen, D. Cabric and J. Villasenor, "Using a vector of observations to identify the number of frequency-hopping transmitters," IEEE Communications Letters, vol. 15, no. 3, pp. 299-301, March 2011.

14. D. Lee, H, Kim, M. Rahimi, D. Estrin, and J.D. Villasenor, "Energy-efficient image compression for resource-constrained platforms," IEEE Transactions on Image Processing, vol. 18. no. 9, pp. 2100-2113, September 2009.

15. D. Lee, R.C.C. Cheung, W. Luk, and J.D. Villasenor, "Hierarchical segmentation for hardware function evaluation," IEEE Transactions on VLSI Systems, vol. 17, No. 1, pp. 103-116, January 2009.

16. D. Lee and J.D. Villasenor, “Optimized custom precision function evaluation for embedded processors,” IEEE Transactions on Computers, vol. 58, no. 1, pp. 46-59, January 2009.

17. H. Kim, M. Rahimi, D. Lee, D. Estrin, and J.D. Villasenor, “Energy-aware high resolution image acquisition via heterogeneous image sensors,” IEEE Journal of Selected Topics in Signal Processing, vol. 2, no. 4, pp. 526-537, August 2008.

18. H. Kim, D. Lee, and J.D. Villasenor, “Design tradeoffs and hardware architecture for real-time iterative MIMO detection using sphere decoding and LDPC coding,” IEEE Journal on Selected Areas in Communications, vol. 26, no. 6, pp. 1003-1014, August 2008.

19. D. Choi, K. Choi, and J.D. Villasenor, “New non-volatile memory structures for FPGA architectures,” IEEE Transactions on VLSI Systems, vol. 16, no. 7, pp. 874-881, July 2008.

20. H. Kim and J.D. Villasenor, “Secure MIMO communications in a system with equal numbers of transmit and receive antennas,” IEEE Communications Letters, vol. 12, no. 5, pp. 386-388, May 2008.

21. D. Lee, H. Kim, C. Jones, and J.D. Villasenor, “Pilotless frame synchronization for LDPC-coded transmission systems,” IEEE Transactions on Signal Processing, vol. 56, No. 7, pp. 2865 - 2874, July 2008.

22. D. Lee, R.C.C. Cheung, J.D. Villasenor, and W. Luk, “Hardware implementation tradeoffs of polynomial approximations and interpolations,” IEEE Transactions on Computers, vol. 57, no. 5, pp. 686-701, May 2008.

23. D.B. Thomas, W. Luk, P.H.W. Leong, and J.D. Villasenor, “Gaussian random number generators,” ACM Computing Surveys, vol. 39, issue 4, article 11, October 2007.

24. D. Lee, H. Kim, C.R. Jones, and J.D. Villasenor, “Pilotless frame synchronization via LDPC code constraint feedback,” IEEE Communications Letters, vol. 11, no. 8, pp. 683-685, August 2007.

25. R.C.C. Cheung, D. Lee, W. Luk, and J.D. Villasenor, “Hardware generation of arbitrary random number distributions from uniform distributions via the inversion method,” IEEE Transactions on VLSI Systems, vol. 15, no. 8, pp. 952-962, August 2007.

26. H. Kim, J. Wen, and J.D. Villasenor, “Secure arithmetic coding,” IEEE Transactions on Signal Processing, vol. 55, no. 5, pp. 2263 - 2272, May 2007.

27. D. Lee, R.C.C. Cheung, and J.D. Villasenor, “A flexible architecture for precise gamma correction,” IEEE Transactions on VLSI Systems, vol. 15, no. 4, pp. 474-479, April 2007.

28. D. Lee and J.D. Villasenor, “A bit-width optimization methodology for polynomial-based function evaluation,” IEEE Transactions on Computers, vol. 56, no. 4, pp. 567-571, April 2007.

29. C. Jones, T. Tian, J.D. Villasenor, and R. Wesel, “The universal operation of LDPC codes over scalar fading channels,” IEEE Transactions on Communications, vol. 55, no. 1, pp.122-132, January 2007.

30. M.D. Smith and J. Villasenor, “JPEG-2000 rate control for digital cinema,” SMPTE Motion Imaging Journal, vol. 115, no. 10, pp. 394-399, October 2006.

31. D. Lee, J.D. Villasenor, W. Luk and P.H.W. Leong, “A hardware Gaussian noise generator using the Box-Muller method and its error analysis,” IEEE Transactions on Computers, vol. 55, no. 6, pp. 659-671, June 2006.

32. D. Lee, E.L. Valles, J.D. Villasenor and C.R. Jones, “Joint LDPC decoding and timing recovery using code constraint feedback,” IEEE Communications Letters, vol. 10, no. 3, pp. 189-191, March 2006.

33. J. Wen, H. Kim and J.D. Villasenor, “Binary arithmetic coding with key-based interval splitting,” IEEE Signal Processing Letters, vol. 13, No. 2, pp. 69-72, February 2006.

34. D. Lee, W. Luk, J.D. Villasenor, G. Zhang and P.H.W. Leong, “A hardware Gaussian noise generator using the Wallace method,” IEEE Transactions on VLSI Systems, vol. 13, no. 8, pp. 911-920, August 2005.

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36. D. Lee, W. Luk, J.D. Villasenor and P.Y.K Cheung, “A Gaussian noise generator for hardware-based simulations,” IEEE Transactions on Computers, vol. 53, no. 12, pp. 1523-1534, December 2004.

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38. T. Tian, C. Jones, J.D. Villasenor, and R. Wesel, ”Selective avoidance of cycles in irregular LDPC code construction,” IEEE Transactions on Communications, vol. 52, no. 8, pp. 1242-1247, August 2004.

39. K. Lakovic, J. Villasenor, “An algorithm for construction of efficient fix-free codes,” IEEE Communication Letters, vol. 7, no. 8, pp. 391-393, August 2003.

40. J. Garcia-Frias, J.D. Villasenor, “Combined turbo detection and decoding for unknown ISI channels", IEEE Transactions on Communications, vol. 51, no. 1, pp. 79-85, January 2003.

41. K. Lakovic, J. Villasenor, “On the design of error-correcting reversible variable length codes,” IEEE Communication Letters, vol. 6, no. 8, pp. 337-339, August 2002.

42. Jiangtao Wen and J.D. Villasenor, “Soft-input soft-output decoding of variable length codes,” IEEE Transactions on Communications, vol. 50, No. 5, pp. 689-692, May 2002.

43. J. Garcia-Frias and J.D. Villasenor, “Turbo decoding of Gilbert-Elliot channels,” IEEE Transactions on Communications, vol. 50, no.3, pp. 357-363, March 2002.

44. J. Garcia-Frias and J.D. Villasenor, “Joint turbo decoding and estimation of hidden Markov sources,” IEEE Journal on Selected Areas in Communications, vol. 19, no. 9, pp. 1671-1679, September 2001.

45. S. Saha, M. Jamtgaard and J.D. Villasenor, “Bringing the wireless internet to mobile devices,” Computer, vol. 34, no.6, pp.54-58, June 2001.

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