AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

PATENT APPLICATION

ATTORNEY DOCKET NO. 70030259-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal L tter

COMMISSIONER FOR PATENTS
PO Box 1450
Al xandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Kong Weng Lee et al.**

TITLE: **PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 8 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( )(Other) _____(fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X $18	$ 0
INDEPENDENT CLAIMS	2 — 3	0	X $84	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$280	$ 0
BASIC FEE: Design ($330.00); Utility ($750.00)				$ 750
TOTAL FILING FEE				$ 750
OTHER FEES				$
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By Linda A. Iimura

Typed Name: **Linda A. Iimura**

Respectfully submitted,

Kong Weng Lee et al.

By

Ian Hardcastle

Attorney/Agent for Applicant(s)
Reg. No. 34,075
Date: June 27, 2003
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR PATENT

Packaging Device for Semiconductor Die, Semiconductor Device Incorporating Same and Method of Making Same

Inventors: Kong Weng Lee
Kee Yean Ng
Yew Cheong Kuan
Cheng Why Tan
Gin Ghee Tan

Related Application

[0001] This application is related to a simultaneously-filed United States patent application serial number 10/xxx,xxx entitled *Method for Fabricating a Packaging Device for Semiconductor Die and Semiconductor Device Incorporating Same* of inventors Kong Weng Lee, Kee Yean Ng, Yew Cheong Kuan, Cheng Why Tan and Gin Ghee Tan, attorney docket number 70030260-1.

Background of the Invention

[0002] Many types of conventional semiconductor device are composed of a semiconductor die mounted in a packaging device. One type of packaging device widely used in the industry includes a metal lead frame. A metallization layer of aluminum located on the bottom surface of the semiconductor die is bonded to a conductive surface that forms part of the lead frame to attach and electrically connect the die to the lead frame. Additionally, electrical connections are made between bonding pads on the top surface of the die and other leads of the lead frame to provide additional electrical connections to the die. The lead frame and semiconductor die are then encapsulated to complete the semiconductor device. The packaging device protects the semiconductor die and provides electrical and mechanical connections to the die that are compatible with conventional printed circuit board assembly

processes.

[0003] In such conventional semiconductor devices, the bottom surface of the die is typically bonded to the conductive surface of the lead frame using a silver epoxy adhesive that cures at a relatively low temperature, typically about 120 °C. The curing temperature of the silver epoxy adhesive is compatible with the other materials of the packaging device.

[0004] The volume of the packaging device used in such conventional semiconductor devices, i.e., the lead frame and the encapsulant, is typically many times that the semiconductor die. This makes such conventional semiconductor devices unsuitable for use in applications in which a high packing density is required. A high packing density allows miniaturization and other benefits. Therefore, what is needed is a semiconductor packaging device that is comparable in volume with the semiconductor die and that is compatible with conventional printed circuit board assembly processes.

[0005] Recently, semiconductor die having a substrate surface metallization layer of a gold-tin alloy (80 % Au:20 % Sn approximately) have been introduced in light-emitting devices. Such semiconductor die typically have a substrate of sapphire, silicon carbide or a Group III-V semiconductor material, such as gallium arsenide. Semiconductor devices having substrates of the first two substrate materials have layers of Group III-V semiconductor materials, such as gallium nitride, deposited on their substrates. The die attach process for such semiconductor die uses a gold-tin eutectic, which has a melting point of about 280 °C. Temperatures as high as about 350 °C can be encountered in the die attach process for such die. Such high temperatures are incompatible with the materials of many conventional packaging devices. Thus, what is also needed is a packaging device for semiconductor die that use a high-temperature die attach process.

[0006] Many printed circuit assembly processes and assembly equipment require the use of standard semiconductor device packages. Modifying such processes to use a new semiconductor device package can be expensive and can interrupt production. Therefore, what is additionally needed is a way to mount a semiconductor die that requires a high-temperature die attach process in a conventional packaging device.

Summary of the Invention

[0007] The invention provides a packaging device for a semiconductor die. The packaging device includes a substrate, a mounting pad, a connecting pad and an interconnecting element. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad.

[0008] The packaging device has a volume that is only a few times that of the semiconductor die and can be fabricated from materials that can withstand a high-temperature die attach process. The packaging device can be configured as the only packaging device of the semiconductor device. The packaging device can alternatively be configured as a submount for a semiconductor die that requires a high-temperature die attach process. The submount with attached semiconductor die can be handled as a conventional, albeit slightly larger, semiconductor die that is then mounted in a conventional packaging device, such as a lead-frame based packaging device, using a conventional semiconductor device assembly process, including conventional temperatures.

[0009] The invention also provides a semiconductor device that includes a substrate, a mounting pad, a connecting pad, an interconnecting element and a semiconductor die. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad. The semiconductor die is affixed to the mounting pad.

[0010] The semiconductor device as just described can be mounted in a conventional packaging device as described above. Alternatively, the semiconductor device may additionally include a bonding pad, an additional connecting pad, an additional interconnecting element and a bonding wire. The bonding pad is conductive and is located on the one of the major surfaces. The additional connecting pad is conductive and is located on the other of the major surfaces. The additional interconnecting

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