UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD
APPLE, INC., Petitioner
v.
QUALCOMM INCORPORATED., Patent Owner
Case IPR2018-01249 Patent 7,693,002

PETITIONER APPLE, INC.'S REPLY TO PATENT OWNER'S RESPONSE

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UPDATED EXHIBIT LIST

APPLE-1001	U.S. Patent No. 7,693,002 to Jentsung Lin ("the '002 patent")
APPLE-1002	Prosecution History of the '002 patent ("the Prosecution History")
APPLE-1003	Declaration of Dr. Robert Horst, Ph.D
APPLE-1004	Curriculum Vitae of Dr. Horst
APPLE-1005	U.S. Patent No. 4,951,259 to Yoichi Sato ("Sato")
APPLE-1006	U.S. Patent Pub. No. 2006/0098520 to Toru Asano et al. ("Asano")
APPLE-1007	Kiyoo Itoh, VLSI Memory Chip Design, (Springer 2001) ("Itoh")
APPLE-1008	U.S. Patent No. 5,291,076 to Jeffrey T. Bridges ("Bridges")
APPLE-1009	Stephen Brown et al., Fundamentals of Digital Logic with Verilog Design, (McGraw Hill 2003) ("Brown")
APPLE-1010	Declaration of Edward G. Faeth (Authentication of APPLE-1007 and APPLE-1009)
APPLE-1011	U.S. Patent No. 6,483,771 to Tae-jeen Shin ("Shin")
APPLE-1012	U.S. Patent No. 5,602,796 to Kenichiro Sugio ("Sugio")
APPLE-1013	Second Declaration of Dr. Robert Horst, Ph.D
APPLE-1014	IEEE Dictionary (with additional page)
APPLE-1015	Modern Dictionary of Electronics
APPLE-1016	U.S. Patent No. 4,922,461 ("Hayakawa")



APPLE-1017 M. Pedram. "Design technologies for Low Power VLSI," in *Encyclopedia of Computer Science and Technology*, Marcel Dekker, Editors: A Kent, J. G. Williams, and C. M. Hall, vol. 36, 1997, pages 73-95

N. Mohyuddin, K. Patel, and M. Pedram. "Deterministic clock gating to eliminate wasteful activity in out-of-order superscalar processors due to wrong-path instructions," *Proc. of Int'l Conf.*

on Computer Design, Oct. 2009, pages 166-172

APPLE-1019 Pedram Deposition Transcript

APPLE-1018



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