

[54] **STATIC RANDOM ACCESS MEMORY WITH ADDRESS TRANSITION DETECTOR**

4,701,889 10/1987 Ando ..... 365/233.5

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[57] **ABSTRACT**

[21] **Appl. No.:** 329,717

When an address transition detector detects a transition of an address signal, it produces an address transition detect signal. The signal drives a bit line initializing circuit which in turn initializes paired bit lines, and initializes the paired output lines of a sense amplifier. At the same time, a clock signal generator generates a clock signal for a predetermined period of time in accordance with the address transition detect signal. The clock signal is supplied to the sense amplifier and a data output circuit. The sense amplifier is active during a period that the clock signal from the clock signal generator is in an effective level. The output terminal of the data output circuit is placed in a high impedance state during the period that the clock signal is in an effective level. During the other periods than the effective level period, the data output circuit produces a signal corresponding to the data as is read out of a memory cell and outputted by the sense amplifier.

[22] **Filed:** Mar. 28, 1989

[30] **Foreign Application Priority Data**

Mar. 30, 1988 [JP] Japan ..... 63-74518  
Mar. 30, 1988 [JP] Japan ..... 63-74519

[51] **Int. Cl.<sup>5</sup>** ..... G11C 13/00

[52] **U.S. Cl.** ..... 365/230.08; 365/207; 365/189.08; 365/233.5

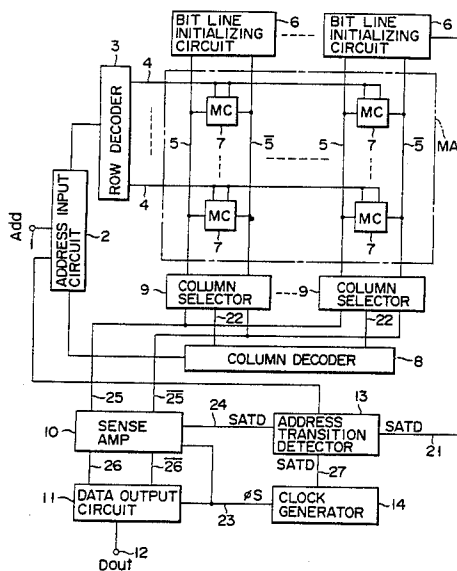
[58] **Field of Search** ..... 365/207, 208, 189.08, 365/233, 233.5, 203, 190, 189.05, 230.08

[56] **References Cited**

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**12 Claims, 5 Drawing Sheets**



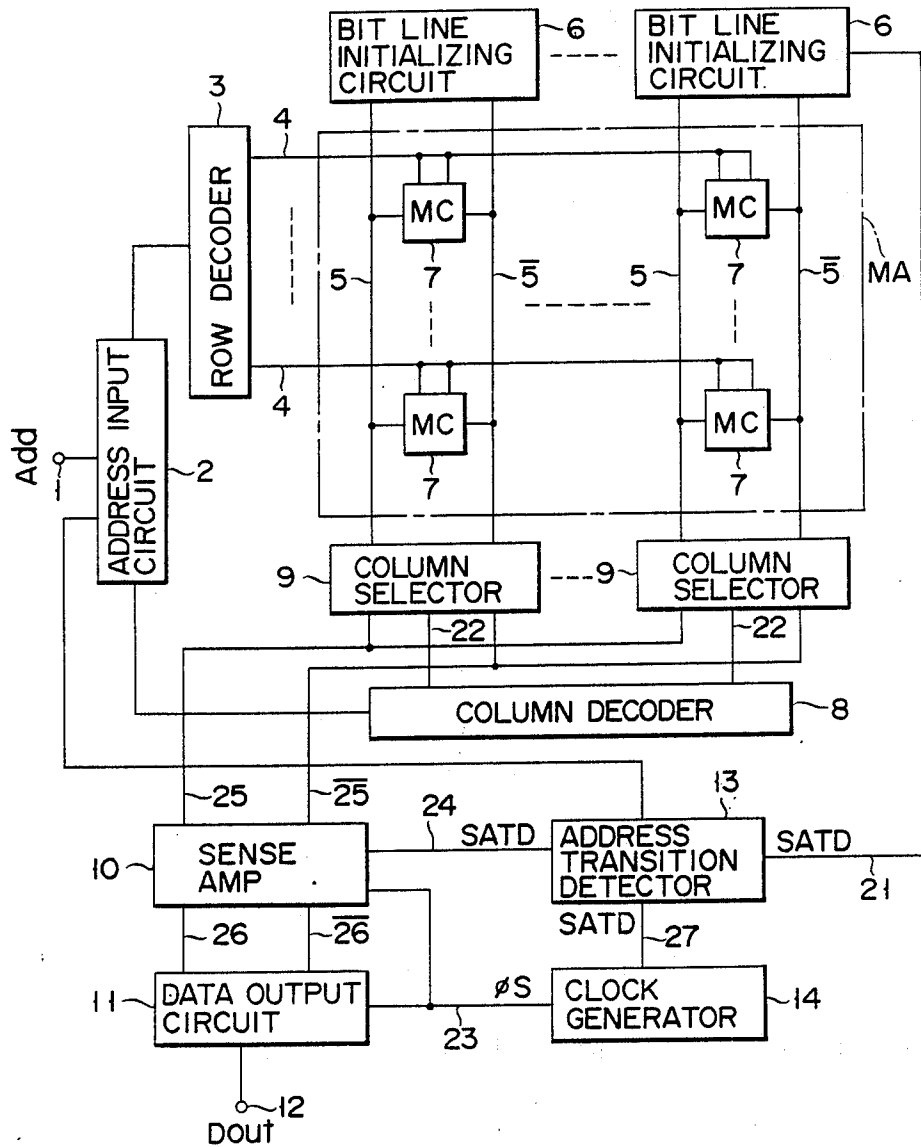
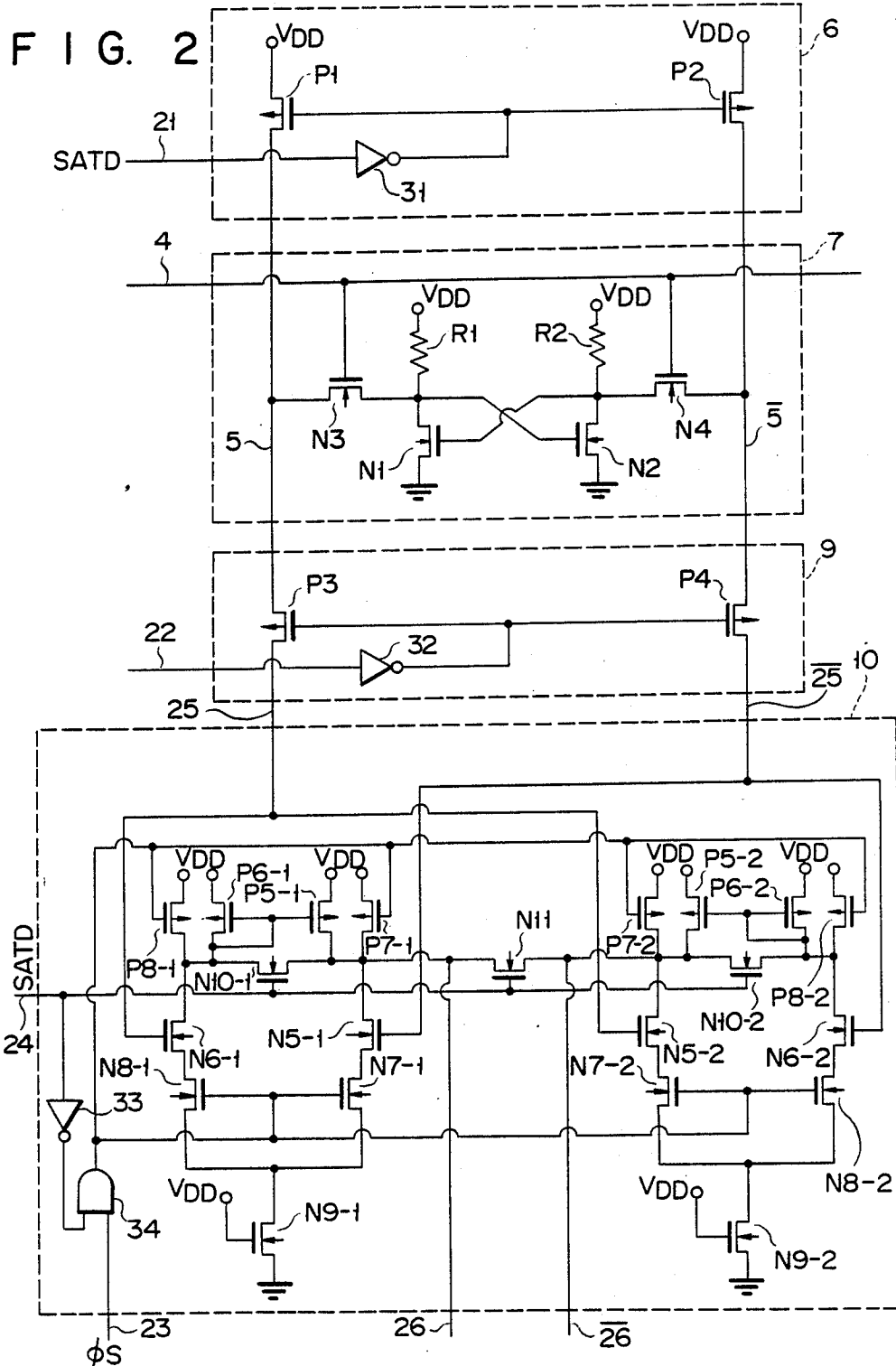


FIG. 1



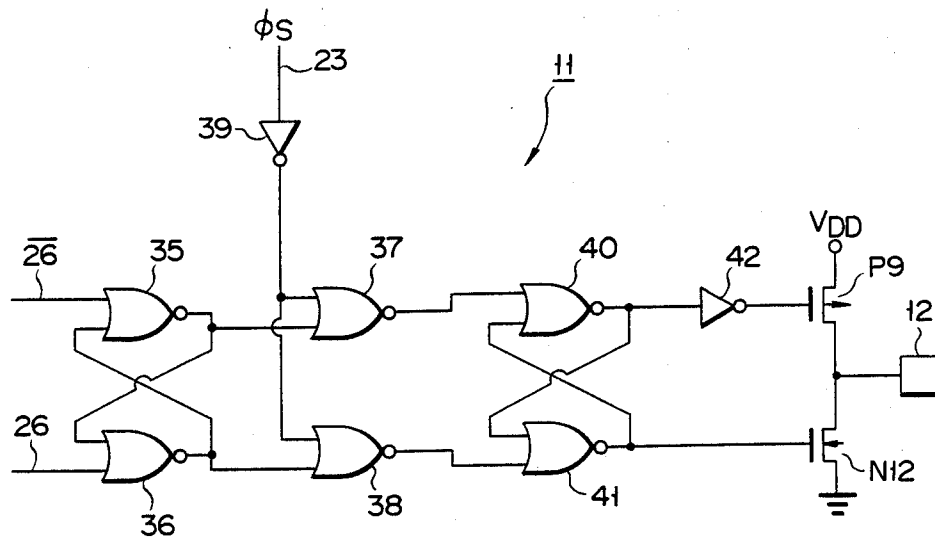


FIG. 3

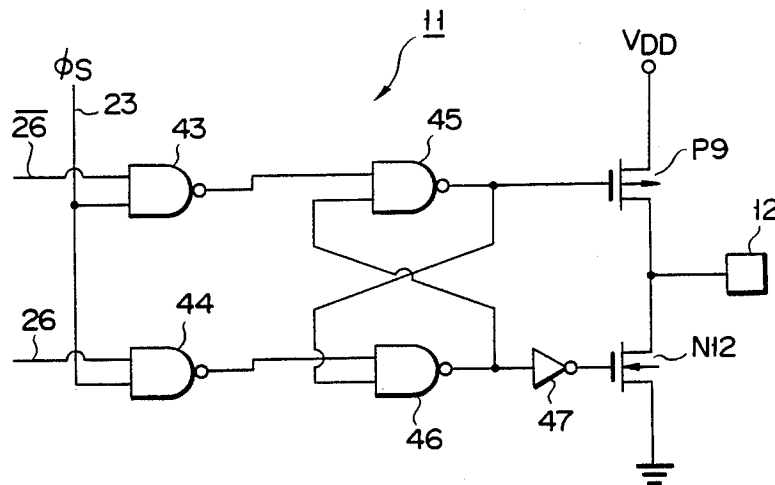


FIG. 4

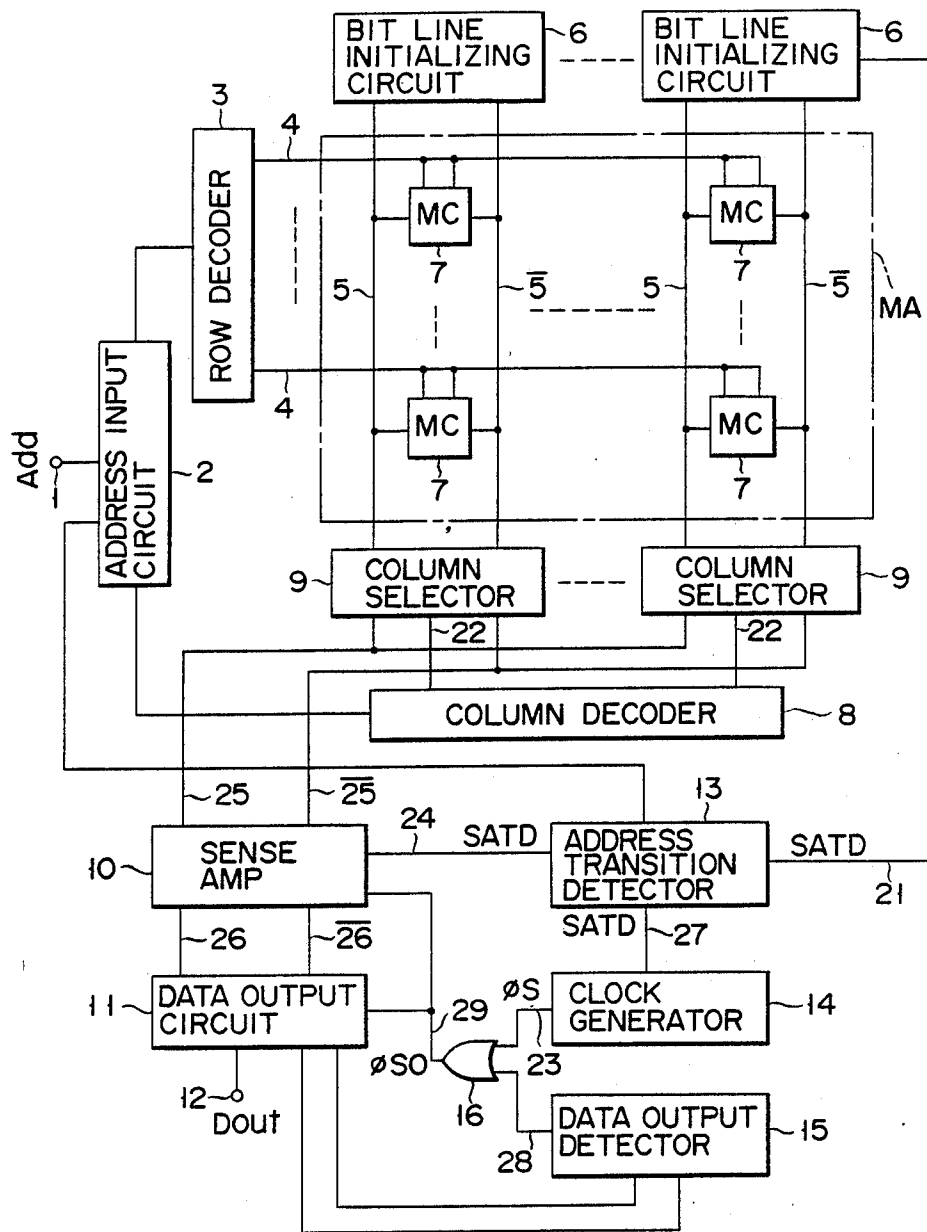


FIG. 5

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