IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Jentsung Lin	
U.S. Patent No.:	7,693,002	Attorney Docket No.:
Issue Date:	April 6, 2010	
Appl. Serial No.:	11/548,132	
Filing Date:	October 10, 2006	
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS	

DECLARATION OF Robert W. Horst, Ph.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

I. Introduction.

1. I summarized my relevant knowledge and experience in my first Declaration (APPLE-1003). In writing this Second Declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of memory systems and circuit design and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite herein and in my first declaration:Patent Owner's Response to the IPR Petition

- Dr. Massoud Pedram's Declaration (Ex. 2001)
- The IEEE Dictionary (Ex. 2002 and APPLE-1014)
- Itoh (additional portions) (Ex. 2003)
- Horst Deposition Transcript (Ex. 2005)
- The Modern Dictionary of Electronics (APPLE-1015)

- U.S. Patent No. 4,922,461 ("Hayakawa") (APPLE-1016)
- M. Pedram. "Design technologies for Low Power VLSI," in *Encyclopedia of Computer Science and Technology*, Marcel Dekker, Editors: A Kent, J. G. Williams, and C. M. Hall, vol. 36, 1997, pages 73-95 (APPLE-1017)
- N. Mohyuddin, K. Patel, and M. Pedram. "Deterministic clock gating to eliminate wasteful activity in out-of-order superscalar processors due to wrong-path instructions," *Proc. of Int'l Conf. on Computer De-sign*, Oct. 2009, pages 166-172 (APPLE-1018)
- Pedram Deposition Transcript (APPLE-1019).

II. A POSITA would not have limited the interpretation of "clock signal" to include only periodic clock signals

A. A broad plain and ordinary meaning for "clock signal" should be used

3. A POSITA would not have considered a periodic clock signal to be the broadest reasonable interpretation (BRI) of "clock signal" as used in the claims of the '002 patent. There is no indication in the '002 patent itself that would have led a POSITA to adopt such a restrictive interpretation because there is no explicit definition, waveform, or circuit in the '002 Patent defining or suggesting such a narrow definition.

4. Instead of using the BRI for "clock signal," Dr. Pedram adopts a restrictive definition inconsistent with the way "clock signal" is used in many systems, patents and textbooks. He defines "clock signal" as follows:

> The term "clock signal," as recited in each of the independent claims of the '002 patent, should be interpreted to mean "a **periodic signal** used for synchronization." This interpretation is consistent with the plain and ordinary meaning of the term as understood by the POSA.

Pedram Decl. at ¶53, emphasis added.

> it is my opinion that a POSA looking at this patent would understand the clock to be a **periodic signal** of fixed frequency used for synchronization purposes in the context of this memory system

Pedram Depo., p. 78, emphasis added.

5. Dr. Pedram's definition appears to be based on his assumption that the '002 Patent is directed only to synchronous memory systems. I disagree because I find no such restriction in the specification or drawings of the '002 Patent. Dr. Pedram's opinion is based on an absence in the depicted embodiments of the '002 patent of any timing circuitry he states would be required in an asynchronous system. However, Dr. Pedram acknowledged during his deposition that the figures in the '002 patent omit many necessary components of any memory system, such as column decoders (44:17-48:1), synchronous memory control logic (54:8-60:7), and clock drivers (40:10-20). Dr. Pedram's exemplary synchronous memory

system, as depicted in Itoh, shows many circuit components that are not depicted in the figures of the '002 patent. The figures in the '002 patent depict only a specific portion of a memory system (e.g., a row address decoder), and the absence of any one circuit component from the figures does not indicate to a POSITA that the circuit component must be absent from the entire memory system. As seen below by the side-by-side comparison of '002 patent's Fig. 1 with Itoh's Fig. 6.15, the '002 patent does not show any control logic or other circuitry associated with either synchronous or asynchronous memory systems, but only that necessary to explain the operation of its row address decoder.

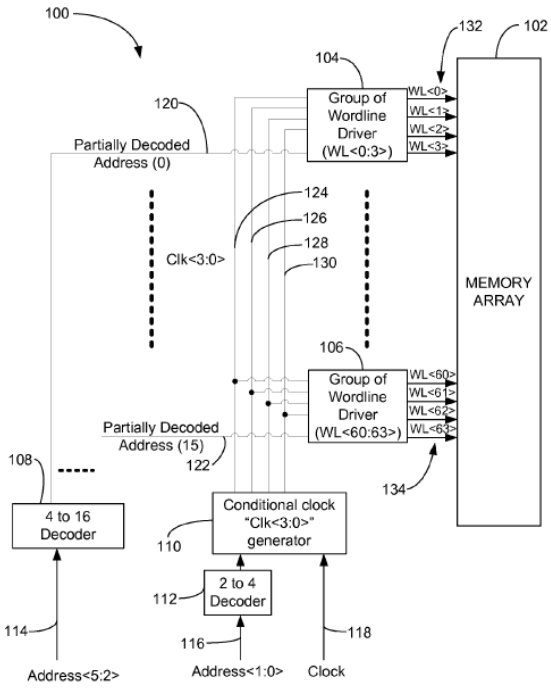

FIG. 1

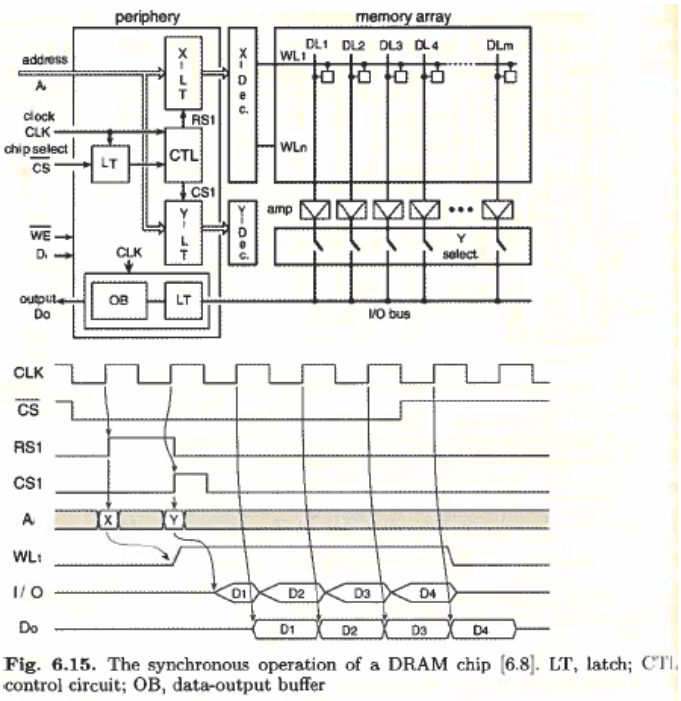

Fig. 6.15. The synchronous operation of a DRAM chip [6.8]. LT, latch; CTL, control circuit; OB, data-output buffer

6. In the embodiment in Fig. 1 of the '002 patent, the clock input could be supplied with any type of clock signal—e.g., a periodic clock signal, a non-

periodic gated clock signal, a non-periodic clock signal derived from a periodic clock (e.g., RS1 as shown in Itoh's synchronous clock system), or another type of non-periodic clock signal—without adversely affecting its row decoding functionality. Similarly, the clock signal supplied to the Sato and Asano prior art combinations could be periodic or non-periodic while implementing the same row decoding functionality as the '002 Patent.

7. Dr. Pedram states that his definition is the broadest reasonable interpretation based on the definition of "clock signal" from an IEEE dictionary. Ex. 2002 and APPLE-1014. The portion of the IEEE dictionary cited in Dr. Pedram's declaration defines "clock signal" as "[a] periodic signal used for synchronizing events," but this partial quotation omits the part of the definition that says "*Synonyms*: clock pulse; timing pulse." Many systems and devices have clock pulses and other timing signals that are not periodic.

8. Also, Dr. Pedram's declaration omits alternate definitions for "clock" in the same IEEE dictionary. One of the alternate definitions of "clock" is as follows:

> (2) A signal, the transitions of which (between the low and high logic level [or vice versa]) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation.

APPLE-1014 at 4.

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