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(54) **APPARATUS AND METHOD OF WORD LINE DECODING FOR DEEP PIPELINED MEMORY**

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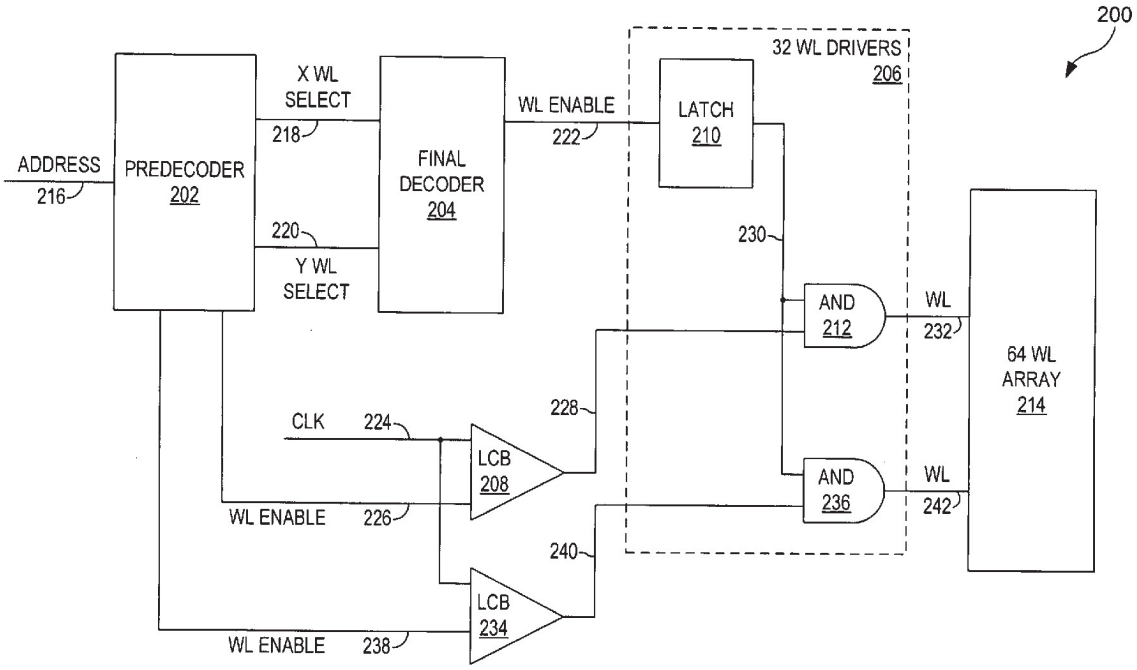
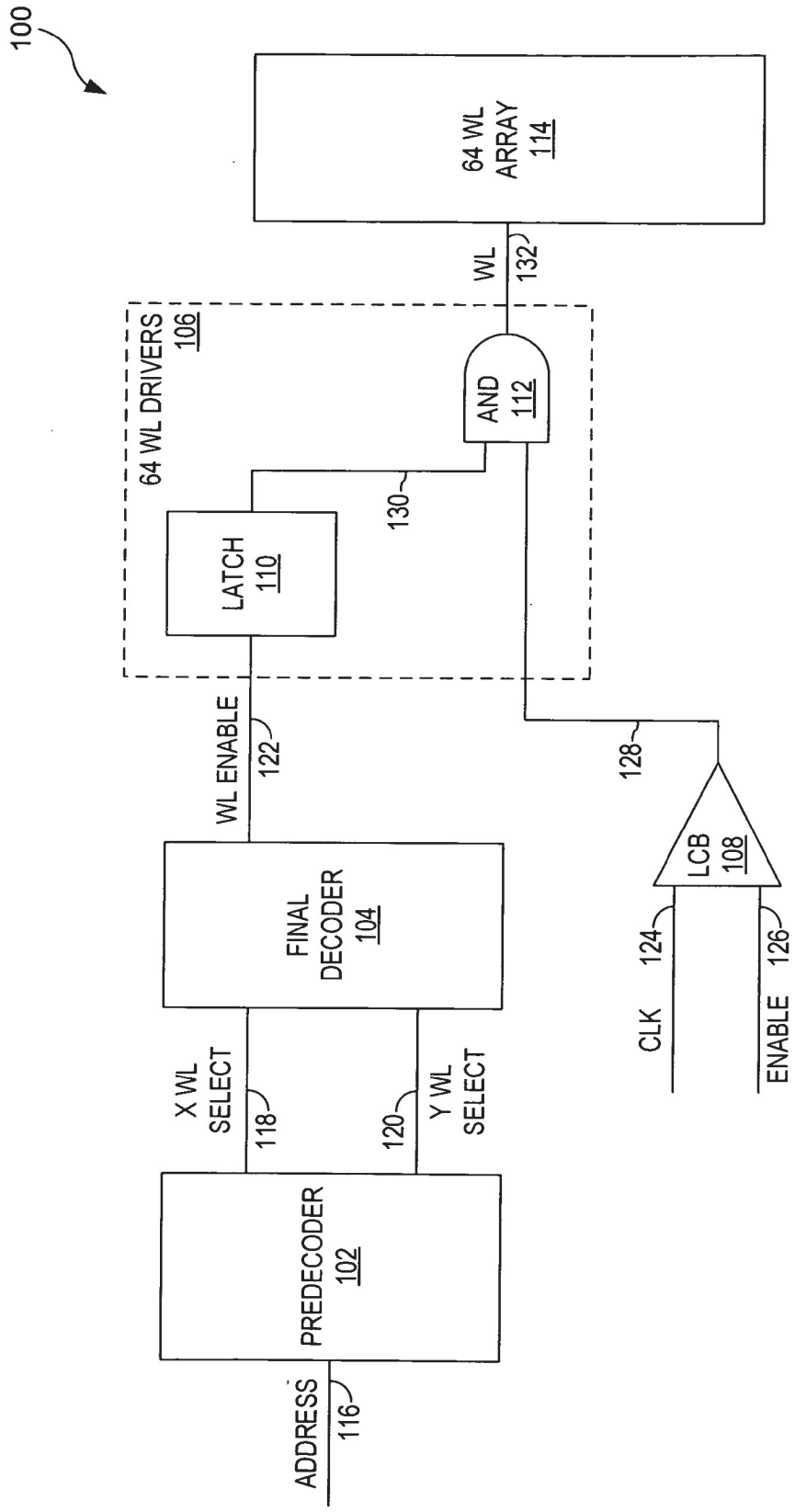
(57) **ABSTRACT**

A method, an apparatus, and a computer program are provided to reduce the number of required latches in a deep pipeline wordline (WL) decoder. Traditionally, a signal local clock buffer (LCB) has been responsible for providing a driving signal to a WL driver. However, with this configuration, a large number of latches are utilized. To reduce this latch usage, a number of LCBs are employed, such that one latch can enable an increased number of WLs. Hence, the overall area occupied by latches is reduced and power consumption is reduced.





PRIOR ART

FIG. 1

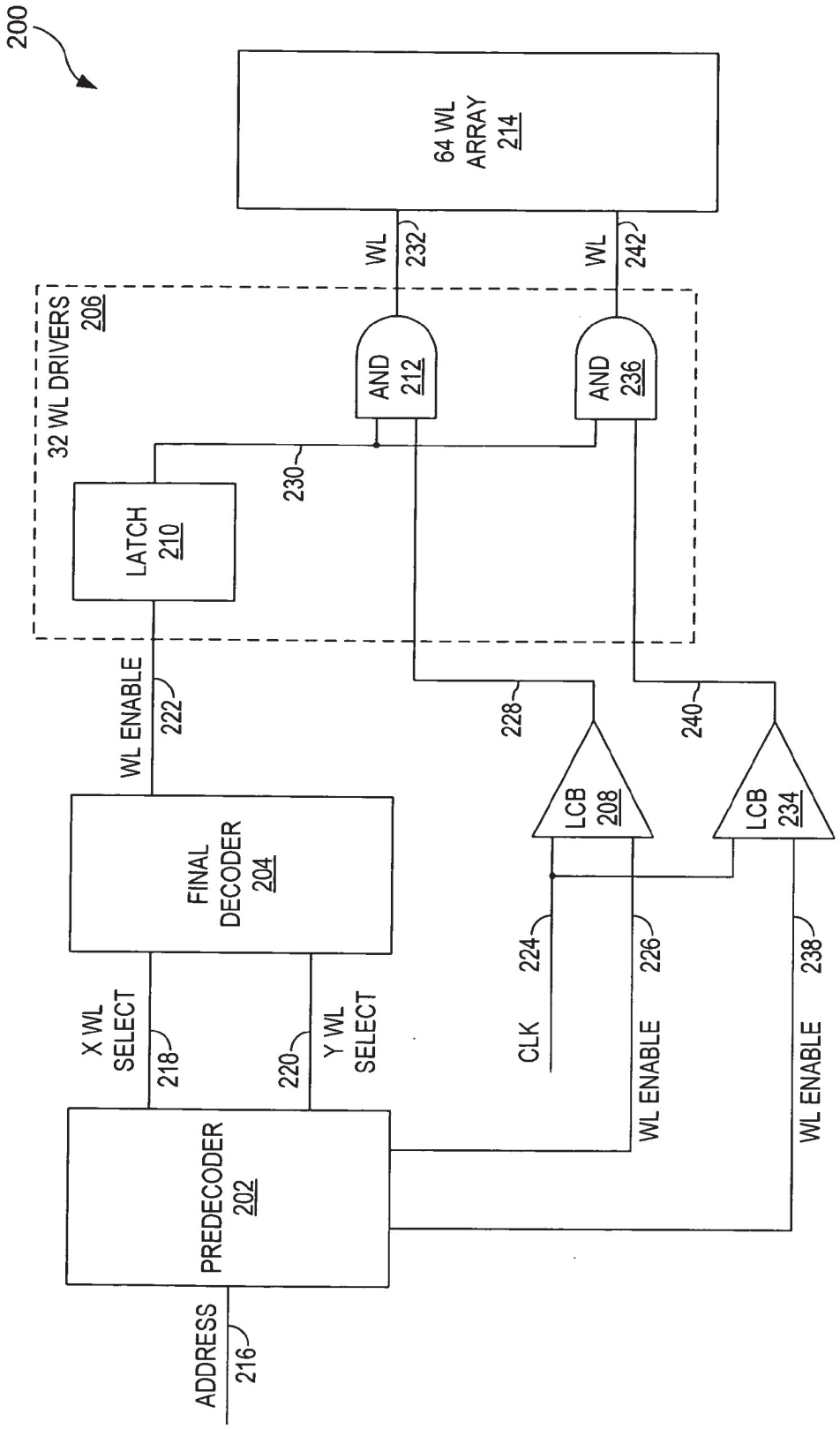


FIG. 2

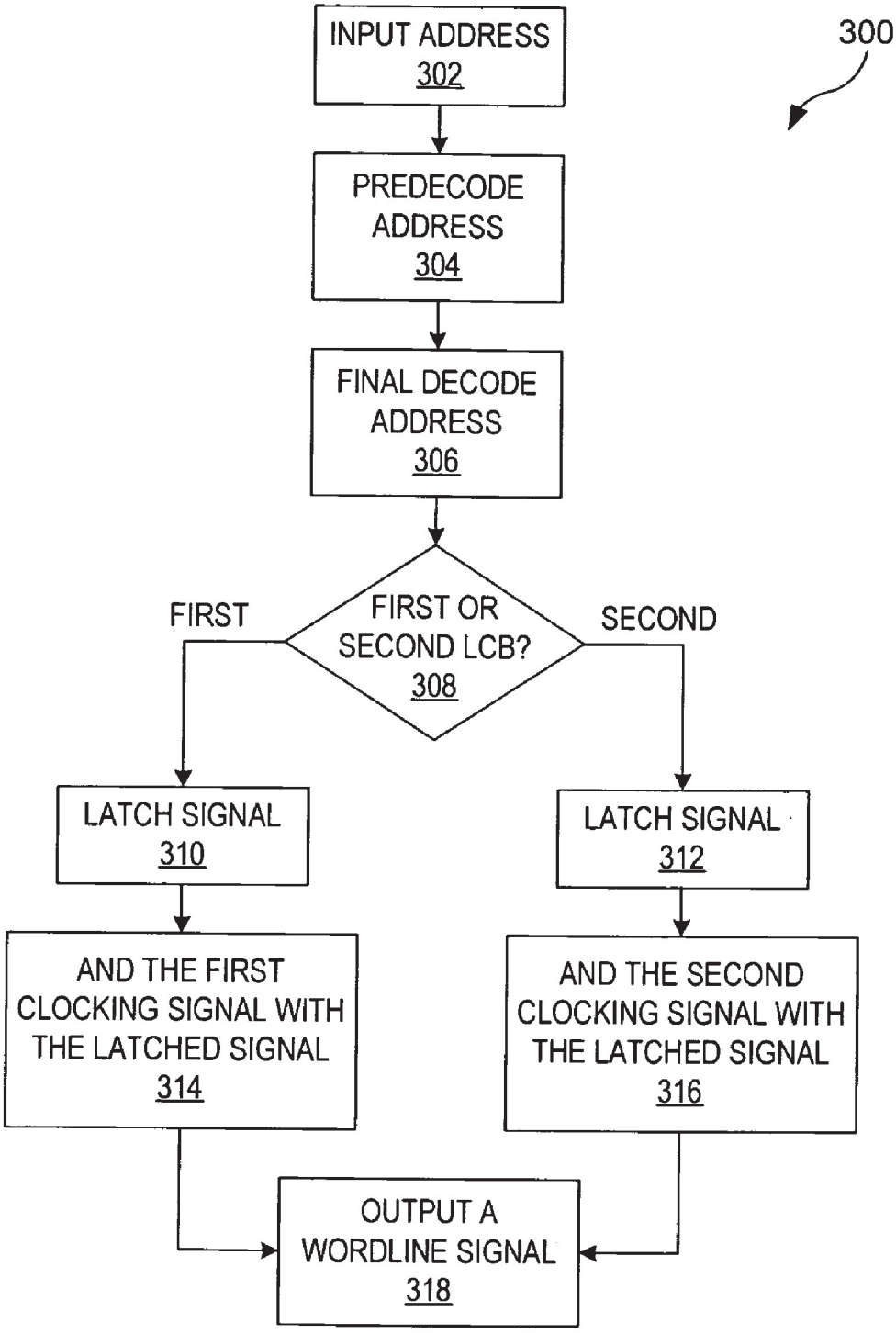


FIG. 3

APPARATUS AND METHOD OF WORD LINE DECODING FOR DEEP PIPELINED MEMORY

FIELD OF THE INVENTION

[0001] The present invention relates generally to memory arrays, and more particularly, to wordline decoding for memory arrays.

DESCRIPTION OF THE RELATED ART

[0002] In conventional memory arrays, the pipeline is becoming increasingly deep. Additionally, the performance of memory arrays is becoming increasingly important to assist in high speed computations and computer performance. However, in deep pipelined high performance memory, a wordline driver has a cycle bound that starts the access cycle. To utilize a cycle bound to initiate the access cycle, wordline drivers typically employ latches. Each latch employed then consumes power.

[0003] Referring to **FIG. 1** of the drawings, the reference numeral **100** generally designates conventional memory. The memory **100** comprises a predecoder **102**, a final decoder **104**, 64 wordline (WL) drivers **106**, a local clock buffer (LCB) **108**, and a 64 wordline array **114**.

[0004] To begin the access cycle for the memory **100**, an address is first received at the predecoder **102** through a first communication channel **116**. Typically, the address is 6 bits long, and from those 6 bits, the predecoder derives two distinct wordline select signals, an X wordline select signal and a Y wordline select signal. The X wordline select signal is 8 bits long and is output to the final decoder **104** through a second communication channel **118**. The Y wordline select signal is output to the final decoder **104** through a third communication channel **120** and is 8 bits long.

[0005] Once the X wordline select signal and the Y wordline select signal have been transmitted to the final decoder **104**, the final decoder **104** determines which of the 64 wordline drivers **106** are to be enabled. The wordline enable signals are communicated to the wordline drivers **106** through a fourth communication channel **122**. The LCB **108** provides a clocking signal to the wordline drivers **106** through a fifth communication channel **128**. The clocking signal from the LCB **108** is usually based on two inputs, a clock input and an enable input, which are provided to the LCB **108** through a sixth communication channel **124** and a seventh communication channel **126**, respectively.

[0006] Each of the wordlines within the array **114** has an associated driver. Each driver comprises a latch and an AND gate, so that for the 64 wordline array **114**, there are 64 drivers. For the sake of illustration, a single latch **110** and an AND gate **112** are depicted. To function, the latch **110** receives a wordline enable signal through the fourth communication channel **122**, where the signal is latched. The latch **110** then outputs a signal to the AND gate **112** through an eighth communication channel **130**. The AND gate **112** also received the clocking signal from the LCB **108** through the fifth communication channel **128**. The AND gate **112** then outputs a wordline signal to a wordline within the 64 wordline array **114** through a ninth communication channel **132**.

[0007] [illegible]

clock load for the wordline timing signal can be high. Because of the large number of latches, there is a substantial risk of soft errors, and more latches require more clock power. Therefore, there is a need for a method and/or apparatus for storing data that addresses at least some of the problems associated with conventional memories.

SUMMARY OF THE INVENTION

[0008] The present invention provides a wordline (WL) driver method, apparatus, and computer program for reducing required latches in a WL decode path for deep pipleined memory and for use in a WL decode scheme. As with many systems, a plurality of timing signals are generated. A WL driver then receives a WL enable data signal. Once received, a plurality of WL signals are generated based on the plurality of timing signals and the WL enable data signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] **FIG. 1** is a block diagram depicting conventional memory;

[0011] **FIG. 2** is a block diagram depicting modified memory; and

[0012] **FIG. 3** is a flow chart depicting the operation of the modified memory.

DETAILED DESCRIPTION

[0013] In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, those skilled in the art will appreciate that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block diagram form in order not to obscure the present invention in unnecessary detail. Additionally, for the most part, details concerning network communications, electro-magnetic signaling techniques, and the like, have been omitted inasmuch as such details are not considered necessary to obtain a complete understanding of the present invention, and are considered to be within the understanding of persons of ordinary skill in the relevant art.

[0014] It is further noted that, unless indicated otherwise, all functions described herein may be performed in either hardware or software, or some combinations thereof. In a preferred embodiment, however, the functions are performed by a processor such as a computer or an electronic data processor in accordance with code such as computer program code, software, and/or integrated circuits that are coded to perform such functions, unless indicated otherwise.

[0015] Referring to **FIGS. 2 and 3** of the drawings, the reference numerals **200** and **300** generally designate modified memory and the operation of the modified memory. The memory **200** comprises a predecoder **202**, a final decoder **204**, **32** wordline drivers **206** a first LCB **208**, a second LCB **234**, and a 64 wordline array **214**.

[0016] [illegible]

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