IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Jentsung Lin	
U.S. Patent No.:	7,693,002	Attorney Docket No.: 39521-0054IP1
Issue Date:	April 6, 2010	
Appl. Serial No.:	11/548,132	
Filing Date:	October 10, 2006	
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS	

DECLARATION OF Robert W. Horst, Ph.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

QUALIFICATIONS AND BACKGROUND INFORMATION

1. I am currently an Adjunct Research Professor in the Department of Electrical and Computer Engineering the University of Illinois at Urbana-Champaign and am also an independent consultant at HT Consulting. I am an independent consultant with more than 30 years of expertise in the design and architecture of computer systems. I have testified as an expert witness and consultant in patent and intellectual property litigation as well as *inter partes* reviews and re-examination proceedings. My curriculum vitae is provided (as APPLE-1004).

2. I earned my M.S. (1978) in electrical engineering and Ph.D. (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master's program, I designed, constructed and debugged a shared memory

parallel microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded task flow computer.

3. After receiving my bachelor's degree and while pursuing my master's degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to 1999, I worked at Tandem Computers, which was acquired by Compaq Computers in 1997. While at Tandem, I was a designer and architect of several generations of fault-tolerant computer systems and was the principal architect of the NonStop Cyclone superscalar processor. The system development work at Tandem also included development of the ServerNet System Area Network and applications of this network to fault tolerant systems and clusters of database servers.

4. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware, Network Appliance, Tibion, and AlterG in the areas of network-attached storage and biomedical devices. From 2012 to 2015, I was Chief Technology Officer of Robotics at AlterG, Inc., where I worked on the design of anti-gravity treadmills and battery-powered orthotic devices to assist those with impaired mobility.

5. In 2001, I was elected an IEEE Fellow "for contributions to the architecture and design of fault tolerant systems and networks." I have authored

over 30 publications, have worked with patent attorneys on numerous patent applications, and I am a named inventor on 82 issued U.S. patents.

6. My patents include those directed to memory system design including U.S. Pat. No. 5,146,589 (Refresh control for dynamic memory in multiple processor system), U.S. Pat. No. 5,287,472 (Memory system using linear array wafer scale integration architecture), and U.S. Pat. No. 5,329,629 (Apparatus and method for reading, writing, and refreshing memory with direct virtual or physical access). My patents also include aspects of circuit design including U.S. Pat. No 5,034,964 (N:1 time-voltage matrix encoded I/O transmission system) and U.S. Pat. No. 9,893,604 (Circuit with low DC bias storage capacitors for high density power conversion).

7. In writing this Declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of memory systems and circuit design and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent No. 7,693,002 (APPLE-1001), and its accompanying prosecution history (APPLE-1002)
- U.S. Patent No. 4,951,259 ("Sato") (APPLE-1005)
- U.S. Patent Pub. No. 2006/0098520 ("Asano") (APPLE-1006)

- Kiyoo Itoh, *VLSI Memory Chip Design*, (Springer 2001) ("Itoh") (APPLE-1007)]
- Stephen Brown et al., *Fundamentals of Digital Logic with Verilog Design*, (McGraw Hill 2003) ("Brown") (APPLE-1009)
- U.S. Patent No. 6,483,771 to Tae-jeen Shin ("Shin") (APPLE-1011)

OVERVIEW OF CONCLUSIONS FORMED

8. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-28 and 31-37 of the '002 patent are rendered obvious by Sato.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-17, 20-28, and 31-36 of the '002 patent are rendered obvious by Asano and Itoh.

BACKGROUND KNOWLEDGE ONE OF SKILL IN THE ART WOULD HAVE HAD PRIOR TO THE PRIORITY DATE OF THE '002 PATENT

9. The technology in the '002 patent at issue generally relates to a circuit device that includes a first and second logic to decode a memory address. The patent specification and figures include CMOS circuits and memory system block diagrams. Prior to the priority date of the '002 patent, there existed numerous

products, publications, and patents that implemented or described the functionality claimed in the ’002 patent. Thus, the methodology of the ’002 patent was well-known in the prior art. Further, to the extent there was any problem to be solved in the ’002 patent, it had already been solved in the prior art systems before the priority date of the ’002 patent.

10. Fig. 1 of the ’002 patent is a block diagram showing the elements for driving wordlines in a memory array.

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