### UNITED STATES PATENT AND TRADEMARK OFFICE

## BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc. Petitioner

v.

Qualcomm Incorporated Patent Owner

Case IPR2018-01249 Patent 7,693,002

PATENT OWNER RESPONSE TO PETITION FOR *INTER PARTES* REVIEW PURSUANT TO 37 C.F.R. § 42.220

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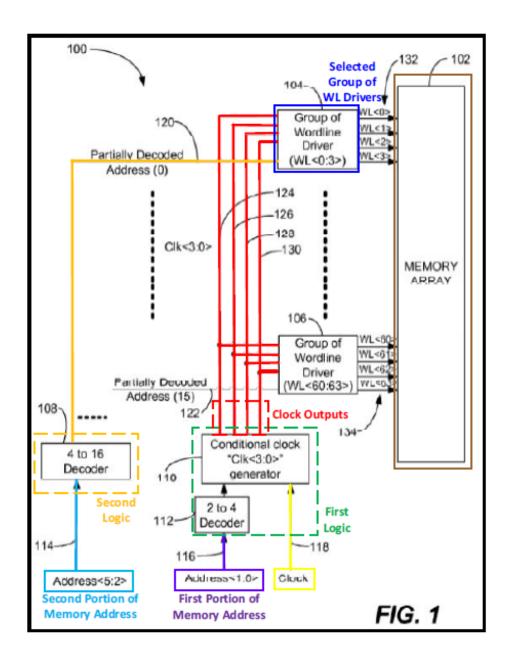
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Pursuant to the Board's Decision – Institution of *Inter Partes* Review (Paper 6), entered January 15, 2019 – Patent Owner Qualcomm, Inc. ("Qualcomm" or "Patent Owner") submits this response in opposition to the petition for *inter partes* review of U.S. Patent No. 7,693,002 (the "'002 patent") filed by Apple Inc. ("Apple" or "Petitioner").

#### I. INTRODUCTION

The '002 patent describes and claims an improved wordline driver system. In that system, a received memory address specifying a particular wordline of a memory array is split into first and second portions. Ex. 1001 at 3:18-25. A first logic receives and decodes the first portion of the memory address, and a second logic receives and decodes the second portion. *Id.* at 3:26-28, 3:37-40. The first logic also receives a clock signal and applies the clock signal to a selected clock output based on the first portion of the memory address. *Id.* at 3:28-36, 9:35-40. The second logic, by contrast, selectively activates a particular wordline driver based on the second portion of the memory address. *Id.* at 3:9-4:8. With this arrangement, the clock loading for the synchronous memory circuit is significantly reduced. Ex. 2001 at ¶34-35, 67. The first and second logics of the '002 patent are shown in the annotated illustration below.



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The first and second logics operate independently of each other and apply their respective outputs directly to wordline drivers in parallel, thus reducing a timing delay in providing the clock signal to a particular wordline driver. Ex. 2001

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