Trials@uspto.gov
571-272-7822

Paper 6
Entered: January 15, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Case IPR2018-01249
Patent 7,693,002 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Apple Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–28 and 31–37 of U.S. Patent No. 7,693,002 B2 ("the '002 patent," Ex. 1001). Paper 2 ("Pet."). Qualcomm Incorporated ("Patent Owner") did not file a Preliminary Response. Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response, if one is filed, shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

After considering the Petition and associated evidence, we institute an *inter partes* review as to all challenged claims and on all grounds raised in the Petition.

A. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 82; Paper 3, 2.

B. The '002 Patent and Illustrative Claim

The '002 patent generally relates wordline drivers and decoders for memory arrays. Ex. 1001, [57], 1:7–9. Figure 1 of the '002 patent is reproduced below.

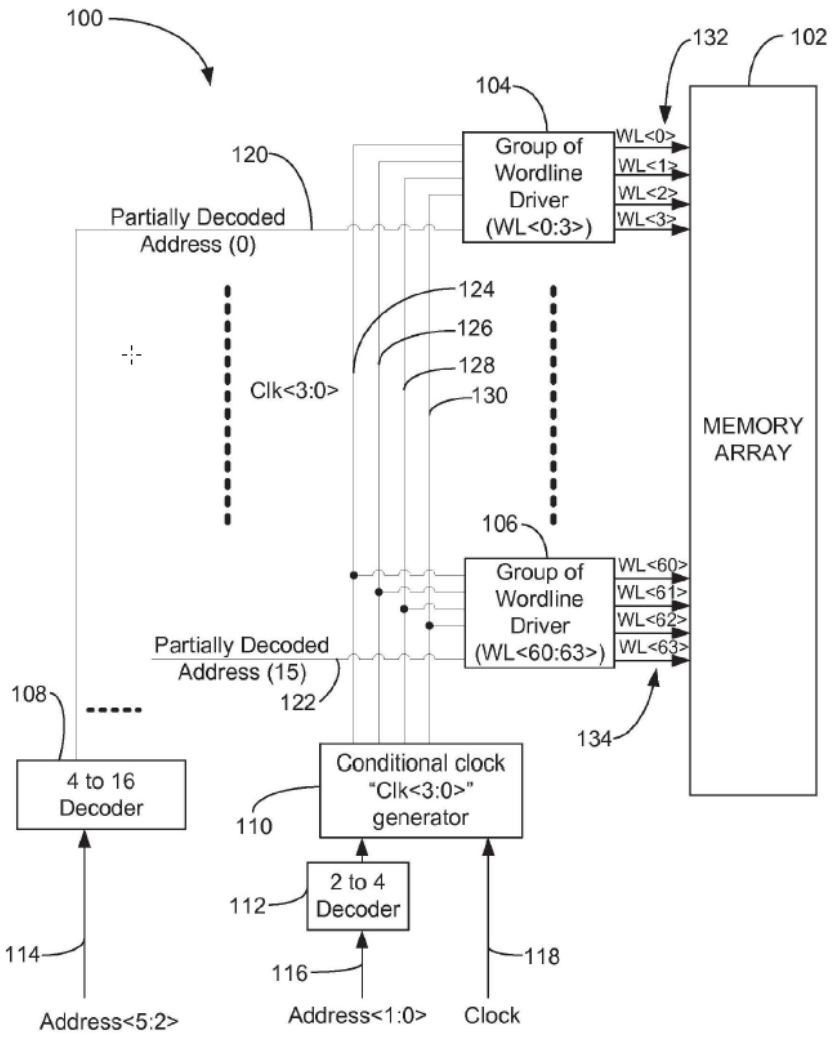

FIG. 1

Figure 1 is a block diagram of an embodiment of a wordline driver system 100. Ex. 1001, 2:31–34. Figure 1 shows groups of wordline drivers 104 and 106 that control particular wordlines in memory array 102. *Id.* at 2:53–3:8. Group of wordline drivers 104 drives wordlines WL<0> through WL<3>, and group of wordline drivers 106 drives wordlines WL<60> through WL<63>. *Id.* Additional wordline drivers that are not shown control the wordlines between WL<3> and WL<60>. *Id.* at 3:4–8.

In operation, two-to-four bit decoder 112 decodes the first portion (such as bits 0 and 1) of a six-bit memory address, and four-to-sixteen bit decoder decodes the remaining portion of the address (bits 2 through 5). Ex. 1001, 3:9–25. Based on the decoded first portion of the address received from decoder 112, conditional clock generator 110 "selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130," each of which is coupled to a particular wordline driver in each group of wordline drivers. *Id.* at 3:26–34. "The four-to-sixteen bit memory address decoder 108 decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address." *Id.* at 3:37–40. For example, if the partially-decoded address indicates that the first group of wordlines is addressed (WL<0> through WL<3>), decoder 108 applies a signal to address line 120, which, as shown in Figure 1, connects to group of wordline drivers 104. Ex. 1001, 3:41–67. The '002 patent explains that "the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104." *Id.* at 4:3–8.

Of the challenged claims, claims 1, 7, 11, 17, 21, and 23–27 are independent. Claim 1, reproduced below, is illustrative.

> 1. A circuit device comprising:
>
> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

C. References

Petitioner relies upon the following references:

Sato	US 4,951,259	Aug. 21, 1990	Ex. 1005
Asano	US 2006/0098520 A1	May 11, 2006	Ex. 1006
Kiyoo Itoh, *VLSI Memory Chip Design*, 2001 ("Itoh")			Ex. 1007

D. Asserted Grounds of Unpatentability

Petitioner asserts claims 1–28 and 31–37 of the '002 patent are unpatentable based on the grounds set forth in the table below.

Reference(s)	**Basis**	**Claims**
Sato	§ 103	1–28 and 31–37
Asano and Itoh	§ 103	1–17, 20–28, and 31–36

II. ANALYSIS

A. Claim Construction

Petitioner proposes constructions for various claim terms. Pet. 3–7. For purposes of deciding whether to institute a trial, we do not find it necessary to construe expressly any claim terms. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy' . . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

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