Apple, Inc. (Petitioner)

v.

Qualcomm Incorporated (Patent Owner)

Petitioner Demonstratives

Case No. IPR2018-01249
U.S. Patent No. 7,693,002

Before Hon. Trevor M. Jefferson, Daniel J. Galligan, and Scott B. Howard
Administrative Patent Judges

FISH.

Issues

- Challenged '002 Patent

- Issue 1: Whether Asano/Itoh Combination Teaches distinct "first" and "second logic"

- Issue 2: Whether Patent Owner's Construction of "Clock Signal" is Improper

- Issue 3: Whether Sato Renders the '002 Patent Claims Obvious
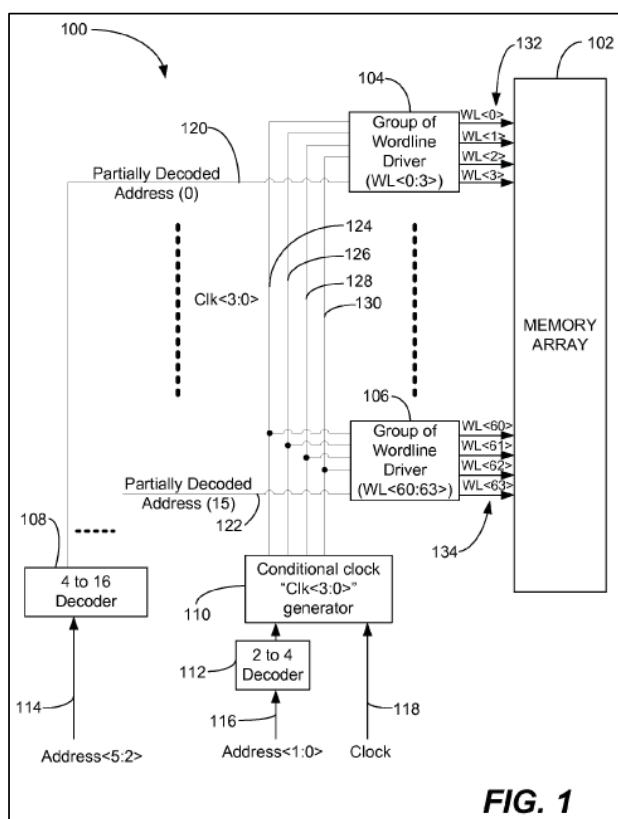
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Challenged '002 Patent

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'002 Overview
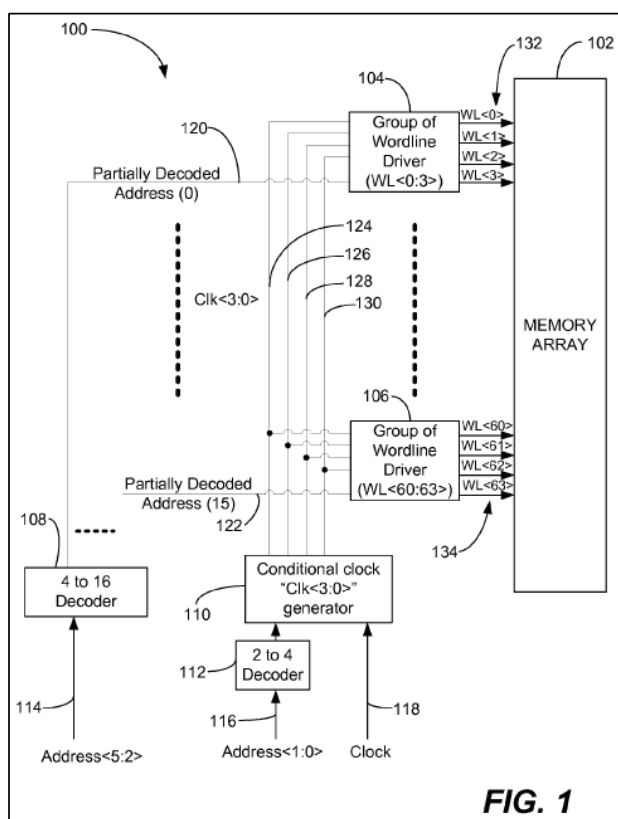

'002 Patent (APPLE-1001), FIG. 1.

- U.S. Patent No. 7,693,002 ("the '002 patent") includes 38 claims, of which claims 1, 7, 11, 17, 21, 23, 24, 25, 26, 27, and 29 are independent.

- The '002 Patent's claims are directed toward, e.g., "dynamic wordline drivers and decoders for memory arrays" and "[a] method of selecting a particular wordline of a memory array."

- IPR2018-01249 challenges claims 1-28 and 31-37 of the '002 patent under 35 U.S.C. § 103 in two independent grounds.

<div align="right">'002 Patent (APPLE-1001), 1:8-9, 10:65-16:9; Petition, 1-2, 7-8.</div>

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'002 Patent Fig. 1

FIG. 1

Q. Would a person of ordinary skill in the art have understood that the 2 to 4 decoder labeled 112 and the conditional clock generator labeled 110 were separate and distinct circuits in the '002 patent?

A. I think a POSA looking at a figure like this would have understood that this is drawn to serve as a functional block diagram describing the major blocks that are needed, functionally, to produce the final wordline driving function into the memory array.

I don't think a POSA, and I don't believe a POSA would look at this functional block diagram and conclude that, therefore, the 2 to 4 decoder and the conditional clock generator block have to be implemented as two separate locks, as such.

Pedram Depo. (APPLE-1019), 50:4-18; Pet. Reply, 22.

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