

**Apple Inc.**  
**v.**  
**Qualcomm Incorporated**

IPR2018-01249

U.S. Patent No. 7,693,002

**Patent Owner's Demonstrative Exhibits**

# U.S. Patent No. 7,693,002

(12) **United States Patent  
Lin**

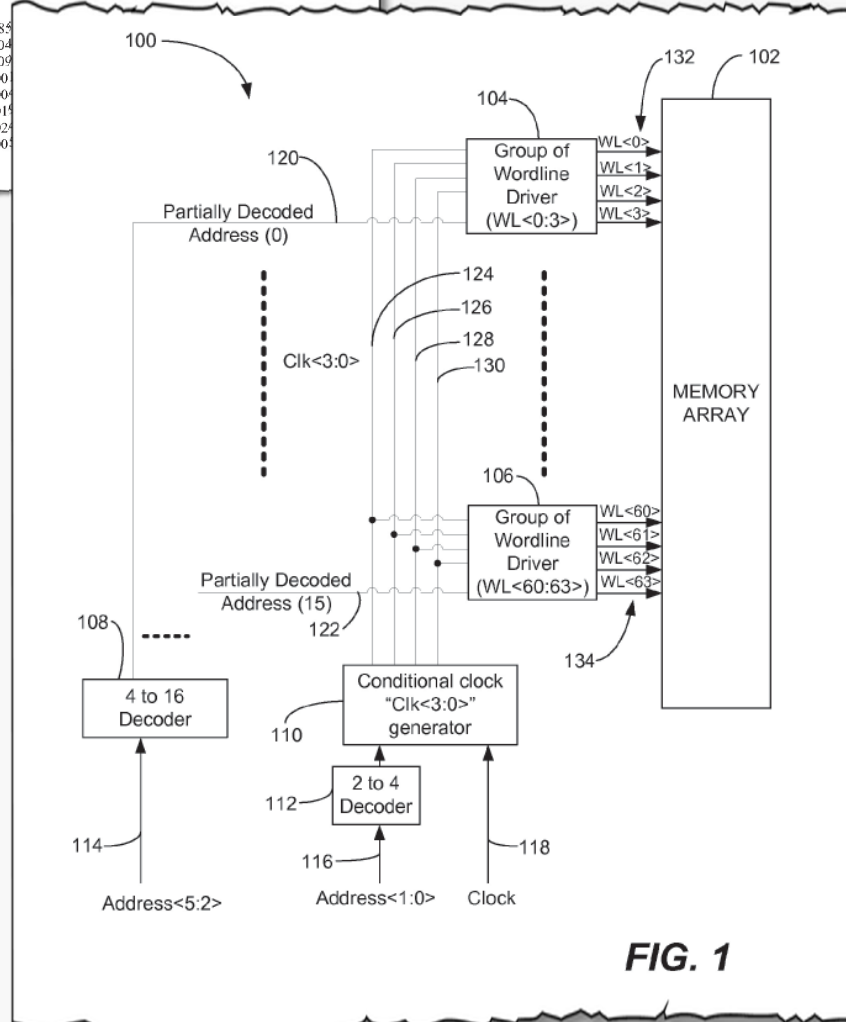
(10) **Patent No.:** US 7,693,002 B2  
(45) **Date of Patent:** Apr. 6, 2010

(54) **DYNAMIC WORD LINE DRIVERS AND  
DECODERS FOR MEMORY ARRAYS**

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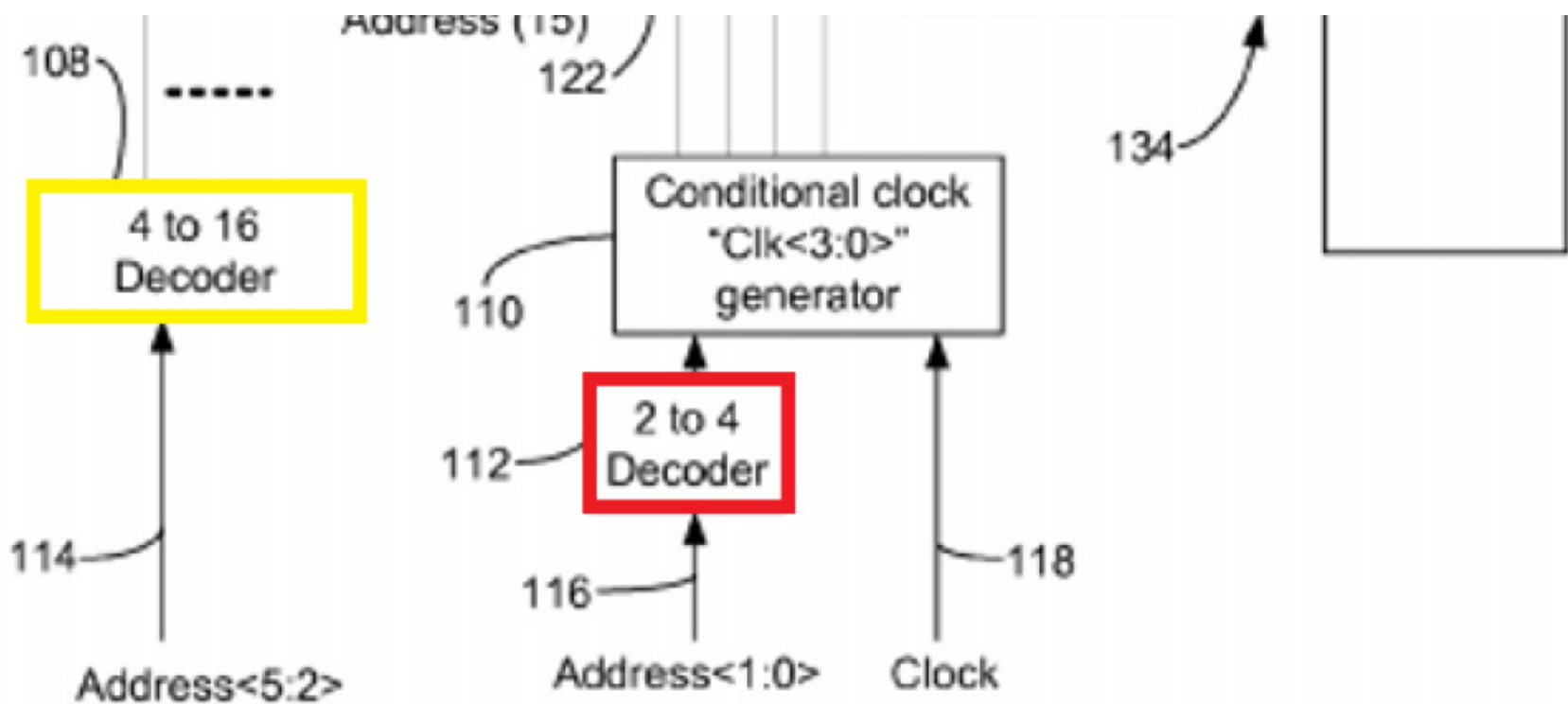
6.85  
7.04  
7.09  
2001/00  
2003/00  
2004/01  
2004/02  
2005/00



**FIG. 1**

Ex. 1001 at Fig. 1

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**FIG. 1**

## '002 Patent – Claim 1

1. A circuit device comprising:  
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and  
second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Ex. 1001 at 10:65-11:10

## Contested Grounds

Ground	Claims	Grounds for Review
1	1-28 and 31-37	Obvious over Sato
2	1-17, 20-28, 31-36	Obvious over Asano and Itoh

Paper 2 at 2

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