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(54) SEMICONDUCTOR MEMORY DEVICE AND METHOD OF OPERATION HAVING DELAY PULSE GENERATION

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- (22) Filed: Jun. 7, 2001

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- (51) Int. Cl.⁷ G11C 8/00
- (52) U.S. Cl. 365/233; 365/194; 365/230.03

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(57) ABSTRACT

A semiconductor memory device including a memory core block, a logic circuit and a direct access circuit which control the memory core block, and a delay pulse generation circuit. The logic circuit generates first and second internal clock signals responsive to first and second external clock signals, and operates the memory core block at high speed during a normal operation. The direct access circuit generates first and second internal clock signals responsive to first and second external clock signals, to test the memory core block during a direct access operation. The delay pulse generation circuit generates a pulse signal corresponding to the delay difference between the first and second internal clock signals generated by the direct access circuit. The delay difference is used by a tester to compensate for actual delay of the internal clock signals when the memory core block is tested during the direct access operation.

18 Claims, 3 Drawing Sheets

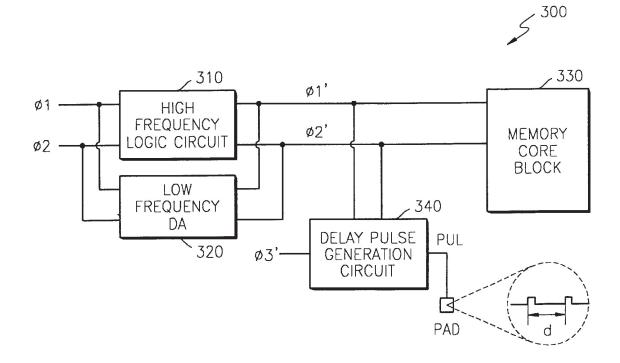


FIG. 1 (PRIOR ART)

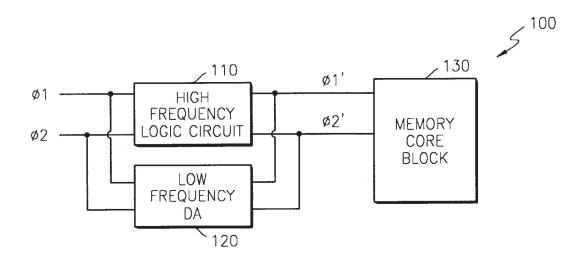
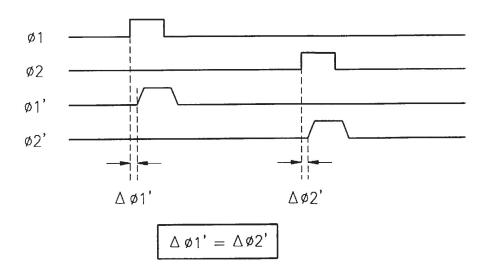
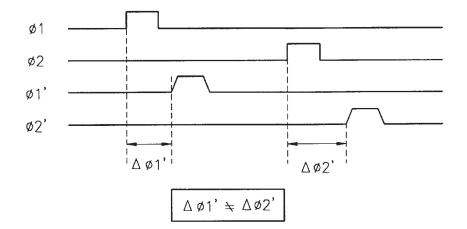


FIG. 2A (PRIOR ART)

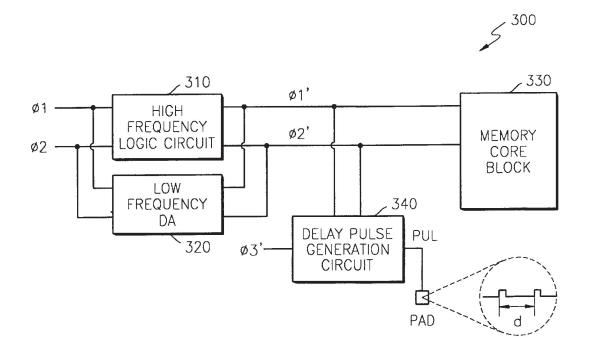


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FIG. 2B (PRIOR ART)







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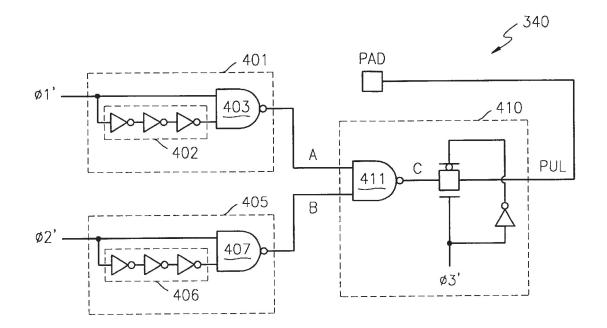
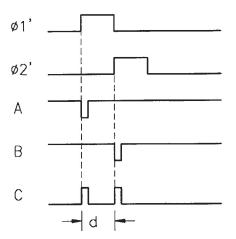


FIG. 5



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SEMICONDUCTOR MEMORY DEVICE AND METHOD OF OPERATION HAVING DELAY **PULSE GENERATION**

The present application claims priority under 35 U.S.C. 5 §119 to Korean Application No. 00-37398 filed on Jun. 30, 2000, which is hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory device and method of operation thereof, and more particularly, to delay pulse generation for measuring the delay between internal control signals.

2. Description of the Related Art

As computer systems deliver higher and higher performance, it is necessary for semiconductor memory devices to have a large capacity and operate at high speed. Semiconductor memory devices can have a large capacity by including memory blocks each having a plurality of 20 memory cells, and can operate at a high speed through a logic circuit operating at a high frequency.

FIG. 1 is a schematic diagram illustrating a conventional semiconductor memory device. Referring to FIG. 1, a semiconductor memory device 100 includes a high frequency 25 logic circuit 110, a low frequency direct access unit (DA) 120 and a memory core block 130. The high frequency logic circuit 110 is generally controlled by external clock signals $\phi 1$ and $\phi 2$, and generates internal clock signals $\phi 1'$ and $\phi 2$ to control the operation of the memory core block 130. Therefore, the memory core block 130 operates at high speed according to the operation specifications of an actual semiconductor memory device. The low frequency DA 120 is used for testing for defects of memory cells within the memory core block 130. The low frequency DA 120 35 capable of operating a memory core block under the same receives the external clock signals $\phi 1$ and $\phi 2$ without operation of the high frequency logic circuit 110, and generates internal clock signals $\phi 1'$ and $\phi 2'$ to control the operation of the memory core block 130. Since it is not necessary to operate the memory core block 130 at high speed during $_{40}$ invention, there is provided a semiconductor memory device testing for defects of memory cells, the low frequency DA 120 operates at low speed.

The internal clock signals $\phi 1'$ and $\phi 2'$ generated by the high frequency logic circuit 110 have different delay times than the internal clock signals $\phi 1'$ and $\phi 2'$ generated by the 45 low frequency DA 120. This will be described with reference to the timing chart shown in FIGS. 2A and 2B. FIG. 2A illustrates the internal clock signals $\phi 1'$ and $\phi 2'$ generated by the high frequency logic circuit 110 in response to the external clock signals $\phi 1$ and $\phi 2$. Since the high frequency 50 logic circuit 110 operates in synchronous relation to a clock signal, the delay time $\Delta \phi \mathbf{1}'$ between the first external clock signal $\phi 1$ and the first internal clock signal $\phi 1'$ is almost the same as the delay time $\Delta \phi 2'$ between the second external clock signal $\phi 2$ and the second internal clock signal $\phi 2'$.

FIG. 2B shows the internal clock signals $\phi 1'$ and $\phi 2'$ generated by the low frequency DA 120. Unlike the high frequency logic circuit 110, the low frequency DA 120 asynchronously operates, and a load on a path through which the first internal clock signal $\phi 1'$ is generated is different 60 from a load on a path through which the second internal clock signal $\phi 2'$ is generated in the low frequency DA 120. Accordingly, the delay time $\Delta \phi 1'$ between the first external clock signal $\phi 1$ and the first internal clock signal $\phi 1'$ is different from the delay time $\Delta \phi 2'$ between the second 65 response to a third internal clock signal. external clock signal $\phi 2$ and the second internal clock signal φ**2**'.

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The internal clock signals $\phi 1'$ and $\phi 2'$ are important to the operation of the memory core block 130. When the internal clock signals $\phi 1'$ and $\phi 2'$ are generated at different times, that is, when $\Delta \phi 1'$ is different from $\Delta \phi 2'$, there may be an error in the operation of memory core block 130. In other words, the memory core block 130 operates normally depending on the internal clock signals $\phi 1'$ and $\phi 2'$ simultaneously generated (i.e. $\Delta \phi 1' = \Delta \phi 2'$) while the semiconductor memory device 100 is operating at high speed in relation with the $_{10}$ high frequency logic circuit **110**. However, the memory core block 130 does not operate properly due to the internal clock signals $\phi 1'$ and $\phi 2'$ sequentially generated with a delay time therebetween (i.e. $\Delta \phi 1' \neq \Delta \phi 2'$) while the semiconductor memory device 100 is operating at low speed in relation with the low frequency DA 120. Even if the memory core block 130 does not operate in error while it is being operated by the low frequency DA 120, the memory core block 130 does not satisfy the conditions of normal operation. Consequently, complete operating conditions required for testing memory cells within the memory core block 130 using a direct access method cannot be achieved.

Therefore, a memory device which can operate a memory core block under the same conditions both when the memory core block operates depending on a high frequency logic circuit and when the memory core block operates depending on a low frequency DA, is desired.

SUMMARY OF THE INVENTION

The present invention is therefore directed to a semiconductor memory device and method of operation which substantially overcomes one or more of the problems due to the limitations and disadvantages of the related art.

To solve the above problems, it is an object of the present invention to provide a semiconductor memory device conditions during high speed operation and during a direct access operation without a delay between internal clock signals.

Accordingly, to achieve the above objects of the including a memory core block including a plurality of memory cells; a logic circuit that generates a first internal clock signal and a second internal clock signal in response to a first external clock signal and a second external clock signal, respectively, and that operates the memory core block at high speed, during normal operation; a direct access circuit that generates the first internal clock signal and the second internal clock signal in response to the first external clock signal and the second external clock signal, respectively, to test the memory cells within the memory core block during a direct access operation; and a delay pulse generation circuit that generates a pulse signal corresponding to the delay difference between the first internal clock signal and the second internal clock signal generated 55 by the direct access circuit.

The delay pulse generation circuit may include a first internal pulse generator that receives the first internal clock signal and that generates a first internal pulse signal having a predetermined pulse width; a second internal pulse generator that receives the second internal clock signal and that generates a second internal pulse signal having a predetermined pulse width; and a pulse signal generator that receives the first and second internal pulse signals and that generates the pulse signal. The pulse signal is transmitted to a pad in

According to the semiconductor memory device of the present invention, the time period of the pulse signal gen-

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