UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,693,002 B2
APPLICATION NO. : 11/548132
DATED : April 6, 2010
INVENTOR(S) : Lin

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 13, claim 14: “appling” to read as --applying--

Column 13, line 59, claim 26: “the second portion” to read as --a second portion--

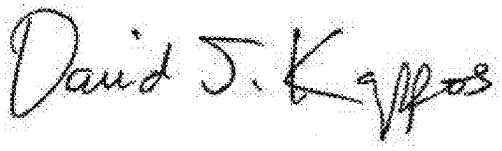
Column 13, line 62, claim 26: “a second portion” to read as --the second portion--

Column 14, line 24, claim 29: “the selected wordline driver” to read as --a selected wordline driver--

Column 16, line 4, claim 38: “wheren” to read as --wherein--

Column 16, line 7, claim 38: “a clock signal” to read as --the clock signal--

Signed and Sealed this
Fifth Day of July, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

061478IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	7,693,002	Confirmation No.	4884
Applicant	:	Jentsung Lin		
Filed	:	October 10, 2006		
Art Unit	:	2827		
Examiner	:	Michael Thanh Tran		
Docket No.	:	061478		
Customer No.	:	23696		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANMITTAL ACCOMPANYING CERTIFICATE OF CORRECTION

Dear Sir:

Attached hereto is a Certificate of Correction for the referenced patent number 7,693,002. The exact page and line number where the error occurs in the application file are:

Column 12, line 13, claim 14: "appling" to read as --applying--
Column 13, line 59, claim 26: "the second portion" to read as --a second portion--
Column 13, line 62, claim 26: "a second portion" to read as --the second portion--
Column 14, line 24, claim 29: "the selected wordline driver" to read as --a selected wordline driver--
Column 16, line 4, claim 38: "wheren" to read as --wherein--
Column 16, line 7, claim 38: "a clock signal" to read as --the clock signal--

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: June 8, 2011

By: /Peter M. Kamarchik/
Peter M. Kamarchik, Reg. No. 63,529
919.297.3170

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 845-4265
Facsimile: (858) 658-2502

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OFCOMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a Collection of information unless it displays a valid OMBControl number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,693,002

APPLICATION NO.: 11/548,132

ISSUE DATE: Apr. 6, 2010

INVENTOR(S): Lin

It is certified that an error appears/errors appear on the above-mentioned Letters Patent is hereby corrected as shown below:

Column 12, line 13, claim 14: “appling” to read as --applying--

Column 13, line 59, claim 26: “the second portion” to read as --a second portion--

Column 13, line 62, claim 26: “a second portion” to read as --the second portion--

Column 14, line 24, claim 29: “the selected wordline driver” to read as --a selected wordline driver--

Column 16, line 4, claim 38: “wheren” to read as --wherein--

Column 16, line 7, claim 38: “a clock signal” to read as --the clock signal--

MAILING ADDRESS OF SENDER:

Kamarchik Peter M.
QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, California 92121

Electronic Patent Application Fee Transmittal	
Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Peter M. Kamarchik/Michelle Sanfilippo
Attorney Docket Number:	061478
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt	
EFS ID:	10261766
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Peter M. Kamarchik/Michelle Sanfilippo
Filer Authorized By:	Peter M. Kamarchik
Attorney Docket Number:	061478
Receipt Date:	08-JUN-2011
Filing Date:	10-OCT-2006
Time Stamp:	16:24:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	3175
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	061478.pdf	69327 3ffa49fc621cdd87e2f7972f5e3d6b62f577d003	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30165 646c107500e70a8adb5f16f7cdb2340b5d0aee6c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	99492		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	04/06/2010	7693002	061478	4884

23696 7590 03/17/2010

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jentsung Lin, Cardiff by the Sea, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23696 7590 11/19/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

TITLE OF INVENTION: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	02/19/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, MICHAEL THANH	2827	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Nicholas J. Pauley
2 Peter Kamarchik
3 Sam Talpalatsky

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: QUALCOMM Incorporated

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Diego, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 170026 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Nicholas J. Pauley Date Feb 2, 2010

Typed or printed name Nicholas J. Pauley Registration No. 44,999

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal	
Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Nicholas John Pauley/Joann Vachon
Attorney Docket Number:	061478
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt	
EFS ID:	6929485
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Vachon
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	02-FEB-2010
Filing Date:	10-OCT-2006
Time Stamp:	13:12:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	9414
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	061478_IFP_02-02-10.pdf	1332522 fe981aaf7e72e878636fb8ccf87ee2c8216650ee	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	31917 8a40e66ca94fede2416e24ee12909470804cb165	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1364439		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23696 7590 11/19/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/19/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

TITLE OF INVENTION: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	02/19/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23696 7590 11/19/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

TITLE OF INVENTION: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	02/19/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, MICHAEL THANH	2827	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 11/19/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/19/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed September 15, 2009*.

2. ☒ The allowed claim(s) is/are *1-16,22-25,28-35,39-47 and 49. The drawings filed October 10, 2006 have been approved*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/MICHAEL T TRAN/
Primary Examiner, Art Unit 2827

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BIB DATA SHEET

CONFIRMATION NO. 4884

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/548,132	10/10/2006	365	2827	061478

APPLICANTS
Jentsung Lin, Cardiff by the Sea, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/01/2007

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MICHAEL THANH TRAN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	27	6

ADDRESS
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE
DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

FILING FEE RECEIVED		
4410	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5592	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/09 07:05
L2	141	L1 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/09 07:05
L3	0	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/09 07:06
L4	0	L3 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/09 07:06
L5	13	365/233.5.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/09 07:07

11/9/2009 7:07:52 AM
C:\Documents and Settings\mtran1\My Documents\EAST\Workspaces\11548132.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009	06/14/2009	11/09/2009			
1	1	✓	=	=	=	=	=			
2	2	O	=	=	=	=	=			
3	3	O	=	=	=	=	=			
4	4	✓	=	=	=	=	=			
5	5	O	=	=	=	=	=			
6	6	O	=	=	=	=	=			
7	7	✓	=	=	=	✓	=			
8	8	✓	=	=	=	✓	=			
9	9	✓	=	=	=	✓	=			
10	10	O	=	=	=	✓	=			
11	11	✓	=	=	=	✓	=			
12	12	✓	=	=	=	✓	=			
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14	14	O	=	=	=	✓	=			
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	20	O	N	N	-	-	-			
	21	O	N	N	-	-	-			
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18	23	O	✓	=	=	O	=			
19	24	O	✓	=	=	O	=			
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27	34		=	=	=	=	=			
28	35		=	=	=	=	=			
	36		N	N	-	-	-			

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009	06/14/2009	11/09/2009			
	37		N	N	-	-	-			
	38		N	N	-	-	-			
29	39		✓	=	=	=	=			
30	40		✓	=	=	=	=			
31	41			=	=	=	=			
32	42			=	=	=	=			
33	43			=	=	=	=			
34	44			=	=	=	=			
35	45			=	=	=	=			
36	46			=	=	✓	=			
37	47			=	=	O	=			
	48			✓	-	-	-			
38	49						=			

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
365	230.06	G	1	1	C	11 / 00 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
365	233.5				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17	26	33	38	49								
2	2		18	27	34										
3	3		19	28	35										
4	4		20		36										
5	5		21		37										
6	6	17	22		38										
7	7	18	23	29	39										
8	8	19	24	30	40										
9	9	20	25	31	41										
10	10		26	32	42										
11	11		27	33	43										
12	12	21	28	34	44										
13	13	22	29	35	45										
14	14	23	30	36	46										
15	15	24	31	37	47										
16	16	25	32		48										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	38	
/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827	11/09/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office Part of Paper No. 20091109

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED

Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt
	updated	3/23/09	mt
	updated	11/9/09	mt

SEARCH NOTES

Search Notes	Date	Examiner
east [see attached]	11/11/07	mt
check 2nd non-final not yet "approved"	4/22/08	mt
east	1/15/09	mt
east	3/23/09	mt
east	6/14/09	mt
east	11/09/09	mt

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
365	230.06	3/23/09	mt
365	233.5	3/23/09	mt
	updated	11/9/09	mt

	/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

In response to the Non-Final Office Action mailed June 17, 2009 ("Office Action"), please reconsider the above-identified application in light of the following amendments and remarks:

REMARKS

Claims 7, 11, 14 and 22 are presently amended. Claim 49 is presently added. No new matter has been added. Claims 1-16, 22-25, 28-35, 39-47 and 49 are currently pending.

The Office indicates, at page 9 of the Office Action, that claims 1-6, 28-35, 39 and 40 are allowable. Applicant thanks the Examiner for these allowances.

The Office has rejected claims 7-10, 11-16, 22, 25, and 46 under 35 U.S.C. §102. Independent claims 7, 11, and 22 are presently amended to include allowable subject matter identified by the Office at page 5 of the Office Action. Specifically, the Office admits that the prior art of record does not show, among other subject matter, "second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address." Applicants presently amend independent claims 7, 11, and 22 to include this allowable subject matter. Claims 7, 11, and 22 are therefore allowable.

Claims 8-10 depend from claim 7. Claims 8-10 are therefore allowable, at least by virtue of their dependence from allowable claim 7. Claims 12-16 and 46 depend from claim 11. Claims 12-16 and 46 are therefore allowable, at least by virtue of their dependence from allowable claim 7. Claim 25 depends from claim 22. Claim 25 is allowable at least by virtue of its dependence form claim 22. Additionally, Applicant has added claim 49 which depends from claim 22. Claim 49 is allowable, at least by virtue of its dependence from claim 22.

Applicant respectfully submits that pending claims 1-16, 22-25, 28-35, 39-47 and 49 are in condition for allowance.

CONCLUSION

Applicant respectfully requests an indication of the allowability of each of the pending claims.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

September 15, 2009
Date

Peter M. Kamarchik
Peter Michael Kamarchik, Reg. No. 63,529
QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502

Electronic Acknowledgement Receipt	
EFS ID:	6077738
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	15-SEP-2009
Filing Date:	10-OCT-2006
Time Stamp:	16:51:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	061478_OAR_09-15-09.pdf	7214843 6adc7bb32b0921fdb41bf05c533e9dd29b18a1e1	no	12
Warnings:					
Information:					

Total Files Size (in bytes):	7214843

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CLAIM AMENDMENTS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. (Original) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. (Original) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. (Original) The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. (Original) The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. (Original) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. (Currently Amended) A method of selecting a particular wordline of a memory array, the method comprising:

decoding a first portion of a memory address of the memory array;

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on [[a]]the first portion of [[a]]the memory address ~~of the memory array~~, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; ~~and~~

decoding a second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to [[a]]the second portion of the memory address.

8. (Previously presented) The method of claim 7, further comprising:

receiving the clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. (Original) The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. (Original) The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. (Currently Amended) A circuit device comprising:

means for decoding a first portion of a memory address of a memory array;

means for selectively providing a clock signal to a selected group of wordline drivers based on [[a]]the first portion of [[a]]the memory address ~~of a memory array~~; ~~and~~

means for decoding a second portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to [[a]]the second portion of the memory address.

12. (Original) The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. (Original) The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. (Currently Amended) The circuit device of claim 12, ~~further comprising a decoder to decode the memory address to determine the second portion of the memory address and~~ wherein the means for decoding a second portion of the memory address further comprises means for appling ~~to apply~~ the second portion of the memory address to a shared address line.

15. (Original) The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. (Original) The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17-21. (Canceled).

22. (Currently Amended) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the group of wordline drivers according to the second portion of the memory address ~~select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver~~.

23. (Original) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. (Original) The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. (Original) The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26-27. (Canceled).

28. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

29. (Previously presented) The circuit device of claim 28, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

30. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

31. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

32. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

33. (Previously presented) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

34. (Previously presented) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array;

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

35. (Previously presented) The circuit device of claim 34, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

36-38. (Canceled).

39. (Previously presented) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

40. (Previously presented) The circuit device of claim 39, wherein a state of the one wordline driver is determined by the selective application of the clock signal.

41. (Previously presented) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output, and wherein the first logic is further to generate multiple conditional clock outputs, wherein one of the multiple conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

42. (Previously presented) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock according to one of the first portion and the second portion of the memory address.

43. (Previously presented) The circuit device of claim 1, wherein the first logic generates a plurality of conditional clock outputs, wherein one of the plurality of conditional clock outputs is active at a time, the first logic to apply the active conditional clock output as the selected clock output.

44. (Previously presented) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input, and wherein the first logic is further to generate four conditional clock outputs, wherein one of the four conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

45. (Previously presented) The method of claim 1, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

46. (Previously presented) The circuit device of claim 11, wherein each of the wordline drivers is associated with a corresponding wordline of the memory array.

47. (Previously presented) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and wherein the logic comprises a conditional clock generator.

48. (Canceled).

49. (New) The circuit device of claim 22, wherein the second logic selects the particular wordline driver of the group of wordline drivers according to the second portion of the memory address and selectively applies a clock signal to one of the plurality of clock outputs to selectively activate the particular wordline.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/548,132	Filing Date 10/10/2006	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	**09/15/2009**	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 38	Minus	** 48	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 11	Minus	***15	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	= 0	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	= 0	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 06/17/2009
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
06/17/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
nanm@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,22-25,28-35 and 39-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6,28-35,39 and 40* is/are allowed.

6)☒ Claim(s) *7-16,22,25 and 46* is/are rejected.

7)☒ Claim(s) *23,24 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *60409*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated June 4, 2009, claims 1-16, 22-25, 28-35, 39-47 are active in this application.

Specification

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

Information Disclosure Statement

3. The information disclosure statements filed June 4, 2009 have been considered.

Claim Objections

4. Claims 23, 24 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections- 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 7-10 are rejected under 35 U.S.C 102(b) as being anticipated by Watanabe et al. [20040190352].

With respect to claim 7, Watanabe et al. disclose, in the figures, a method of selecting a particular wordline of a memory array [see figure 3, via 10i], the method comprising: selectively providing a clock signal [via 1] to a selected group of a plurality of wordline drivers [via 15ia] based on a first portion [via 37b] of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and activating a particular wordline driver of the selected group of wordline drivers according to a second portion [37c] of the memory address.

With respect to claim 8, Watanabe et al. disclose, in the figures, receiving the clock signal; selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address. See figure 3, element 10i.

With respect to claim 9, Watanabe et al. disclose, in the figures, determining a clock output according to the first portion of the memory address using a conditional clock generator. See figure 3, element 1.

With respect to claim 10, Watanabe et al. disclose, in the figures, each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address. See figure 3, elements 1 and 10i.

7. Claims 11-16 and 46 are rejected under 35 U.S.C 102(b) as being anticipated by Watanabe et al. [20040190352].

With respect to claim 11, Watanabe et al. disclose, in the figures, a circuit device comprising:

means for selectively providing a clock signal [figure 3, 1] to a selected group of wordline drivers [15ia] based on a first portion of a memory address [ADDIN connected to 37b] of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers

according to a second portion of the memory address [37c].

With respect to claim 12, Watanabe et al. disclose, in the figures, each of the wordline drivers is associated with a wordline of the memory array. See figure 3.

With respect to claim 13, Watanabe et al. disclose, in the figures, a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address. See figure 3, element 1.

With respect to claim 14, Watanabe et al. discloses, in the figures, a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line. See figure 3, element 10i.

With respect to claim 15, Watanabe et al. discloses, in the figures, the circuit device comprises an integrated circuit. See figure 3, any elements.

With respect to claim 16, Watanabe et al. discloses, in the figures, the integrated circuit includes the memory array. See figure 3, element MBi.

With respect to claim 46, Watanabe et al. discloses, each of the wordline drivers is associated with a corresponding wordline of the memory array. See figure 60.

8. Claims 22 and 25 are rejected under 35 U.S.C 102(b) as being anticipated by Watanabe et al. [20040190352].

With respect to claim 22, Watanabe et al. disclose, in the figures, a circuit device comprising: an address input [see figure 3, electrode coupled to ADD]; a plurality of clock outputs [see figure 3, 10i]; a group of wordline drivers [15ia] coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and logic comprising: first logic to receive a clock signal [41] and a first portion

of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and second logic [15ia] to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

With respect to claim 25, Watanabe et al. disclose, in the figures, the logic comprises a conditional clock generator. See figure 3, element 1.

Allowable Subject Matter

9. Claims 1-6, 28-35, 39 and 40 are allowable over the prior art of record.

10. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.
- the selected wordline driver of the group ofwordline drivers is in an active evaluation state wherein other wordline drivers of the group ofwordline drivers are in a static precharge state.
- the selected wordline driver of the group ofwordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and wherein the logic comprises a conditional clock generator.
- second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.
- each wordline driver in the selected group ofwordline drivers has a shared address input to receive the second portion of the memory address; and activating a particular wordline driver of the selected group ofwordline drivers according to a second portion of the memory address.

- a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

- second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group ofwordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

Conclusion

11. When responding to the Office action, Applicants are advised to provide

the Examiner with line and page numbers of the application and/or references cited to assist the

Examiner in the prosecution of this case.

12. .Any inquiry concerning this communication or earlier communications

from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795.

The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

13. .Any inquiry of a general nature or relating to the status of this application.

should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
June 15, 2009

Notice of References Cited	Application/Control No. 11/548,132	Applicant(s)/Patent Under Reexamination LIN, JENTSUNG	
	Examiner MICHAEL T. TRAN	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0190352	09-2004	Watanabe et al.	365/191
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009	06/14/2009				
	1	✓	=	=	=	=				
	2	O	=	=	=	=				
	3	O	=	=	=	=				
	4	✓	=	=	=	=				
	5	O	=	=	=	=				
	6	O	=	=	=	=				
	7	✓	=	=	=	✓				
	8	✓	=	=	=	✓				
	9	✓	=	=	=	✓				
	10	O	=	=	=	✓				
	11	✓	=	=	=	✓				
	12	✓	=	=	=	✓				
	13	O	=	=	=	✓				
	14	O	=	=	=	✓				
	15	✓	=	=	=	✓				
	16	✓	=	=	=	✓				
	17	✓	N	N	-	-				
	18	✓	N	N	-	-				
	19	O	N	N	-	-				
	20	O	N	N	-	-				
	21	O	N	N	-	-				
	22	✓	✓	=	=	✓				
	23	O	✓	=	=	O				
	24	O	✓	=	=	O				
	25	✓	✓	=	=	✓				
	26		N	N	-	-				
	27		N	N	-	-				
	28		=	=	=	=				
	29		=	=	=	=				
	30		=	=	=	=				
	31		=	=	=	=				
	32		=	=	=	=				
	33		=	=	=	=				
	34		=	=	=	=				
	35		=	=	=	=				
	36		N	N	-	-				

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009	06/14/2009				
	37		N	N	-	-				
	38		N	N	-	-				
	39		✓	=	=	=				
	40		✓	=	=	=				
	41			=	=	=				
	42			=	=	=				
	43			=	=	=				
	44			=	=	=				
	45			=	=	=				
	46			=	=	✓				
	47			=	=	O				
	48			✓	-	-				

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED			
Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt
	updated	3/23/09	mt

SEARCH NOTES		
Search Notes	Date	Examiner
east [see attached]	11/11/07	mt
check 2nd non-final not yet "approved"	4/22/08	mt
east	1/15/09	mt
east	3/23/09	mt
east	6/14/09	mt

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
365	230.06	3/23/09	mt
365	233.5	3/23/09	mt

	/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	Lin-Jentsung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:06
S2	83	clock same (partical or portion) same address same driver same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:07
S3	71	@ay<"2006" and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S4	17745	column same row same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:39
S5	2195	column same row same driver same clock	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S6	287	column same row same driver same clock same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S7	258	@ay<"2006" and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:16

S8	10867	address$2 same driver same (share or "same")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S9	8974	@ay<"2006" and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S10	1691	S9 and (driver same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:20
S11	726	S10 and (address$2 same clock$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:21
S12	240	S11 and (clock same generator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:08
S13	6	"5459684".did. or "6856574".did. or "5596539".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:39
S14	525	select$5 same clock same ((word adj line $1) or wordline$1) same driver same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S15	466	@ay<"2006" and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40

S16	296	S15 and ((activat$3 or enabl$3) same driver same address$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 11:42
S17	114	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2 same invert$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S18	99	@ay<"2006" and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S19	706	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S20	27	S19 and driver$1.ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:06
S21	685	clock same ((word adj line$1) or wordline$1) same driver$1 same address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S22	614	@ay<"2006" and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S23	4037	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17

S25	4306	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S26	97	S25 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S27	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:41
S28	3541	S27 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:42
S29	739	S28 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:44
S30	653	@ay<"2006" and S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:45
S31	63	(first adj fuse) same (second adj fuse) same compar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:01
S32	2	"6728158".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:23

S33	6	"20020166028".did. or "6233191".did. or "4365319".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:14
S34	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S35	3541	S34 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S36	739	S35 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S37	653	@ay<"2006" and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S38	3	S33 and S37	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S39	6	"6856574".did. or "5602796".did. or "20010015926".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 15:01
S40	6	"20040190035".did. or "20050052904".did. or "20040246806".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/15 21:50

S41	2	"6549480".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 09:03
S42	4392	address$3 same (clock $3) same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:28
S43	536	address$3 same (clock $3) same ((word adj line$1) or wordline$1) same (high or activat $3 or enabl$3) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:29
S44	421	@ay<"2006" and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30
S45	0	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30
S46	0	S45 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30
S48	5238	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:32
S50	0	dual same bit$1 same flash same paage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35

S51	63	dual same bit$1 same flash same page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35
S52	41	S51 and simultaneous $2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35
S53	19	S51 and "at same time"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:49
S54	104901	(portion or part) same memory same address $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:49
S55	104901	(portion or part) same memory same address $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:50
S56	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:51
S57	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:51
S58	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:54

S59	75	@ay<"2006" and S58	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:54
S60	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13
S61	384	@ay<"2006" and S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13
S62	309	S61 not S59	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13
S63	626	memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35
S64	501	@ay<"2006" and S63	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35
S65	498	S64 not S62	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35
S66	857	address$3 same clock $3 same ((word adj line $1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:19

S67	687	@ay<"2006" and S66	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S68	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S69	75	@ay<"2006" and S68	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S70	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S71	384	@ay<"2006" and S70	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S72	309	S71 not S69	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S73	626	memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S74	501	@ay<"2006" and S73	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20

S75	498	S74 not S72	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S76	189	S67 not S75	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S77	1	"5826056".did. and S76	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 11:50
S78	0	"5826056"".did"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 11:50
S79	2	"5826056".did. and (address$3 same clock $3 same driver$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 11:51
S80	2	"4365319".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 12:23
S81	5324	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:07
S82	136	S81 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:07

S83	130	365/233.$.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:08
S84	12	365/233.5.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:09
S85	2	"2004190352".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/13 17:15
S86	0	"20041900352".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/13 17:20
S87	2	"20040190352".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/13 17:21

6/14/2009 7:09:28 AM
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (04-09)
Approved for use through 05/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11548132
Filing Date	2006-10-10
First Named Inventor	LIN
Art Unit	2827
Examiner Name	TRAN, MICHAEL THANH
Attorney Docket Number	061478

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7092305		2006-08-15	WATANABE ET AL.	

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U.S.PATENT APPLICATION PUBLICATIONS

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.T./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11548132
	Filing Date	2006-10-10
	First Named Inventor	LIN
	Art Unit	2827
	Examiner Name	TRAN, MICHAEL THANH
	Attorney Docket Number	061478

	1	INTERNATIONAL SEARCH REPORT - PCT/US07/080993 - INTERNATIONAL SEARCH AUTHORITY - EUROPEAN PATENT OFFICE - 2008-05-14	☐
	2	WRITTEN OPINION - PCT/US07/080993 - INTERNATIONAL SEARCH AUTHORITY - EUROPEAN PATENT OFFICE - 2008-05-14	☐

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/080993

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C8/08 G11C8/12 G11C11/408

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/190352 A1 (WATANABE NAOYA [JP] ET AL) 30 September 2004 (2004-09-30)	11-27
A	abstract figures 3,34 paragraphs [0176] - [0199] paragraphs [0400] - [0403]	1-10
A	US 2005/052904 A1 (CHO BEAK-HYUNG [KR] ET AL) 10 March 2005 (2005-03-10) abstract figure 4 paragraphs [0038] - [0058]	1-27
A	US 2004/246806 A1 (HA CHANG WAN [US]) 9 December 2004 (2004-12-09) abstract figure 1 paragraphs [0039] - [0043]	1-27

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents :

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 May 2008	14/05/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Operti, Antonio

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/080993

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004190352 A1	30-09-2004	NONE	
US 2005052904 A1	10-03-2005	KR 20050025730 A	14-03-2005
		US 2006215435 A1	28-09-2006
		US 2006250885 A1	09-11-2006
US 2004246806 A1	09-12-2004	NONE	

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(PCT Rule 43*bis*.1)

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Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/080993	10.10.2007	10.10.2006

International Patent Classification (IPC) or both national classification and IPC
INV. G11C8/08 G11C8/12 G11C11/408

Applicant
QUALCOMM INCORPORATED

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Operti, Antonio Telephone No. +49 89 2399-5781

Form (PCT/ISA/237) (Cover Sheet) (April 2005)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-10
	No:	Claims	11-27
Inventive step (IS)	Yes:	Claims	1-10
	No:	Claims	11-27
Industrial applicability (IA)	Yes:	Claims	1-27
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V.

1. The following document D1: US 2004/190352 A1 (WATANABE NAOYA [JP] ET is referred to in this communication; the numbering will be adhered to the rest of the procedure.

2. The subject-matter of the apparatus claims 1, as far as they can be understood (see Item VIII below), is neither disclosed neither rendered obvious by the available prior art, because it applies the clock signal only to a selected clock output (for ex. CLK<0>), so that the clock drives a single line (130) of a group of wordline drivers (104..106). This apparatus has the advantage of reducing the power consumption and additionally it reduces the layout complexity of the circuit design.

   These apparatus claim 1 would thus appear to meet requirements of Art 33(1) PCT with respect to the available prior art.

   Although these apparatus claim 1 would thus appear to meet requirements of Art. 33(1) PCT with respect to the available prior art, amendment is required to overcome the clarity objections under Item VIII.

3. The same argumentation is also valid for the method according to independent claim 7 and its dependent claims 8-10 representing the same combination of features as apparatus claims 1-6, but formulated as a method. Thus, the subject-matter of claims 7 and 8-10 would thus appear to meet the requirements of novelty and inventive step and thus satisfies the criterion set forth in Article 33(1) PCT.

4. The subject-matter of the claim 11 is not new in the sense of Article 33(2) PCT.
   The document D1 discloses (the references in parentheses applying to this document): means for selectively providing a clock (figure 3, 1) to a selected group of wordlines (15ia and other drivers connected to the other local control circuit 10a) based on a first portion address (ADDIN connected to 37b), means for activating a particular wordline drivers based on a second portion address (37c).

5. The additional features of dependent claims 12-16 appear to add nothing of inventive

significance to claim 11, as the additional features introduced by said dependent claims refer only to minor implementing details which are disclosed or obviously derivable from the cited prior art references or fall within the general knowledge of a person skilled in the art.

6. The subject-matter claims 17-27 essentially corresponds to the subject-matter of claims 11-16. The same objections raised in respect of claims 11-16 (under points above), therefore, apply, mutatis mutandis, to the claims 17-27.

Re Item VII

1. To meet the requirements of Rule 5.1(a)(ii) PCT, the document D1 should be identified in the description and the relevant background art disclosed therein should be briefly discussed.

2. Any independent claim should be in the proper two-part "characterized" form recommended by Rule 63(b) PCT, having a preamble that correctly reflects the nearest prior art represented by document D1.

3. Reference signs in parentheses should be inserted in the claims to increase their intelligibility, Rule 6.2(b) PCT.

Re Item VIII

1. Claim 1 lacks an essential feature so that Art 6 PCT read in combination with Rule 6.3(b) PCT.

   Subject-matter of claim 1 does not say **how** to associate a selected clock with a selected group of a plurality of wordline drivers (claim 1 lines 5-6). According to figure 1, the selected clock output is associated to a **plurality** of wordline drivers (106, 106) and not to a **selected** (for ex. 104) group of a plurality of wordline drivers.

2. The various definition of the invention given by the independent claims 1, 11, 17, 22 and

26 are such that the claims as a whole **are not concise**, so that Article 6 PCT is not met.

Electronic Patent Application Fee Transmittal	
Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Nicholas John Pauley/Joann Denbow
Attorney Docket Number:	061478
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	5457884
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	04-JUN-2009
Filing Date:	10-OCT-2006
Time Stamp:	18:09:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	4390
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	061478_RCE_06-04-09.pdf	2297520 9895a79a2aa9a4040c59dc797fc1667ee7a07131	no	3
Warnings:					
Information:					
2	Transmittal Letter	061478_SIDS_06-04-09.pdf	3748185 ee9228848c2c0b237440482d9d5c96aab2e0e828	no	4
Warnings:					
Information:					
3	NPL Documents	061478_2008-05-14_ISR.pdf	1610559 628f09ca27d3e3f79613e257b4dee50dd5c929cb	no	2
Warnings:					
Information:					
4	NPL Documents	061478_2008-05-14_WO.pdf	224359 4b3ee8a0e272f2a0d93656292eeb65f011221179	no	6
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30459 ff61450b7b6bf11bea641d11dfc2babb57c5681a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7911082		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (08/06)
Approved for use through 08/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11548132	Filing Date	2006-10-10	Docket Number (if applicable)	061478	Art Unit	2827
First Named Inventor	LIN, Jentsung			Examiner Name	TRAN, Michael Thanh		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 170026

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

EFS - Web 2.0

PTO/SB/30EFS (08/08)
Approved for use through 08/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	Peter M. Kamarchik	Date (YYYY-MM-DD)	2009-06-04
Name	Peter M. Kamarchik	Registration Number	63529

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EFS - Web 2.0

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (04-09)
Approved for use through 05/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	11548132
	Filing Date	2006-10-10
	First Named Inventor	LIN
	Art Unit	2827
	Examiner Name	TRAN, MICHAEL THANH
	Attorney Docket Number	061478

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7092305		2006-08-15	WATANABE ET AL.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.13

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11548132
	Filing Date	2006-10-10
	First Named Inventor	LIN
	Art Unit	2827
	Examiner Name	TRAN, MICHAEL THANH
	Attorney Docket Number	061478

	1	INTERNATIONAL SEARCH REPORT - PCT/US07/080993 - INTERNATIONAL SEARCH AUTHORITY - EUROPEAN PATENT OFFICE - 2008-05-14	☐
	2	WRITTEN OPINION - PCT/US07/080993 - INTERNATIONAL SEARCH AUTHORITY - EUROPEAN PATENT OFFICE - 2008-05-14	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11548132
	Filing Date	2006-10-10
	First Named Inventor	LIN
	Art Unit	2827
	Examiner Name	TRAN; MICHAEL THANH
	Attorney Docket Number	061478

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	Peter M. Kamarchik	Date (YYYY-MM-DD)	2009-6-4
Name/Print	PETER M. KAMARCHIK	Registration Number	63529

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Receipt date: 05/29/2008
Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

11548132 - GAU: 2827

PTO/SB/08a (03-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11548132
	Filing Date	2006-10-10
	First Named Inventor	Jentsung Lin
	Art Unit	2827
	Examiner Name	Tran, Michael Thanh
	Attorney Docket Number	061478

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
PAP 4/21/09	1	2004/0190352 ~~20040190035~~		2004-09-30	Watanabe, Naoya	
	2	20050052904		2005-03-10	Cho, Beak-Hung	
	3	20040246806		2004-12-09	Ha, Chang Wan	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NOTICE OF ALLOWANCE AND FEE(S) DUE

23696 7590 04/02/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/02/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

TITLE OF INVENTION: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/02/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
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or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23696 7590 04/02/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

TITLE OF INVENTION: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, MICHAEL THANH	2827	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 04/02/2009

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/02/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed March 19, 2009*.

2. ☒ The allowed claim(s) is/are *1-16,22-25,28-35 and 39-47. The drawings filed October 10, 2006 have been approved*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/MICHAEL T TRAN/
Primary Examiner, Art Unit 2827

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009					
1	1	✓	=	=	=					
2	2	O	=	=	=					
3	3	O	=	=	=					
4	4	✓	=	=	=					
5	5	O	=	=	=					
6	6	O	=	=	=					
12	7	✓	=	=	=					
13	8	✓	=	=	=					
14	9	✓	=	=	=					
15	10	O	=	=	=					
16	11	✓	=	=	=					
17	12	✓	=	=	=					
18	13	O	=	=	=					
19	14	O	=	=	=					
20	15	✓	=	=	=					
21	16	✓	=	=	=					
	17	✓	N	N	-					
	18	✓	N	N	-					
	19	O	N	N	-					
	20	O	N	N	-					
	21	O	N	N	-					
23	22	✓	✓	=	=					
24	23	O	✓	=	=					
25	24	O	✓	=	=					
26	25	✓	✓	=	=					
	26		N	N	-					
	27		N	N	-					
28	28		=	=	=					
29	29		=	=	=					
30	30		=	=	=					
31	31		=	=	=					
32	32		=	=	=					
33	33		=	=	=					
34	34		=	=	=					
35	35		=	=	=					
	36		N	N	-					

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009	03/23/2009					
	37		N	N	-					
	38		N	N	-					
36	39		✓	=	=					
37	40		✓	=	=					
7	41			=	=					
11	42			=	=					
8	43			=	=					
9	44			=	=					
10	45			=	=					
22	46			=	=					
27	47			=	=					
	48			✓	-					

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	MICHAEL T TRAN	2827

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
365	230.06	G	1	1	C	11 / 00 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
365	233.5				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17	33	33										
2	2		18	34	34										
3	3		19	35	35										
4	4		20		36										
5	5		21		37										
6	6	23	22		38										
12	7	24	23	36	39										
13	8	25	24	37	40										
14	9	26	25	7	41										
15	10		26	11	42										
16	11		27	8	43										
17	12	28	28	9	44										
18	13	29	29	10	45										
19	14	30	30	22	46										
20	15	31	31	27	47										
21	16	32	32		48										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	37	
/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827	03/23/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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Part of Paper No. 20090323

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CONFIRMATION NO. 4884

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/548,132	10/10/2006 RULE	365	2827	061478

APPLICANTS
Jentsung Lin, Cardiff by the Sea, CA;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
03/01/2007

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MICHAEL THANH TRAN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	27	6

ADDRESS
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE
DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

FILING FEE RECEIVED		
4410	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5324	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:07
L2	136	L1 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:07
L3	130	365/233.$.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:08
L4	12	365/233.5.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/23 09:09

3/23/2009 9:44:15 AM
C:\Documents and Settings\mtran1\My Documents\EAST\Workspaces\11548132.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the Final Office Action mailed January 28, 2009 ("Final Office Action"), please reconsider the above-identified application in light of the following amendments and remarks:

Entry Approved
/mt/ 3/21/09

CLAIM AMENDMENTS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. (Original) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. (Original) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. (Original) The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. (Original) The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. (Original) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. (Original) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

8. (Previously presented) The method of claim 7, further comprising:

receiving the clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. (Original) The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. (Original) The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. (Original) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

12. (Original) The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. (Original) The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. (Original) The circuit device of claim 12, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

15. (Original) The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. (Original) The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17-21. (Canceled).

22. (Previously presented) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

23. (Original) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. (Original) The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. (Original) The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26-27. (Canceled).

28. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

29. (Previously presented) The circuit device of claim 28, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

30. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

31. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

32. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

33. (Previously presented) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

34. (Previously presented) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array;

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

35. (Previously presented) The circuit device of claim 34, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

36-38. (Canceled).

39. (Previously presented) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

40. (Previously presented) The circuit device of claim 39, wherein a state of the one wordline driver is determined by the selective application of the clock signal.

41. (Previously presented) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output, and wherein the first logic is further to generate multiple conditional clock outputs, wherein one of the multiple conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

42. (Previously presented) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock according to one of the first portion and the second portion of the memory address.

43. (Previously presented) The circuit device of claim 1, wherein the first logic generates a plurality of conditional clock outputs, wherein one of the plurality of conditional clock outputs is active at a time, the first logic to apply the active conditional clock output as the selected clock output.

44. (Previously presented) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input, and wherein the first logic is further to generate four conditional clock outputs, wherein one of the four conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

45. (Previously presented) The method of claim 1, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

46. (Previously presented) The circuit device of claim 11, wherein each of the wordline drivers is associated with a corresponding wordline of the memory array.

47. (Previously presented) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and wherein the logic comprises a conditional clock generator.

48. (Canceled).

REMARKS

The Office has indicated that claims 1-16, 22-25, 28-35, and 39-47 are allowable, at paragraphs 6 and 7 of the Final Office Action. Applicant thanks the Examiner for these allowances. Claims 17-21, 26-27, 36-38, and 48 have been canceled without prejudice or disclaimer. Hence, pending claims 1-16, 22-25, 28-35, and 39-47 are in condition for allowance.

CONCLUSION

Applicant respectfully requests an indication of the allowability of each of the pending claims.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

March 18, 2009
Date

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED

Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt
	updated	3/23/09	mt

SEARCH NOTES

Search Notes	Date	Examiner
east [see attached]	11/11/07	mt
check 2nd non-final not yet "approved"	4/22/08	mt
east	1/15/09	mt
east	3/23/09	mt

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
365	230.06	3/23/09	mt
365	233.5	3/23/09	mt

	/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the Final Office Action mailed January 28, 2009 ("Final Office Action"), please reconsider the above-identified application in light of the following amendments and remarks:

CLAIM AMENDMENTS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. (Original) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. (Original) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. (Original) The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. (Original) The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. (Original) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. (Original) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

8. (Previously presented) The method of claim 7, further comprising:

receiving the clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. (Original) The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. (Original) The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. (Original) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

12. (Original) The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. (Original) The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. (Original) The circuit device of claim 12, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

15. (Original) The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. (Original) The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17-21. (Canceled).

22. (Previously presented) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

23. (Original) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. (Original) The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. (Original) The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26-27. (Canceled).

28. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

29. (Previously presented) The circuit device of claim 28, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

30. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

31. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

32. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

33. (Previously presented) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

34. (Previously presented) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array;

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

35. (Previously presented) The circuit device of claim 34, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

36-38. (Canceled).

39. (Previously presented) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

40. (Previously presented) The circuit device of claim 39, wherein a state of the one wordline driver is determined by the selective application of the clock signal.

41. (Previously presented) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output, and wherein the first logic is further to generate multiple conditional clock outputs, wherein one of the multiple conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

42. (Previously presented) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock according to one of the first portion and the second portion of the memory address.

43. (Previously presented) The circuit device of claim 1, wherein the first logic generates a plurality of conditional clock outputs, wherein one of the plurality of conditional clock outputs is active at a time, the first logic to apply the active conditional clock output as the selected clock output.

44. (Previously presented) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input, and wherein the first logic is further to generate four conditional clock outputs, wherein one of the four conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

45. (Previously presented) The method of claim 1, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

46. (Previously presented) The circuit device of claim 11, wherein each of the wordline drivers is associated with a corresponding wordline of the memory array.

47. (Previously presented) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and wherein the logic comprises a conditional clock generator.

48. (Canceled).

REMARKS

The Office has indicated that claims 1-16, 22-25, 28-35, and 39-47 are allowable, at paragraphs 6 and 7 of the Final Office Action. Applicant thanks the Examiner for these allowances. Claims 17-21, 26-27, 36-38, and 48 have been canceled without prejudice or disclaimer. Hence, pending claims 1-16, 22-25, 28-35, and 39-47 are in condition for allowance.

CONCLUSION

Applicant respectfully requests an indication of the allowability of each of the pending claims.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

March 18, 2009
Date

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Electronic Acknowledgement Receipt

EFS ID:	4994556
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	19-MAR-2009
Filing Date:	10-OCT-2006
Time Stamp:	08:32:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment After Final	061478_FOAR_03-19-09.pdf	100575 cfa6e80f7298af07fd963d630897d4bf803c86b7	no	11

Warnings:	
Information:	

Total Files Size (in bytes):	100575

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/548,132	10/10/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	min us 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/06/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 48	Minus	** 40	= 8	X $ =		OR	X $52=	416
	Independent (37 CFR 1.16(h))	* 15	Minus	***14	= 1	X $ =		OR	X $220=	220
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	636

AMENDMENT	03/19/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 37	Minus	** 48	= 0	X $ =		OR	X $52 =	0
	Independent (37 CFR 1.16(h))	* 11	Minus	*** 15	= 0	X $ =		OR	X $220 =	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 01/28/2009
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
01/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
nanm@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *17-21,26,27 and 36-38* is/are withdrawn from consideration.

5)☒ Claim(s) *1-16,22-25,28-35 and 39-47* is/are allowed.

6)☒ Claim(s) *48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated December 6, 2008, claims 1-48 are active in this application.

This application currently contains an election, to a restriction requirement, with traverse. The Examiner has argued Applicant's grounds of traversing the requirement. However, Applicant has not yet finalized the argument to the requirement. The Examiner has attached the original argument to the traversal below. Applicant is required to argue or withdraw the traversal of the requirement in the next response to expedite the prosecution of this case.

In response to the restriction requirement, Applicant elected group one with traverse. Applicant argued that the examination of all claims is not believed to create an undue burden on the USPTO and since the subject matter among the species is not independent and distinct as required by statute. Additionally, Applicant adds that the different classifications as recited by the USPTO are not adequate grounds for restriction since the USPTO has historically examined applications containing multiple sets of claims with different classifications. However, the Examiner contends that the restriction requirements are proper for the following reasons:

- the two species are distinct – one group merely recites a driver; while the other group specifically defines a particular driver. See definition of the two cited classes and subclasses.
- It is a burden to look for two distinct features in two different subclasses as there are thousands of prior art to consider.
- This office action is prepared for the purposes of examining this case, and only this case. Therefore, the argument of examined cases with multiple sets of claims classified in different classifications is irrelevant.

Specification

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

Claim Rejections- 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claim 48 is rejected under 35 U.S.C 102(b) as being anticipated by Noda [U.S. Patent 5,826,056].

With respect to claim 48, Noda disclose, in the figures, a circuit device comprising: means for providing a clock signal to a selected group of wordline drivers based on a portion of a memory address of a memory array; and means for activating a particular wordline driver of the selected group of wordline drivers according to another portion of the memory address. See 6th paragraph of the Summary of the Invention section.

Remarks

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date

of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Allowable Subject Matter

6. Claims 1-16, 22-25, 28-35 and 39-47 are allowable over the prior art of record.

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

- selectively providing a clock signal to a selected group of a plurality ofwordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality ofwordline drivers is associated with a wordline of the memory array; and activating a particular wordline driver of the selected group ofwordline drivers according to a second portion of the memory address.

- means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

- first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate the selected wordline driver.

- first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

- first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

- first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

- first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

- selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality ofwordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

- means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array; a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

Conclusion

8. When responding to the Office action, Applicants are advised to provide

the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. .Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. .Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
January 26, 2009

Notice of References Cited	Application/Control No. 11/548,132	Applicant(s)/Patent Under Reexamination LIN, JENTSUNG	
	Examiner MICHAEL T. TRAN	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,826,056	10-1998	Noda, Kazuyuki	711/167
*	B	US-7,047,385	05-2006	Bhattacharya et al.	711/169
*	C	US-2003/0046632	03-2003	Hatakenaka et al.	714/763
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009						
	1	✓	=	=						
	2	O	=	=						
	3	O	=	=						
	4	✓	=	=						
	5	O	=	=						
	6	O	=	=						
	7	✓	=	=						
	8	✓	=	=						
	9	✓	=	=						
	10	O	=	=						
	11	✓	=	=						
	12	✓	=	=						
	13	O	=	=						
	14	O	=	=						
	15	✓	=	=						
	16	✓	=	=						
	17	✓	N	N						
	18	✓	N	N						
	19	O	N	N						
	20	O	N	N						
	21	O	N	N						
	22	✓	✓	=						
	23	O	✓	=						
	24	O	✓	=						
	25	✓	✓	=						
	26		N	N						
	27		N	N						
	28		=	=						
	29		=	=						
	30		=	=						
	31		=	=						
	32		=	=						
	33		=	=						
	34		=	=						
	35		=	=						
	36		N	N						

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	11548132	LIN, JENTSUNG
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CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008	01/16/2009						
	37		N	N						
	38		N	N						
	39		✓	=						
	40		✓	=						
	41			=						
	42			=						
	43			=						
	44			=						
	45			=						
	46			=						
	47			=						
	48			✓						

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	857	address$3 same clock $3 same ((word adj line $1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:19
L10	687	@ay<"2006" and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L11	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L12	75	@ay<"2006" and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L13	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L14	384	@ay<"2006" and L13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L15	309	L14 not L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20

L16	626	memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L17	501	@ay<"2006" and L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L18	498	L17 not L15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
L19	189	10 not L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/16 09:20
S1	0	Lin-Jentsung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:06
S2	83	clock same (partical or portion) same address same driver same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:07
S3	71	@ay<"2006" and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S4	17745	column same row same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:39

S5	2195	column same row same driver same clock	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S6	287	column same row same driver same clock same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S7	258	@ay<"2006" and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:16
S8	10867	address$2 same driver same (share or "same")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S9	8974	@ay<"2006" and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S10	1691	S9 and (driver same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:20
S11	726	S10 and (address$2 same clock$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:21
S12	240	S11 and (clock same generator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:08

S13	6	"5459684".did. or "6856574".did. or "5596539".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:39
S14	525	select$5 same clock same ((word adj line $1) or wordline$1) same driver same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S15	466	@ay<"2006" and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S16	296	S15 and ((activat$3 or enabl$3) same driver same address$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 11:42
S17	114	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2 same invert$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S18	99	@ay<"2006" and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S19	706	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S20	27	S19 and driver$1.ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:06

S21	685	clock same ((word adj line$1) or wordline$1) same driver$1 same address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S22	614	@ay<"2006" and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S23	4037	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S25	4306	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S26	97	S25 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S27	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:41
S28	3541	S27 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:42
S29	739	S28 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:44

S30	653	@ay<"2006" and S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:45
S31	63	(first adj fuse) same (second adj fuse) same compar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:01
S32	2	"6728158".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:23
S33	6	"20020166028".did. or "6233191".did. or "4365319".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:14
S34	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S35	3541	S34 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S36	739	S35 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S37	653	@ay<"2006" and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15

S38	3	S33 and S37	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
S39	6	"6856574".did. or "5602796".did. or "20010015926".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 15:01
S40	6	"20040190035".did. or "20050052904".did. or "20040246806".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/15 21:50
S41	2	"6549480".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 09:03
S42	4392	address$3 same (clock $3) same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:28
S43	536	address$3 same (clock $3) same ((word adj line$1) or wordline$1) same (high or activat $3 or enabl$3) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:29
S44	421	@ay<"2006" and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30
S45	0	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30

S46	0	S45 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:30
S47	127	365/233.$.ccls. and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:31
S48	5238	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:32
S49	134	S48 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 08:32
S50	0	dual same bit$1 same flash same paage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35
S51	63	dual same bit$1 same flash same page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35
S52	41	S51 and simultaneous $2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:35
S53	19	S51 and "at same time"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 11:49

S54	104901	(portion or part) same memory same address $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:49
S55	104901	(portion or part) same memory same address $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:50
S56	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:51
S57	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:51
S58	100	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:54
S59	75	@ay<"2006" and S58	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 17:54
S60	462	(portion or part) same memory same address $3 same clock$3 same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13
S61	384	@ay<"2006" and S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13

S62	309	S61 not S59	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 18:13
S63	626	memory same address $3 same clock$3 same ((word adj line$1) or wordline$1) same driver$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35
S64	501	@ay<"2006" and S63	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35
S65	498	S64 not S62	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/15 21:35

1/16/2009 11:27:32 AM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED

Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt

SEARCH NOTES

Search Notes	Date	Examiner
east [see attached]	11/11/07	mt
check 2nd non-final not yet "approved"	4/22/08	mt
east	1/15/09	mt

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

	/MICHAEL T TRAN/ Primary Examiner.Art Unit 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

In response to the Non-Final Office Action mailed July 30, 2008, please reconsider the above-identified application in light of the following amendments and remarks:

CLAIM AMENDMENTS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. (Original) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. (Original) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. (Original) The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. (Original) The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. (Original) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. (Original) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

8. (Previously presented) The method of claim 7, further comprising:

receiving the clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. (Original) The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. (Original) The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. (Original) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

12. (Original) The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. (Original) The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. (Original) The circuit device of claim 12, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

15. (Original) The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. (Original) The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17. (Withdrawn) A circuit device comprising:

a group of wordline drivers, each of the wordline drivers comprising a control terminal, an address terminal, and an output terminal, the output terminal coupled to a wordline of a memory array;

an inverter including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers; and

a plurality of clock outputs, each of the plurality of clock outputs coupled to the control terminal of a respective one of the group of wordline drivers.

18. (Withdrawn) The circuit device of claim 17, further comprising logic to derive the plurality of clock outputs from a single clock.

19. (Withdrawn) The circuit device of claim 17, further comprising:

a clock generator to receive a clock signal and to selectively apply the clock signal to one of the plurality of clock outputs.

20. (Withdrawn) The circuit device of claim 19, wherein the wordline driver associated with the selected one of the plurality of clock outputs is in a dynamic evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

21. (Withdrawn) The circuit device of claim 20, wherein the static precharge state comprises a fixed voltage level.

22. (Currently amended) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate [[a]]the selected wordline driver ~~of the group of wordline drivers~~.

23. (Original) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. (Original) The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. (Original) The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26. (Withdrawn) An integrated circuit comprising:

a substrate; and

a plurality of circuit devices comprising:

a first wordline driver comprising a first transistor, a third transistor, and a first wordline output;

a second wordline driver comprising a second transistor, a fourth transistor, and a second wordline output;

wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the first wordline output and the second wordline output are disposed on the substrate in a single row;

wherein the first wire trace couples the first transistor to the third transistor and the third transistor to the first wordline output;

wherein the second wire trace couples the second transistor to the fourth transistor and the fourth transistor to the second wordline output; and

wherein the first wire trace and the second wire trace are substantially parallel.

27. (Withdrawn) The integrated circuit of claim 26, further comprising:

a first output associated with the first wire trace; and

a second output associated with the second wire trace;

wherein a voltage on the first output opposes capacitive coupling between the first wire trace and the second wire trace.

28. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

29. (Previously presented) The circuit device of claim 28, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

30. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

31. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

32. (Previously presented) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

33. (Previously presented) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

34. (Previously presented) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array;

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

35. (Previously presented) The circuit device of claim 34, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

36. (Withdrawn) A circuit device comprising:

a group of wordline drivers, each of the wordline drivers comprising a control terminal, an address terminal, and an output terminal, the output terminal coupled to a wordline of a memory array;

a clock generator to receive a clock signal and to selectively apply the clock signal to one of a plurality of clock outputs, wherein each of the plurality of clock outputs coupled to the control terminal of a respective one of the group of wordline drivers; and

an inverter including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers.

37. (Withdrawn) The circuit device of claim 36, wherein the wordline driver associated with the selected one of the plurality of clock outputs is in a dynamic evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

38. (Withdrawn) The circuit device of claim 37, wherein the static precharge state comprises a fixed voltage level.

39. (Currently amended) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and

logic comprising:

first logic to receive a clock signal and a first portion of a memory address of the memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of the plurality of clock outputs; and

second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of the plurality of clock outputs to activate [[a]]the selected wordline driver ~~of the group of wordline drivers~~.

40. (Previously presented) The circuit device of claim 39, wherein a state of the one wordline driver is determined by the selective application of the clock signal.

41. (New) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output, and wherein the first logic is further to generate multiple conditional clock outputs, wherein one of the multiple conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

42. (New) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock according to one of the first portion and the second portion of the memory address.

43. (New) The circuit device of claim 1, wherein the first logic generates a plurality of conditional clock outputs, wherein one of the plurality of conditional clock outputs is active at a time, the first logic to apply the active conditional clock output as the selected clock output.

44. (New) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input, and wherein the first logic is further to generate four conditional clock outputs, wherein one of the four conditional clock outputs is an active conditional clock output, the first logic to apply the active conditional clock output as the selected clock output.

45. (New) The method of claim 1, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

46. (New) The circuit device of claim 11, wherein each of the wordline drivers is associated with a corresponding wordline of the memory array.

47. (New) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and wherein the logic comprises a conditional clock generator.

48. (New) A circuit device comprising:

means for providing a clock signal to a selected group of wordline drivers based on a portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to another portion of the memory address.

REMARKS

Status of the Claims

Claims 22-23 and 39 are amended. Claims 17-21, 26-27, and 36-38 have been withdrawn. New claims 41-48 have been added. Claims 1-16, 22-25, 28-35, and 39-48 are pending.

Claims 1-16 and 28-35 are Allowable

The Office has indicated that claims 1-16 and 28-35 are allowable, at paragraphs 7 and 8 of the Office Action. Applicant thanks the Examiner for these allowances.

Claims 22-25 and 39-40 are Allowable

The Office has rejected claims 22-25, at paragraphs 4-5 of the Office Action, under 35 U.S.C. §102(b), as anticipated by U.S. Patent No. 6,856,574 ("Iwahashi"). Applicant respectfully traverses the rejections.

The cited portions of Iwahashi do not disclose the specific combination of claim 22. For example, the cited portions of Iwahashi do not disclose second logic to decode a second portion of a memory address, the second logic to select a particular wordline driver of a group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of a plurality of clock outputs to activate a selected wordline driver, as in claim 22. The Office admits that the cited portions of Iwahashi do not disclose second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address. *See* Office Action, paragraph 8. Therefore, the cited portions of Iwahashi do not disclose each and every element of claim 22. Hence, claim 22 is allowable.

Claims 23-25 depend from claim 22. Therefore, claims 23-25 are allowable, at least by virtue of their dependence from claim 22.

The Office has rejected claims 39-40, at paragraph 6 of the Office Action, under 35 U.S.C. §102(b), as anticipated by Iwahashi. Applicant respectfully traverses the rejections.

The cited portions of Iwahashi do not disclose the specific combination of claim 39. For example, the cited portions of Iwahashi do not disclose second logic to decode a second portion of a memory address, the second logic to select a particular wordline driver of a group of wordline drivers according to the second portion of the memory address and to selectively apply a clock signal to one of a plurality of clock outputs to activate a selected wordline driver, as in claim 39. The Office admits that Iwahashi does not disclose second logic to decode a second portion of the memory address, the second logic to select a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address. *See* Office Action, paragraph 8. Hence, claim 39 is allowable.

Claim 40 depends from claim 39. Therefore, claim 40 is allowable, at least by virtue of its dependence from claim 39.

Claims 41-48 are Allowable

Applicant has added new claims 41-48, which are supported by the Specification. No new matter has been added.

Claims 41-45 depend from claim 1, which the Office has indicated to be allowable. Therefore, claims 41-45 are allowable, at least by virtue of their dependence from claim 1.

Claim 46 depends from claim 11, which the Office has indicated to be allowable. Therefore, claims 46 is allowable, at least by virtue of its dependence from claim 11.

Claim 47 depends from claim 22, which Applicant has shown to be allowable. Therefore, claim 47 is allowable, at least by virtue of its dependence from claim 22.

Claim 48 is allowable over the cited portions of Iwahashi.

CONCLUSION

Applicant has pointed out specific features of the claims not disclosed, suggested, or rendered obvious by the references applied in the Office Action. Accordingly, Applicant respectfully requests reconsideration and withdrawal of each of the rejections, as well as an indication of the allowability of each of the pending claims.

Any changes to the claims in this amendment, which have not been specifically noted to overcome a rejection based upon the cited portions of the above-cited references, should be

considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

December 3, 2008
Date

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Electronic Patent Application Fee Transmittal

Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Nicholas John Pauley/Joann Denbow
Attorney Docket Number:	061478

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 5 months with $0 paid	1255	1	2350	2350

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**2350**

Electronic Acknowledgement Receipt	
EFS ID:	4408098
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	06-DEC-2008
Filing Date:	10-OCT-2006
Time Stamp:	22:05:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2350
RAM confirmation Number	4017
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	061478_OA_12-06-08.pdf	137389 ccc4807557c0c6d7fb92c6461f363b3fc4487283	no	15
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	30443 80684c3df375fed73a317e68431bb7837b3b9028	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	167832		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 07/30/2008
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
07/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
nanm@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Febrauary 19, 2008 through May 29, 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-16 and 28-35* is/are allowed.

6)☒ Claim(s) *22-25,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *17-21,26,27 and 36-38* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *052908*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated February 19, 2008 through May 29, 2008, claims 1-40 are active in this application.

In response to the restriction requirement, Applicant elected group one with traverse. Applicant argued that the examination of all claims is not believed to create an undue burden on the USPTO and since the subject matter among the species is not independent and distinct as required by statute. Additionally, Applicant adds that the different classifications as recited by the USPTO are not adequate grounds for restriction since the USPTO has historically examined applications containing multiple sets of claims with different classifications. However, the Examiner contends that the restriction requirements are proper for the following reasons:

- the two species are distinct – one group merely recites a driver; while the other group specifically defines a particular driver. See definition of the two cited classes and subclasses.
- It is a burden to look for two distinct features in two different subclasses as there are thousands of prior art to consider.
- This office action is prepared for the purposes of examining this case, and only this case. Therefore, the argument of examined cases with multiple sets of claims classified in different classifications is irrelevant.

Specification

2. If there are cross-reference to related applications, please include the

respective patent numbers, if known.

Information Disclosure Statement

3. The information disclosure statements filed May 29, 2008 have been considered.

Claim Rejections- 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C.

102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 22-25 are rejected under 35 U.S.C 102(b) as being anticipated by

Iwahashi et al. [U.S. Patent 6,856,574].

With respect to claim 22, Iwahashi et al. disclose, in figures 1 and 2, a circuit device comprising: an address input [via 41s]; a plurality of clock outputs [via 111s]; a group of wordline drivers [42] coupled to a wordline of a memory array [see figure 2], each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and logic [32/33] to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

With respect to claim 23, Iwahashi et al. disclose, in figures 1 and 2, the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state. This depends on the selective process of the device.

With respect to claim 24, Iwahashi et al. disclose, in figures 1 and 2, a state of the wordline driver is determined by the selective application of the clock signal. This depends on the selective process of the device.

With respect to claim 25, Iwahashi et al. disclose, in figures 1 and 2, the logic comprises a conditional clock generator. The generator is dependent upon the PWRP signals.

6. Claims 39 and 40 are rejected under 35 U.S.C 102(b) as being anticipated by Iwahashi et al. [U.S. Patent 6,856,574].

With respect to claim 39, Iwahashi et al. disclose, in figures 1 and 2, a circuit device comprising: an address input; a plurality of clock outputs; a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

With respect to claim 40, Iwahashi et al. disclose, in figures 1 and 2, a state of the one wordline driver is determined by the selective application of the clock signal. This depends on the selective process of the device.

Allowable Subject Matter

7. Claims 1-16 and 28-35 are allowable over the prior art of record.

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. .Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. .Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
July 28, 2008

PTO/SB/08a (03-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11548132
Filing Date	2006-10-10
First Named Inventor	Jentsung Lin
Art Unit	2827
Examiner Name	Tran, Michael Thanh
Attorney Docket Number	061478

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040190035		2004-09-30	Watanabe, Naoya	
	2	20050052904		2005-03-10	Cho, Beak-Hung	
	3	20040246806		2004-12-09	Ha, Chang Wan	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MT/

Receipt date: 05/29/2008

11548132 - GAU: 2827

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11548132
Filing Date	2006-10-10
First Named Inventor	Jentsung Lin
Art Unit	2827
Examiner Name	Tran, Michael Thanh
Attorney Docket Number	061478

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Michael Tran/	Date Considered	07/25/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MT/

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008							
	1	✓	=							
	2	O	=							
	3	O	=							
	4	✓	=							
	5	O	=							
	6	O	=							
	7	✓	=							
	8	✓	=							
	9	✓	=							
	10	O	=							
	11	✓	=							
	12	✓	=							
	13	O	=							
	14	O	=							
	15	✓	=							
	16	✓	=							
	17	✓	N							
	18	✓	N							
	19	O	N							
	20	O	N							
	21	O	N							
	22	✓	✓							
	23	O	✓							
	24	O	✓							
	25	✓	✓							
	26		N							
	27		N							
	28		=							
	29		=							
	30		=							
	31		=							
	32		=							
	33		=							
	34		=							
	35		=							
	36		N							

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CLAIM		DATE								
Final	Original	11/12/2007	07/25/2008							
	37		N							
	38		N							
	39		✓							
	40		✓							

Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11548132
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	First Named Inventor	Jentsung Lin
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	Examiner Name	Tran, Michael Thanh
	Attorney Docket Number	061478

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040190035		2004-09-30	Watanabe, Naoya	
	2	20050052904		2005-03-10	Cho, Beak-Hung	
	3	20040246806		2004-12-09	Ha, Chang Wan	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

EFS Web 2.1.1

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	Filing Date	2006-10-10
	First Named Inventor	Jentsung Lin
	Art Unit	2827
	Examiner Name	Tran, Michael Thanh
	Attorney Docket Number	061478

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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐
If you wish to add additional non-patent literature document citation information please click the Add button			Add

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

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	First Named Inventor	Jentsung Lin
	Art Unit	2827
	Examiner Name	Tran, Michael Thanh
	Attorney Docket Number	061478

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Nicholas J. Pauley/	Date (YYYY-MM-DD)	2008-05-27
Name/Print	Nicholas J. Pauley	Registration Number	44,999

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	3371453
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Joseph B. Agusta/Joann Denbow
Filer Authorized By:	Joseph B. Agusta
Attorney Docket Number:	061478
Receipt Date:	29-MAY-2008
Filing Date:	10-OCT-2006
Time Stamp:	09:35:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	061478_IDS_PTOSB08_05-19-08.pdf	574226 a85a4a82ac4b98720e58cbf022e162cab3b17295	no	4
Warnings:					
Information:					

Total Files Size (in bytes):	574226

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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Electronic Acknowledgement Receipt

EFS ID:	3329275
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Joseph B. Agusta/Joann Denbow
Filer Authorized By:	Joseph B. Agusta
Attorney Docket Number:	061478
Receipt Date:	20-MAY-2008
Filing Date:	10-OCT-2006
Time Stamp:	14:02:54
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	061478_RR_05-20-08.pdf	355384 0f5818aa69a43614d641a454b1ca206f72d496c4	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	355384

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Dear Sir:

The USPTO has restricted claims 1-40 of this application into Species I (claims 1-16, 22-25, 28-35, 39 and 40) and Species II (claims 17-21, 26, 27, 36-38).

Applicant elects the claims of Species I (claims 1-16, 22-25, 28-35, 39 and 40) and provisionally withdraws the non-elected claims of Species II (claims 17-21, 26, 27, 36-38). The restriction is respectfully traversed in order to preserve the issue for subsequent petition since the examination of all of the claims is not believed to create an undue burden on the USPTO and since the subject matter among the species is not independent and distinct as required by statute. Furthermore, different classifications as recited by the USPTO are not adequate grounds for restriction since the USPTO has historically examined applications containing multiple sets of claims with different classifications.

Applicant traverses the restriction, and believes that subject matter of Species I and II can be used together. For example, claim 7 of Species I includes a method of selecting a particular wordline of a memory array that includes activating a particular wordline driver of a selected group of wordline drivers. Claim 17 of Species II includes a circuit device that includes a group of wordline drivers. Applicant submits that the subject matter in Species I and Species II can be used together compatibly.

In summary, Applicant elects the claims of Species I for further prosecution and provisionally withdraws the non-elected claims from consideration. Reconsideration and further prosecution on the merits of at least the claims of Species I are respectfully requested.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

Date: May 19, 2008

Nicholas J. Pauley, Reg. No. 44,999
QUALCOMM Incorporated
Attn: Patent Department
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San Diego, California 92121-1714
Telephone: (858) 658-5787
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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 04/28/2008
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
04/28/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
nanm@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-40* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated February 19, 2008, claims 1-40 are active in this application.

Election of Species

2. A telephone call was made to Nicholas Pauley to request an oral election to the below restriction requirement, but did not result in an election being made.

3. This application contains claims directed to the following patentably distinct species of the claimed invention: 1) Addressing [claims 1-16, 22-25, 28-35, 39 and 40; classified in class 365, subclass 230.01]; and 2) Particular Driver [claims 17-21, 26, 27 and 36-38; classified in class 365, subclass 230.06]. These species reflect figures 1 and 3 of the present application.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a response to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to

consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

Conclusion

4. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

5. A shortened statutory period for response to this Office action is set to

expire 30 days from the date of this communication. Failure to response within the period for response will cause the application to become abandoned (see MPEP § 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

7. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1950.

/Michael T. Tran/
Michael T. Tran
Primary Examiner
Art Unit 2827
April 24, 2008

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED			
Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt

SEARCH NOTES		
Search Notes	Date	Examiner
east [see attached]	11/11/07	mt
check 2nd non-final not yet "approved"	4/22/08	mt

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	6	"20020166028".did. or "6233191".did. or "4365319".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:14
L6	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
L7	3541	L6 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
L8	739	L7 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
L9	653	@ay<"2006" and L8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
L10	3	5 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 14:15
L11	6	"6856574".did. or "5602796".did. or "20010015926".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/23 15:01

S1	0	Lin-Jentsung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:06
S2	83	clock same (partical or portion) same address same driver same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:07
S3	71	@ay<"2006" and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S4	17745	column same row same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:39
S5	2195	column same row same driver same clock	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S6	287	column same row same driver same clock same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S7	258	@ay<"2006" and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:16
S8	10867	address$2 same driver same (share or "same")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19

S9	8974	@ay<"2006" and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S10	1691	S9 and (driver same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:20
S11	726	S10 and (address$2 same clock$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:21
S12	240	S11 and (clock same generator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:08
S13	6	"5459684".did. or "6856574".did. or "5596539".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:39
S14	525	select$5 same clock same ((word adj line $1) or wordline$1) same driver same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S15	466	@ay<"2006" and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S16	296	S15 and ((activat$3 or enabl$3) same driver same address$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 11:42

S17	114	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2 same invert$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S18	99	@ay<"2006" and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S19	706	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S20	27	S19 and driver$1.ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:06
S21	685	clock same ((word adj line$1) or wordline$1) same driver$1 same address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S22	614	@ay<"2006" and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S23	4037	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S24	109	S23 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18

S25	4306	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S26	97	S25 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S27	33961	address$3 same (portion$1 or segment $1 or part$1) same driv $3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:41
S28	3541	S27 and (address$3 same ((word adj line $1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:42
S29	739	S28 and (address$3 same clock$3 same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:44
S30	653	@ay<"2006" and S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 11:45
S31	63	(first adj fuse) same (second adj fuse) same compar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:01
S32	2	"6728158".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/22 14:23

4/23/2008 5:52:45 PM
C:\Documents and Settings\mtran1\My Documents\EAST\Workspaces\11548132.wsp

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/548,132	10/10/2006	Jentsung Lin	061478

CONFIRMATION NO. 4884

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA92121

Title: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

Publication No. US-2008-0084778-A1
Publication Date: 04/10/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Jentsung Lin		
Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
App. No.:	11/548,132	Filed:	October 10, 2006
Examiner:	TRAN, Michael Thanh	Group Art Unit:	2827
Customer No.:	23696	Confirmation No.:	4884
Atty. Dkt. No.:	061478		

M/S: Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

In response to the Non-Final Office Action mailed November 19, 2007, please reconsider the above-identified application in light of the following amendments and remarks:

CLAIM AMENDMENTS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. (Original) The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. (Original) The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. (Original) The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. (Original) The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. (Original) The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. (Original) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

8. (Currently Amended) The method of claim 7, further comprising:

receiving [[a]] the clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. (Original) The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. (Original) The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. (Original) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

12. (Original) The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. (Original) The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. (Original) The circuit device of claim 12, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

15. (Original) The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. (Original) The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17. (Original) A circuit device comprising:

a group of wordline drivers, each of the wordline drivers comprising a control terminal, an address terminal, and an output terminal, the output terminal coupled to a wordline of a memory array;

an inverter including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers; and

a plurality of clock outputs, each of the plurality of clock outputs coupled to the control terminal of a respective one of the group of wordline drivers.

18. (Original) The circuit device of claim 17, further comprising logic to derive the plurality of clock outputs from a single clock.

19. (Original) The circuit device of claim 17, further comprising:

a clock generator to receive a clock signal and to selectively apply the clock signal to one of the plurality of clock outputs.

20. (Original) The circuit device of claim 19, wherein the wordline driver associated with the selected one of the plurality of clock outputs is in a dynamic evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

21. (Currently amended) The circuit device of claim 20, wherein the ~~state~~ static precharge state comprises a fixed voltage level.

22. (Original) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

23. (Original) The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. (Original) The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. (Original) The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26. (Original) An integrated circuit comprising:

a substrate; and

a plurality of circuit devices comprising:

a first wordline driver comprising a first transistor, a third transistor, and a first wordline output;

a second wordline driver comprising a second transistor, a fourth transistor, and a second wordline output;

wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the first wordline output and the second wordline output are disposed on the substrate in a single row;

wherein the first wire trace couples the first transistor to the third transistor and the third transistor to the first wordline output;

wherein the second wire trace couples the second transistor to the fourth transistor and the fourth transistor to the second wordline output; and

wherein the first wire trace and the second wire trace are substantially parallel.

27. (Original) The integrated circuit of claim 26, further comprising:

a first output associated with the first wire trace; and

a second output associated with the second wire trace;

wherein a voltage on the first output opposes capacitive coupling between the first wire trace and the second wire trace.

28. (New) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

29. (New) The circuit device of claim 28, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

30. (New) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

31. (New) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

32. (New) A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

33. (New) A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

34. (New) A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array, wherein each of the wordline drivers is associated with a wordline of the memory array;

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive the clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

35. (New) The circuit device of claim 34, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

36. (New) A circuit device comprising:

a group of wordline drivers, each of the wordline drivers comprising a control terminal, an address terminal, and an output terminal, the output terminal coupled to a wordline of a memory array;

a clock generator to receive a clock signal and to selectively apply the clock signal to one of a plurality of clock outputs, wherein each of the plurality of clock outputs coupled to the control terminal of a respective one of the group of wordline drivers; and

an inverter including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers.

37. (New) The circuit device of claim 36, wherein the wordline driver associated with the selected one of the plurality of clock outputs is in a dynamic evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

38. (New) The circuit device of claim 37, wherein the static precharge state comprises a fixed voltage level.

39. (New) A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state; and

logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

40. (New) The circuit device of claim 39, wherein a state of the one wordline driver is determined by the selective application of the clock signal.

REMARKS

New claims 28-40 have been added. Support for the new claims can be found in at least paragraphs [0004]-[0008], [0016]-[0018], [0028]-[0030] and [0043]-[0046] of the application.

I. Claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 And 24 Are Allowable

The Office has objected to claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 as being dependent upon a rejected base claim at paragraph 2, of the Office Action, but states that the claims would be allowable if rewritten in independent form including all limitations of the respective base claim and any intervening claims. Accordingly, Applicants have rewritten the above-identified claims as new claims 28-40 based on the allowable subject matter indicated by the Office Action. In addition, Applicants respectfully traverse the rejections of the original claims as explained below.

II. Claims 1-6 Are Allowable

The Office has rejected claims 1 and 4, at paragraph 4 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claims 2, 3, 5 and 6 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

It is axiomatic that anticipation of a claim under 35 U.S.C. §102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). Here, the cited portions of the reference, Iwashi, does not anticipate claim 1 because the cited portions of Iwashi do not teach every element of claim 1. For example, the cited portions of Iwashi do not teach first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. The Office asserts that this feature is taught by Figure 1 of Iwashi.

However, in contrast to claim 1, Iwashi discloses a semiconductor memory device having a group of read word decoders/drivers (12) and a group of read column decoders/drivers (13). *See* Iwashi, column 8, lines 28-31. The read word decoders/drivers (12) include a read word decoder for decoding signals and a read word driver for driving a word line on the basis of a decoding result generated by the read word decoder. A first clock signal "ckxr" is provided to the group of the read word drivers. *See* Iwashi, column 8, lines 44-47; Figure 1. The read column decoders/drivers (13) include a read column decoder for decoding signals and a read column driver for driving a read column select circuit, which is employed in the read/write unit, on the basis of a decoding result generated by the read column decoder. Clock signal "ckyr" is provided to the group of read column drivers. *See* Iwashi, column 8, lines 53-55, Figure 1.

The Office Action states that the read address buffer (11) of Iwashi anticipates a first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and a second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 1, Iwashi does not output signals to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not decode a second portion of a memory address to activate a particular wordline driver of the selected group of drivers, as in claim 1. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach a first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and a second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. Thus, Iwashi does not teach every element of claim 1. Therefore, claim 1 is allowable. Claims 2-6 depend from claim 1, which Applicants have shown to be allowable. Accordingly, claims 2-6 are also allowable.

III. Claims 7-10 Are Allowable

The Office has rejected claims 7-9, at paragraph 5 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claim 10 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Iwashi do not anticipate claim 7 because Iwashi does not teach every element of claim 7. For example, the cited portions of Iwashi do not teach selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 7. The Office asserts that this feature is taught by Figure 1 of Iwashi.

The Office Action states that Iwashi anticipates selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers, as in claim 7. However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 7, the cited portions of Iwashi do not provide a clock signal to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not activate a particular wordline driver of the selected group of drivers according to a second portion of a memory address, as in claim 7. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 7. Thus, Iwashi does not teach every element of claim 7. Therefore, claim 7 is allowable. Claims 8-10 depend from claim 7, which Applicants have shown to be allowable. Accordingly, claims 8-10 are also allowable.

IV. Claims 11-16 Are Allowable

The Office has rejected claims 11, 12, 15 and 16, at paragraph 6 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claim 13 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Iwashi do not anticipate claim 11 because Iwashi does not teach every element of claim 11. For example, the cited portions of Iwashi do not teach means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 11. The Office asserts that this feature is taught by Figure 1 of Iwashi.

However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 11, the cited portions of Iwashi do not disclose means for selectively providing a clock signal to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not activate a particular wordline driver of the selected group of drivers according to a second portion of a memory address, as in claim 11. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 11. Thus, Iwashi does not teach every element of claim 11. Therefore, claim 11 is allowable. Claims 12-16 depend from claim 11, which Applicants have shown to be allowable. Accordingly, claims 12-16 are also allowable.

V. Claims 17-21 Are Allowable

The Office has rejected claims 17 and 18, at paragraph 7 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 5,602,796 ("Sugio"). The Office has

objected to claims 19-21 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Sugio do not anticipate claim 17 because Sugio does not teach every element of claim 17. For example, the cited portions of Sugio do not teach a group of wordline drivers wherein each of the wordline drivers comprise a control terminal and a plurality of clock outputs, where each of the plurality of clock outputs is coupled to the control terminal of a respective one of the group of wordline drivers, as recited in claim 17. The Office asserts that this feature is taught by Figures 1-4 of Sugio.

In contrast to claim 17, Sugio discloses that a timing control circuit outputs the control signals for controlling the timings provided for the respective components based on the control signal and clock. *See* Sugio, column 3, lines 58-61. Thus, with Sugio, the clock signal (CK) is used to drive all the wordline drivers. Accordingly, Sugio does not teach a group of wordline drivers wherein each of the wordline drivers comprise a control terminal and a plurality of clock outputs, and where each of the plurality of clock outputs is coupled to the control terminal of a respective one of the group of wordline drivers, as recited in claim 17. By applying the clock signal to the selected clock output as in claim 17, power consumption is reduced, since the clock drives a single line of a group of wordline drivers, as opposed to driving all of the wordline drivers. Thus, Sugio does not teach every element of claim 17. Therefore, claim 17 is allowable. Claims 18-21 depend from claim 17, which Applicants have shown to be allowable. Accordingly, claims 18-21 are also allowable.

VI. Claims 22-25 Are Allowable

The Office has rejected claims 22 and 25, at paragraph 8 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent Application Publication No. 2001/0015926 ("Kato"). The Office has objected to claims 23 and 24 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Kato do not anticipate claim 22 because Kato does not teach every element of claim 22. For example, the cited portions of Kato do not teach a circuit device

including a group of wordline drivers wherein each of the wordline drivers is coupled to a respective clock output of a plurality of clock outputs and logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers, as recited in claim 22. The Office asserts that this feature is taught by Figures 1-6 of Kato.

In contrast to claim 22, Kato discloses a semiconductor memory device having a burn-in test control circuit for providing a stress voltage to a plurality of wordlines and pairs of bit lines to perform a burn-in test based on a burn-in control signal. *See* Kato, Abstract. During the burn-in test, a word decoder driver simultaneously selects all of the wordlines based on the burn-in control signal. *See* Kato, paragraph [0054]. Accordingly, Kato does not teach a circuit device including a group of wordline drivers wherein each of the wordline drivers is coupled to a respective clock output of a plurality of clock outputs and logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers, as in claim 22. By applying the clock signal to the selected clock output to activate a selected wordline driver, as in claim 22, power consumption is reduced, since the clock drives a single line of a group of wordline drivers, as opposed to driving all of the wordline drivers. Thus, Kato does not teach every element of claim 22. Therefore, claim 22 is allowable. Claims 23-25 depend from claim 22, which Applicants have shown to be allowable. Accordingly, claims 23-25 are also allowable.

VII. Claims 26 And 27 Are Allowable

The Office apparently has not examined claims 26 and 27, submitted with the original application. The Office Action does not address claims 26 and 27. The cited portions of Iwashi, Sugio and Kato, fail to disclose or suggest the specific combination of claim 26. For example, the cited portions of Iwashi, Sugio and Kato do not disclose a first transistor, a second transistor, a third transistor, a fourth transistor, a first wordline output, and a second wordline output disposed on a substrate in a single row, as recited in claim 26. Hence, claim 26 is allowable. Claim 27 depends from claim 26, which Applicants have shown to be allowable. Accordingly, claim 27 is also allowable, at least by virtue of its dependency from claim 26.

VIII. Claims 28-40 Are Allowable

New claims 28-40 have been added. Support for the new claims can be found in at least paragraphs [0004]-[0008], [0016]-[0018], [0028]-[0030] and [0043]-[0046] of the application. The Office Action states that claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Accordingly, claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 have been rewritten as new claims 28-40. Hence, claims 28-40 are allowable.

CONCLUSION

Applicants have pointed out specific features of the claims not disclosed, suggested, or rendered obvious by the references applied in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of each of the rejections, as well as an indication of the allowability of each of the pending claims.

Any changes to the claims in this amendment, which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

_____2/15/08_____
Date

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REMARKS

New claims 28-40 have been added. Support for the new claims can be found in at least paragraphs [0004]-[0008], [0016]-[0018], [0028]-[0030] and [0043]-[0046] of the application.

I. Claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 And 24 Are Allowable

The Office has objected to claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 as being dependent upon a rejected base claim at paragraph 2, of the Office Action, but states that the claims would be allowable if rewritten in independent form including all limitations of the respective base claim and any intervening claims. Accordingly, Applicants have rewritten the above-identified claims as new claims 28-40 based on the allowable subject matter indicated by the Office Action. In addition, Applicants respectfully traverse the rejections of the original claims as explained below.

II. Claims 1-6 Are Allowable

The Office has rejected claims 1 and 4, at paragraph 4 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claims 2, 3, 5 and 6 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

It is axiomatic that anticipation of a claim under 35 U.S.C. §102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). Here, the cited portions of the reference, Iwashi, does not anticipate claim 1 because the cited portions of Iwashi do not teach every element of claim 1. For example, the cited portions of Iwashi do not teach first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. The Office asserts that this feature is taught by Figure 1 of Iwashi.

However, in contrast to claim 1, Iwashi discloses a semiconductor memory device having a group of read word decoders/drivers (12) and a group of read column decoders/drivers (13). *See* Iwashi, column 8, lines 28-31. The read word decoders/drivers (12) include a read word decoder for decoding signals and a read word driver for driving a word line on the basis of a decoding result generated by the read word decoder. A first clock signal "ckxr" is provided to the group of the read word drivers. *See* Iwashi, column 8, lines 44-47; Figure 1. The read column decoders/drivers (13) include a read column decoder for decoding signals and a read column driver for driving a read column select circuit, which is employed in the read/write unit, on the basis of a decoding result generated by the read column decoder. Clock signal "ckyr" is provided to the group of read column drivers. *See* Iwashi, column 8, lines 53-55, Figure 1.

The Office Action states that the read address buffer (11) of Iwashi anticipates a first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and a second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 1, Iwashi does not output signals to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not decode a second portion of a memory address to activate a particular wordline driver of the selected group of drivers, as in claim 1. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach a first logic to apply a clock signal to a plurality of clock outputs associated with a selected group of a plurality of wordline drivers and a second logic to selectively activate a particular wordline driver of the selected group of wordline drivers, as in claim 1. Thus, Iwashi does not teach every element of claim 1. Therefore, claim 1 is allowable. Claims 2-6 depend from claim 1, which Applicants have shown to be allowable. Accordingly, claims 2-6 are also allowable.

III. Claims 7-10 Are Allowable

The Office has rejected claims 7-9, at paragraph 5 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claim 10 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Iwashi do not anticipate claim 7 because Iwashi does not teach every element of claim 7. For example, the cited portions of Iwashi do not teach selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 7. The Office asserts that this feature is taught by Figure 1 of Iwashi.

The Office Action states that Iwashi anticipates selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers, as in claim 7. However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 7, the cited portions of Iwashi do not provide a clock signal to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not activate a particular wordline driver of the selected group of drivers according to a second portion of a memory address, as in claim 7. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 7. Thus, Iwashi does not teach every element of claim 7. Therefore, claim 7 is allowable. Claims 8-10 depend from claim 7, which Applicants have shown to be allowable. Accordingly, claims 8-10 are also allowable.

IV. Claims 11-16 Are Allowable

The Office has rejected claims 11, 12, 15 and 16, at paragraph 6 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 6,856,574 ("Iwashi"). The Office has objected to claim 13 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Iwashi do not anticipate claim 11 because Iwashi does not teach every element of claim 11. For example, the cited portions of Iwashi do not teach means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 11. The Office asserts that this feature is taught by Figure 1 of Iwashi.

However, with Iwashi, the read address buffer (11) outputs signals to all the read word drivers and read column drivers. In contrast with claim 11, the cited portions of Iwashi do not disclose means for selectively providing a clock signal to a selected group of the read word drivers and read column drivers. *See* Iwashi, column 8, lines 35-38. Further, the read word and read column decoders of Iwashi do not activate a particular wordline driver of the selected group of drivers according to a second portion of a memory address, as in claim 11. Instead, Iwashi discloses that each driver has its own decoded address input placing a large load on the decoder. *See* Iwashi, column 18, lines 39-44 and 57-62. Accordingly, Iwashi does not teach means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array and means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address, as in claim 11. Thus, Iwashi does not teach every element of claim 11. Therefore, claim 11 is allowable. Claims 12-16 depend from claim 11, which Applicants have shown to be allowable. Accordingly, claims 12-16 are also allowable.

V. Claims 17-21 Are Allowable

The Office has rejected claims 17 and 18, at paragraph 7 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent No. 5,602,796 ("Sugio"). The Office has

objected to claims 19-21 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Sugio do not anticipate claim 17 because Sugio does not teach every element of claim 17. For example, the cited portions of Sugio do not teach a group of wordline drivers wherein each of the wordline drivers comprise a control terminal and a plurality of clock outputs, where each of the plurality of clock outputs is coupled to the control terminal of a respective one of the group of wordline drivers, as recited in claim 17. The Office asserts that this feature is taught by Figures 1-4 of Sugio.

In contrast to claim 17, Sugio discloses that a timing control circuit outputs the control signals for controlling the timings provided for the respective components based on the control signal and clock. *See* Sugio, column 3, lines 58-61. Thus, with Sugio, the clock signal (CK) is used to drive all the wordline drivers. Accordingly, Sugio does not teach a group of wordline drivers wherein each of the wordline drivers comprise a control terminal and a plurality of clock outputs, and where each of the plurality of clock outputs is coupled to the control terminal of a respective one of the group of wordline drivers, as recited in claim 17. By applying the clock signal to the selected clock output as in claim 17, power consumption is reduced, since the clock drives a single line of a group of wordline drivers, as opposed to driving all of the wordline drivers. Thus, Sugio does not teach every element of claim 17. Therefore, claim 17 is allowable. Claims 18-21 depend from claim 17, which Applicants have shown to be allowable. Accordingly, claims 18-21 are also allowable.

VI. Claims 22-25 Are Allowable

The Office has rejected claims 22 and 25, at paragraph 8 of the Office Action, under 35 U.S.C. §102(b), as being unpatentable over U.S. Patent Application Publication No. 2001/0015926 ("Kato"). The Office has objected to claims 23 and 24 as being dependent on a rejected base claim. Applicants respectfully traverse the rejections.

The cited portions of Kato do not anticipate claim 22 because Kato does not teach every element of claim 22. For example, the cited portions of Kato do not teach a circuit device

including a group of wordline drivers wherein each of the wordline drivers is coupled to a respective clock output of a plurality of clock outputs and logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers, as recited in claim 22. The Office asserts that this feature is taught by Figures 1-6 of Kato.

In contrast to claim 22, Kato discloses a semiconductor memory device having a burn-in test control circuit for providing a stress voltage to a plurality of wordlines and pairs of bit lines to perform a burn-in test based on a burn-in control signal. *See* Kato, Abstract. During the burn-in test, a word decoder driver simultaneously selects all of the wordlines based on the burn-in control signal. *See* Kato, paragraph [0054]. Accordingly, Kato does not teach a circuit device including a group of wordline drivers wherein each of the wordline drivers is coupled to a respective clock output of a plurality of clock outputs and logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers, as in claim 22. By applying the clock signal to the selected clock output to activate a selected wordline driver, as in claim 22, power consumption is reduced, since the clock drives a single line of a group of wordline drivers, as opposed to driving all of the wordline drivers. Thus, Kato does not teach every element of claim 22. Therefore, claim 22 is allowable. Claims 23-25 depend from claim 22, which Applicants have shown to be allowable. Accordingly, claims 23-25 are also allowable.

VII. Claims 26 And 27 Are Allowable

The Office apparently has not examined claims 26 and 27, submitted with the original application. The Office Action does not address claims 26 and 27. The cited portions of Iwashi, Sugio and Kato, fail to disclose or suggest the specific combination of claim 26. For example, the cited portions of Iwashi, Sugio and Kato do not disclose a first transistor, a second transistor, a third transistor, a fourth transistor, a first wordline output, and a second wordline output disposed on a substrate in a single row, as recited in claim 26. Hence, claim 26 is allowable. Claim 27 depends from claim 26, which Applicants have shown to be allowable. Accordingly, claim 27 is also allowable, at least by virtue of its dependency from claim 26.

VIII. Claims 28-40 Are Allowable

New claims 28-40 have been added. Support for the new claims can be found in at least paragraphs [0004]-[0008], [0016]-[0018], [0028]-[0030] and [0043]-[0046] of the application. The Office Action states that claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Accordingly, claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 have been rewritten as new claims 28-40. Hence, claims 28-40 are allowable.

CONCLUSION

Applicants have pointed out specific features of the claims not disclosed, suggested, or rendered obvious by the references applied in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of each of the rejections, as well as an indication of the allowability of each of the pending claims.

Any changes to the claims in this amendment, which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 17-0026.

Respectfully submitted,

_____2/15/08_____
Date

_____/Nicholas j. Pauley/_____
Nicholas J. Pauley, Reg. No. 44,999
QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502

Electronic Patent Application Fee Transmittal

Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Nicholas John Pauley/Joann Denbow
Attorney Docket Number:	061478
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	13	50	650
Independent claims in excess of 3	1201	8	210	1680
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2330**

Electronic Acknowledgement Receipt	
EFS ID:	2876013
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Nicholas John Pauley/Joann Denbow
Filer Authorized By:	Nicholas John Pauley
Attorney Docket Number:	061478
Receipt Date:	19-FEB-2008
Filing Date:	10-OCT-2006
Time Stamp:	12:19:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2330
RAM confirmation Number	10619
Deposit Account	170026
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment - After Non-Final Rejection	061478_ROA_02-14-08.pdf	140286 f7b9d97e62b78332d4b3185a1ffcbe3393814aaa	no	20
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8313 801eaca085159bcdf8951c2a7fe70e80ea8f470e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	148599		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/548,132	10/10/2006	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	02/19/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 40	Minus	** 27	= 13	X $ =		OR	X $50=	650
	Independent (37 CFR 1.16(h))	* 14	Minus	***6	= 8	X $ =		OR	X $210=	1680
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	2330

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DIANIECE M. JACOBS/

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/548,132	10/10/2006	Jentsung Lin	061478	4884

23696 7590 11/19/2007
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

NOTIFICATION DATE	DELIVERY MODE
11/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
nanm@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	11/548,132	LIN, JENTSUNG	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 10, 2006 through May 1, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-9,11,12,15-18,22 and 25* is/are rejected.

7)☒ Claim(s) *2,3,5,6,10,13,14,19-21,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
AU 2827

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated October 10, 2006 through May 1, 2007, claims 1-25 are active in this application.

Claim Objections

2. Claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Is "a clock signal" in claim 7 and claim 8 the same?

Claim Rejections- 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1 and 4 are rejected under 35 U.S.C 102(b) as being anticipated by Iwahashi et al. [U.S. Patent #6,856,574].

With respect to claim 1, Iwahashi et al. disclose, in figure 1, a circuit device comprising: first logic [one of 11] to receive a clock signal [via 185] and a first portion of a memory address of a memory array [address input of one of 11], the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers [12 and 13] that are associated with the memory array [182]; and second logic [another of 11] to decode a second portion of the memory address [address inputs of 11], the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers [12 and 13] according to the second portion of the memory address.

With respect to claim 4, Iwahashi et al. disclose, in figure 1, the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. Claims 7-9 are rejected under 35 U.S.C 102(b) as being anticipated by Iwahashi et al. [U.S. Patent #6,856,574].

With respect to claim 7, Iwahashi et al. disclose, in figure 1, a method of selecting a particular wordline of a memory array, the method comprising: selectively providing a clock signal [via 185 and any of the 11] to a selected group of a plurality of wordline

drivers [12 and 13] based on a first portion of a memory address of the memory array [the addresses of any of the 11], wherein each of the plurality of wordline drivers is associated with a wordline of the memory array [182]; and activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address [addresses of any of the other 11].

With respect to claim 8, Iwahashi et al. disclose, in figure 1, receiving a clock signal [via 185]; selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address [Any of the 11].

With respect to claim 9, Iwahashi et al. disclose, in figure 1, determining a clock output [via 185] according to the first portion of the memory address using a conditional clock generator.

6. Claims 11, 12, 15 and 16 are rejected under 35 U.S.C 102(b) as being anticipated by Iwahashi et al. [U.S. Patent #6,856,574].

With respect to claim 11, Iwahashi et al. disclose, in figure 1, a circuit device comprising: means for selectively providing a clock signal [185 via 11 with respective addresses] to a selected group of wordline drivers [12 and 13] based on a first portion of a memory address of a memory array [addresses of any 11]; and means [185 with any other 11 with respective addresses] for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

With respect to claim 12, Iwahashi et al. disclose, in figure 1, that each of the wordline drivers is associated with a wordline of the memory array.

With respect to claim 15, Iwahashi et al. disclose, in figure 1, the circuit comprises an integrated circuit [any of the other elements].

With respect to claim 16, Iwahashi et al. disclose, in figure 1, the integrated circuit includes the memory array [182].

7. Claims 17 and 18 are rejected under 35 U.S.C 102(b) as being anticipated by Sugio [U.S. Patent #5,602,796].

With respect to claim 17, Sugio discloses, in figures 1-4, a circuit device comprising: a group of wordline drivers [see figure 4], each of the wordline drivers comprising a control terminal [Pwi], an address terminal [n41-1], and an output terminal [coupled to respective wordline – wl], the output terminal coupled to a wordline of a memory array [wl]; an inverter [41-1] including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers; and a plurality of clock outputs [via 1], each of the plurality of clock and outputs coupled to the control terminal of a respective one of the group of wordline drivers [1 is indirectly connected to 4, 5 and 6] .

With respect to claim 18, Sugio discloses, in figures 1-4, logic [1] to derive the plurality of clock outputs from a single clock [ck].

8. Claims 22 and 25 are rejected under 35 U.S.C 102(b) as being anticipated by Kato et al. [U.S. Patent Application #20010015926].

With respect to claim 22, Kato et al. disclose, in figures 1-6, a circuit device comprising: an address input [add]; a plurality of clock outputs [via 9]; a group of wordline drivers [3] coupled to a wordline of a memory array [dwl], each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and logic [9] to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

With respect to claim 25, Kato et al. disclose, in figure 1, the logic comprises a conditional clock generator.

Allowable Subject Matter

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.
- the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

- the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.
- a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.
- a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.
- a clock generator to receive a clock signal and to selectively apply the clock signal to one of the plurality of clock outputs.
- the selected wordline driver of the group ofwordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. Any inquiry of a general nature or relating to the status of this application.

should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
November 12, 2007

Notice of References Cited	Application/Control No. 11/548,132	Applicant(s)/Patent Under Reexamination LIN, JENTSUNG	
	Examiner MICHAEL T. TRAN	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2001/0015926	08-2001	Kato et al.	365/201
*	B	US-5,602,796	02-1997	Sugio, Kenichiro	365/230.06
*	C	US-5,051,959	09-1991	Nakano et al.	365/230.06
*	D	US-6,856,574	02-2005	Iwahashi et al.	365/233
*	E	US-5,596,539	01-1997	Passow et al.	365/210
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

SEARCHED

Class	Subclass	Date	Examiner
365	230.06	11/11/07	mt
365	233	11/11/07	mt

SEARCH NOTES

Search Notes	Date	Examiner
east [see attached]	11/11/07	mt

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11548132	LIN, JENTSUNG
	Examiner	Art Unit
	TRAN, MICHAEL T	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2007								
	1	✓								
	2	O								
	3	O								
	4	✓								
	5	O								
	6	O								
	7	✓								
	8	✓								
	9	✓								
	10	O								
	11	✓								
	12	✓								
	13	O								
	14	O								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	O								
	20	O								
	21	O								
	22	✓								
	23	O								
	24	O								
	25	✓								

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	Lin-Jentsung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:06
S2	83	clock same (partical or portion) same address same driver same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:07
S3	71	@ay<"2006" and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S4	17745	column same row same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:39
S5	2195	column same row same driver same clock	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S6	287	column same row same driver same clock same ((word adj line$1) or wordline$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 17:40
S7	258	@ay<"2006" and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:16

EAST Search History

S8	10867	address$2 same driver same (share or "same")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S9	8974	@ay<"2006" and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:19
S10	1691	S9 and (driver same ((word adj line$1) or wordline$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:20
S11	726	S10 and (address$2 same clock$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/11 20:21
S12	240	S11 and (clock same generator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:08
S13	6	"5459684".did. or "6856574".did. or "5596539".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:39
S14	525	select$5 same clock same ((word adj line$1) or wordline$1) same driver same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40

EAST Search History

S15	466	@ay<"2006" and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 08:40
S16	296	S15 and ((activat$3 or enabl$3) same driver same address$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 11:42
S17	114	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2 same invert$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S18	99	@ay<"2006" and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07
S19	706	((word adj line$1) or wordline$1) same driver$1 same clock$1 same address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 14:02
S20	27	S19 and driver$1.ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:06
S21	685	clock same ((word adj line$1) or wordline$1) same driver$1 same address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 15:07

EAST Search History

S22	614	@ay<"2006" and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S23	4037	365/233.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:17
S24	109	S23 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S25	4306	365/230.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18
S26	97	S25 and (((word adj line$1) or wordline$1) same driver$1 same clock same address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/12 16:18

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/548,132	10/10/2006	2827	2080	061478	27	6

CONFIRMATION NO. 4884

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA92121

UPDATED FILING RECEIPT

Date Mailed: 05/10/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Jentsung Lin, Cardiff by the Sea, CA;

Power of Attorney: The patent practitioners associated with Customer Number 23696

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 03/01/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/548,132**

Projected Publication Date: 04/10/2008

Non-Publication Request: No

Early Publication Request: No

Title

DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the

Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Attorney Docket No.: 061478

COMBINED DECLARATION / POWER OF ATTORNEY

AS BELOW NAMED INVENTOR, I HEREBY DECLARE THAT: This Declaration is of the following type:

☒ Original ☐ Supplemental ☐ Continuation-In-Part ☐ Divisional
☐ Continuation ☐ National Stage of PCT

My residence, post office address and citizenship are as stated below next to my name: I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY RAYS** the specification of which:

☐ is attached hereto.
☒ was filed on **10/10/06** as Serial No. **11/548,132**
☐ was amended on (if applicable).
☐ was described and claimed in PCT International Application No. filed on and as amended under PCT Article 19 on .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(Country)	(Application No.)	(Day/Month/Year/Filed)	Priority Claimed (Yes)	(No)

I hereby claim the benefit under Title 35 USC 119(e) of any United States provisional application(s) listed below:

(Serial No.)	(Filing Date)

I hereby claim the benefit under Title 35 USC 120 of the United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 USC 112, I acknowledge the duty to disclose material information as defined in Title 37 CFR 1.56(a) which occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status)

I hereby appoint the attorneys and/or agents associated with Customer No. 23696 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith. Please direct all telephone calls to Philip R. Wadsworth at (858) 651-4404 and address all correspondence to: QUALCOMM Incorporated, Patent Department, 5775 Morehouse Drive, San Diego, California 92121-1714.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Joint Inventor **Jentsung Lin**	Inventor Signature	Date 3/22/07
Residence **2382 Carol View Drive., #301, Cardiff by the Sea, California 92007**		Citizenship **United States**
Post Office Address **2382 Carol View Drive., #301, Cardiff by the Sea, California 92007**		

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/548,132	10/10/2006	Jentsung Lin	061478

CONFIRMATION NO. 4884

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

FORMALITIES LETTER

Date Mailed: 03/02/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a non-small entity

- **$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents

P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Electronic Patent Application Fee Transmittal

Application Number:	11548132
Filing Date:	10-Oct-2006
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Filer:	Timothy Frederick Loomis/Timothy Sloan
Attorney Docket Number:	061478

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt	
EFS ID:	1733875
Application Number:	11548132
International Application Number:	
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor/Applicant Name:	Jentsung Lin
Customer Number:	23696
Filer:	Timothy Frederick Loomis/Timothy Sloan
Filer Authorized By:	Timothy Frederick Loomis
Attorney Docket Number:	061478
Receipt Date:	01-MAY-2007
Filing Date:	10-OCT-2006
Time Stamp:	16:13:41
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$130
RAM confirmation Number	404
Deposit Account	170026
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	061478_DECL.pdf	711838	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8187	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	720025		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
11/548,132	10/10/2006	2827	1950	061478	5	27	6

CONFIRMATION NO. 4884

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA92121

FILING RECEIPT

Date Mailed: 03/02/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Jentsung Lin, San Diego, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 03/01/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/548,132**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have

no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

BACKGROUND

I. *Field*

[0001] The present disclosure generally relates to memory arrays, and more particularly, to dynamic wordline drivers and decoders for memory arrays.

II. *Description of Related Art*

[0002] In general, memory systems with a traditional dynamic/static circuit structure may place a heavy load on the clock. For example, in a memory structure having a plurality of wordline drivers, a single clock may drive multiple drivers and multiple address decoders, placing a large electrical load on the clock.

[0003] Additionally, each wordline driver may have its own decoded address input, which may place a large load on the decoder and which may utilize a large area of the circuit substrate, increasing complexity and power consumption. Moreover, when the clock signal is provided to multiple wordline drivers, capacitive noise coupling between the wordline driver outputs may introduce additional design complexities. Hence, there is a need for improved wordline drivers.

SUMMARY

[0004] In a particular illustrative embodiment, a circuit device that includes first logic and second logic is disclosed. The first logic receives a clock signal and a first portion of a memory address of a memory array, decodes the first portion of the memory address, and selectively applies the clock signal to a selected group of wordline drivers associated with the memory array. The second logic decodes a second portion of the memory address and selectively activates a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

[0005] In another particular embodiment, a method of selecting a particular wordline of a memory array is disclosed. The method includes selectively providing a clock signal to a selected group of wordline drivers of a plurality of wordline drivers based on a first portion of a memory address of the memory array. Each wordline driver is associated with a wordline of the memory array. The method further includes activating a particular

wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

[0006] In another particular embodiment, an integrated circuit includes a substrate and a plurality of circuit devices. The circuit devices are arranged on the substrate to reduce capacitive coupling noise. The plurality of circuit devices includes a first wordline driver having a first pair of transistors and a first wordline output and includes a second wordline driver having a second pair of transistors and a second wordline output. The first and second wordline drivers are disposed on the substrate in a single row. A first wire trace couples the first pair of transistors to the first wordline output. The second wire trace couples the second pair of transistors to the second wordline output. The first wire trace and the second wire trace are substantially parallel. An advantage of this embodiment is that the layout provides increased capacitive noise-coupling immunity.

[0007] One particular advantage of a particular illustrative embodiment of the circuit device is that a timing delay from a clock to a particular wordline is reduced. Still another particular advantage of a particular illustrative embodiment of the circuit device is that the clock driver's capacitance loading may also be reduced. Another particular advantage of a particular illustrative embodiment is that use of multiple conditional clocks to selectively apply a clock signal reduces power consumption. In a particular embodiment, the clock power consumption may be reduced to one-fourth of the power consumed by a single clock system (e.g. the power consumption of a clock generator may be reduced by 75%). This reduction in power consumption provides an additional advantage in that power is conserved for use in other processes and/or to extend an operational life of a power source, such as a battery.

[0008] Still another particular advantage of a particular illustrative embodiment may be realized by sharing a common address signal among multiple wordline decoders, which reduces power consumption and conserves layout area. In a particular embodiment, four wordline drivers may share a common address signal, which reduces transistor gate loading of the decoders without decreasing speed.

[0009] Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The aspects and the attendant advantages of the embodiments described herein will become more readily apparent by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

[0011] FIG. 1 is a block diagram of a particular illustrative embodiment of a wordline driver system including a plurality of groups of wordline drivers associated with a memory array;

[0012] FIG. 2 is a circuit diagram of a particular illustrative embodiment of a portion of a memory array, such as the memory array of FIG. 1;

[0013] FIG. 3 is a circuit diagram of a particular illustrative embodiment of a group of wordline drivers, such as a selected group of wordline drivers of the plurality of groups of wordline drivers in FIG. 1;

[0014] FIG. 4 is a block diagram of a particular illustrative embodiment of a layout on a circuit substrate including a group of wordline drivers, such as the group of wordline drivers of FIG. 3; and

[0015] FIG. 5 is a flow diagram of a particular illustrative embodiment of a method of selectively activating a wordline of a group of wordline drivers, such as the group of wordline drivers of FIG. 4.

DETAILED DESCRIPTION

[0016] FIG. 1 is a block diagram of a particular illustrative embodiment of a wordline driver system 100 including a set of wordline drivers, such as the groups of wordline drivers 104 and 106 that are associated with a memory array 102. The system 100 may include multiple additional sets of wordline drivers (not shown). Each set of wordline drivers may control up to sixty-four wordlines (numbered zero to sixty-three) using sixty-four corresponding wordline drivers. The set of sixty-four wordlines and corresponding wordline drivers may be divided into groups of wordline drivers, such as the groups of wordline drivers 104 and 106. In a particular embodiment, the group of wordline drivers 104 may drive wordlines, such as the wordlines 132 from zero to three (WL<0>, WL<1>, WL<2>, and WL<3>), and the group of wordline drivers 106 may control wordlines, such as the wordlines 134 from sixty to sixty-three (WL<60>, WL<61>, WL<62>, and WL<63>). In this instance, each of the groups of wordline drivers 104 and 106 control four wordlines, and the set of wordline drivers may include sixteen groups. For clarity,

only the two illustrative groups of wordline drivers 104 and 106 are shown and other groups associated with wordlines of the memory array 102 (such as wordline drivers that control the wordlines from four through fifty-nine) are omitted.

[0017] The system 100 may also include a four-to-sixteen bit memory address decoder 108, a conditional clock generator 110, a two-to-four bit memory address decoder 112, address inputs 114 and 116, and a clock input 118. The system 100 may also include partially decoded address lines 120 and 122, conditional clock outputs 124, 126, 128 and 130, and a group of wordline driver outputs 132 and 134. The conditional clock outputs 124, 126, 128, and 130 are also inputs to the groups of wordline drivers 104 and 106.

[0018] In a particular embodiment, a six-bit memory address specifying one of sixty-four wordlines in the memory array 102 is received. The two-to-four bit memory address decoder 112 may decode a first portion of the six-bit memory address (such as bits zero and one) via the address input 116, and the four-to-sixteen bit memory address decoder 108 may decode the remainder (i.e. a second portion) of the six-bit memory address (such as bits two to five) via the address input 114. The two-to-four bit decoder 112 may decode the first portion of the memory address and may provide the decoded portion to the conditional clock generator 110. The conditional clock generator 110 receives a clock signal via the clock input 118 and selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130. In general, each clock output 124, 126, 128 and 130 is coupled to each of the groups of wordline drivers 104 and 106 of the particular group of wordline drivers. In a particular embodiment, the conditional clock generator 110 may derive the clock outputs 124, 126, 128 and 130 from a single clock.

[0019] The four-to-sixteen bit memory address decoder 108 decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address. For example, the decoded four bits of the partially decoded address may be applied to the partially decoded address line (0) 120 to enable the group of wordline drivers 104 to enable one of the four wordlines (WL<0:3>) 132 to access data stored in the memory array 102.

[0020] In general, each group of wordline drivers, such as the group of wordline drivers 104 may share a common partially decoded address input, such as the partially decoded address line (0) 120 for the group of wordline drivers 104, reducing layout area usage and layout complexity. Additionally, the common address input reduces input gate capacitance loading without introducing timing delays. In general, the clock outputs 124, 126, 128,

and 130 determine whether a device is in a dynamic evaluation state (e.g., an active evaluation state where a clock signal is applied) or in a static precharge state (e.g., a fixed voltage level, such a voltage high signal, is applied). Since only one of the four clock outputs 124, 126, 128 and 130 may be active at a time, only one of the four wordline drivers of the group of wordline drivers 104 is in the dynamic evaluation state (e.g. a clock signal is present), while the other three remain in a static precharge state (such as a logic high state). If the four-to-sixteen memory address decoder 108 decodes a portion (e.g. bits two to five) of the memory address to determine a set of wordlines from zero to three (WL<0>,WL<1>, WL<2> and WL<3> in Fig.1), the four-to-sixteen bit memory address decoder 108 applies a signal to the address line 120. The dynamic evaluation state of a clock output, such as the clock 124, activates a particular wordline of the group of wordline drivers 104, such as wordline zero (WL<0>) of the memory array 102. In general, the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104, for example.

[0021] FIG. 2 is a circuit diagram of a particular illustrative embodiment of a portion 200 of a memory array, such as a portion of the memory array 102 of FIG. 1. The portion 200 of the memory array 102 includes wordlines 202, 204, 206, and 208 and bit lines 210 and 212. The portion 200 of the memory array 102 further includes transistors 214 and 216 and cross-coupled inverters 218 and 220 associated with the wordline 202. Additionally, the portion 200 of the memory array 102 may include transistors 222 and 224 and cross-coupled inverters 226 and 228 associated with the wordline 204. The portion 200 of the memory array 102 may further include transistors 230 and 232 and cross-coupled inverters 234 and 236 associated with the wordline 206. The portion 200 of the memory array 102 also includes transistors 238 and 240 and cross-coupled inverters 242 and 244 associated with the wordline 208. In a particular embodiment, the wordlines 202, 204, 206 and 208 may correspond to the wordlines 132 of the group wordline drivers 104 of FIG. 1.

[0022] In operation, when a particular wordline, such as the wordline 202 is charged, the other wordlines 204, 206 and 208 are held at a logic low level. The charged wordline 202 activates the transistors 214 and 216, which apply a differential voltage to the bit lines 210 and 212. The differential voltage is related to a bit stored by the cross-coupled inverters 242 and 244, which operates as a data latch to store a bit value. A sense amplifier or a

differential amplifier (not shown) may be coupled to the bit lines 210 and 212 to detect a differential voltage and to output a value related to a value of the stored bit associated with the wordline 202.

[0023] FIG. 3 is a circuit diagram of a particular illustrative embodiment of a group of wordline drivers, such as the group of wordline drivers 104 in FIG. 1. The group of wordline drivers 104 includes an address input 120, clock outputs 124, 126, 128 and 130, an inverter 302, a shared address line 304, and wordline drivers 306, 308, 310 and 312.

[0024] The wordline driver 306 includes a first transistor (Mp0) 314, a second transistor (Mn0) 316, and an output driver 318, including a transistor 320 and an inverter (XWL0) 322 that are coupled to the first and second transistors 314 and 316 via a data line (ddh0) 324. The transistor 320 holds the data from device leakage. The inverter 322 is also coupled to the wordline (WL<0>) 202. The first transistor 314 includes a first terminal 326 coupled to a power terminal, a control terminal 328 coupled to the clock 130, and a second terminal coupled to the data line (ddh0) 324. The second transistor 316 includes a first terminal coupled to the data line (ddh0) 324, a control terminal 330 coupled to the clock 130, and a second terminal 332 coupled to the shared address line 304.

[0025] The wordline driver 308 includes a first transistor (Mp1) 334, a second transistor (Mn1) 336, and an output driver 338, including a transistor 340 to hold the data from device leakage and including an inverter (XWL1) 342 that are coupled to the first and second transistors 334 and 336 via a data line (ddh1) 344. The inverter 342 is also coupled to the wordline (WL<1>) 204. The first transistor 334 includes a first terminal 346 coupled to a power terminal, a control terminal 348 coupled to the clock 128, and a second terminal coupled to the data line (ddh1) 344. The second transistor 336 includes a first terminal coupled to the data line (ddh1) 344, a control terminal 350 coupled to the clock 128, and a second terminal 352 coupled to the shared address line 304.

[0026] The wordline driver 310 includes a first transistor (Mp2) 354, a second transistor (Mn2) 356, and an output driver 358, including a transistor 360 to hold the data from device leakage and including an inverter (XWL2) 362 that are coupled to the first and second transistors 354 and 356 via a data line (ddh2) 364. The inverter 362 is also coupled to the wordline (WL<2>) 206. The first transistor 354 includes a first terminal 366 coupled to a power terminal, a control terminal 368 coupled to the clock 126, and a second terminal coupled to the data line (ddh2) 364. The second transistor 356 includes a first

terminal coupled to the data line 364, a control terminal 370 coupled to the clock 126, and a second terminal 372 coupled to the shared address line 304.

[0027] The wordline driver 312 includes a first transistor (Mp3) 374, a second transistor (Mn3) 376, and an output driver 378, including a transistor 380 to hold the data from device leakage and including an inverter (XWL3) 382 that are coupled to the first and second transistors 374 and 376 via a data line (ddh3) 384. The inverter 382 is also coupled to the wordline (WL<3>) 208. The first transistor 374 includes a first terminal 386 coupled to a power terminal, a control terminal 388 coupled to the clock 124, and a second terminal coupled to the data line (ddh3) 384. The second transistor 376 includes a first terminal coupled to the data line 384, a control terminal 390 coupled to the clock 124, and a second terminal 392 coupled to the shared address line 304.

[0028] In a particular embodiment, an address is received via the address input 120 and inverted by the inverter 302 to provide a shared address input 304. As previously disclosed, a conditional clock generator, such as the conditional clock generator 110 of FIG. 1, applies a clock signal to a selected clock output, such as the clock output 130. The clock signal applied to the clock output 130 selectively activates the wordline driver 306 to access data of a memory array (such as the memory array 102 in FIG. 1) via the selected wordline 202. By applying the clock signal only to the selected clock output 130, power consumption is reduced, since the clock only drives a single line of a group of wordline drivers, as opposed to driving all of the wordline drivers. In a particular embodiment, since only one of the four clock outputs 124, 126, 128 and 130 is active at any given time, the power consumed by the clock may be reduced by 75% over a single clock system.

[0029] By sharing a common address 304 among multiple wordline drivers (decoders) 306, 308, 310, and 312, power consumption of the overall wordline driver circuitry may be reduced. Additionally, the layout area of the wordline drivers and layout complexity of the circuit design may be reduced. Further, the shared address input reduces transistor gate loading (e.g. control terminals 328, 330, 348, 350, 368, 370, 388, and 390) of the wordline drivers (decoders) 306, 308, 310 and 312 without decreasing the performance of the circuit.

[0030] In a particular illustrative embodiment, a conditional clock generator, such as the conditional clock generator 110 in FIG. 1, applies the clock signal to a selected clock output, such as the clock output 126. The other clocks 124, 128 and 130 may be held at a ground voltage level. The transistors 314, 334, and 374 are p-channel transistors, which

are activated by a logic low signal. Thus, when the clocks 124, 128 and 130 are at a logic low level, the p-channel transistors 314, 334 and 374 are active, and the data lines 324, 344 and 384 are at a logic high level, placing a logic low voltage on the wordlines 202, 204 and 208, due to the inverters 322, 362 and 382.

[0031] The clock 126 deactivates the p-channel transistor (Mp2) 354 and activates the n-channel transistor (Mn2) 356. The address 120 is inverted by the inverter 302 and applied to the address line 304, which is coupled to the source of the n-channel transistor 356. The inverted address appears on the data line (ddh2) 364 and is inverted again by the inverter (XWL2) 362, coupling the address 120 to the wordline (WL<2>) 206. The clock 126 activates the desired wordline 206, while causing the other wordlines 202, 204 and 208 to be held at a logic low level. Thus, only the desired wordline 206 is active at any given time. The conditional clock generator, such as the conditional clock generator 110 in FIG. 1, applies the clock signal to only one of the four clocks 124, 126, 128 and 130, reducing power consumption by 75%.

[0032] In general, other conditional clock generator implementations may be used. For example, in a particular embodiment, a three-bit portion of the address 120 may be decoded and may be applied by the conditional clock generator to selectively apply a clock signal to one of eight lines, reducing power consumption by approximately 87.5%. Thus, the particular arrangement may allow for further reductions in power consumption.

[0033] FIG. 4 is a block diagram of a particular illustrative embodiment of a circuit layout 400 of a circuit substrate including a group of wordline drivers, such as wordline drivers 306, 308, 310 and 312 of FIG. 3. In general, the elements of the wordline drivers 306, 308, 310 and 312 are depicted as rectangular regions on the substrate. It should be understood that transistors and other circuit components may be formed within such regions and may be sized to match the memory cell's height, such as a height between wordlines 202 and 208 in FIG. 2. For the purpose of the discussion, the regions are identified by the particular circuit components of FIG. 3 that may be formed within the particular region.

[0034] The circuit layout 400 includes the first transistor (Mp0) 314, the second transistor (Mn0) 316, and the output driver (XWL0) 318 of the wordline driver 306 in FIG. 3. The circuit layout 400 also includes the first transistor (Mp1) 334, the second transistor (Mn1) 336, and the output driver (XWL1) 338 of the wordline driver 308 in FIG. 3. The circuit layout 400 may also include the first transistor (Mp2) 354, the second transistor (Mn2)

356, and the output driver (XWL2) 358 of the wordline driver 310 in FIG. 3. Additionally, the circuit layout 400 may include the first transistor (Mp3) 374, the second transistor (Mn3) 376, and the output driver (XWL3) 378 of the wordline driver 312 in FIG. 3.

[0035] In general, a first row 402 includes the transistor (Mn0) 316, the transistor (Mn1) 336, the transistor (Mp0) 314, the transistor (Mp1) 334, the output driver (XWL0) 318, and the output driver (XWL1) 338. A second row 404 includes the transistor (Mn2) 356, the transistor (Mn3) 376, the transistor (Mp2) 354, the transistor (Mp3) 374, the output driver (XWL2) 358, and the output driver (XWL3) 378. The first row 402 and the second row 404 are substantially parallel.

[0036] Additionally, the line (ddh0) 324, the line (ddh1) 344, the line (ddh2) 364 and the line (ddh3) 384 are substantially parallel to one another. The output driver (XWL0) 318 may include a first region (N) 406 and a second region (P) 408. The output driver (XWL1) 338 may include a first region (P) 410 and a second region (N) 412. The output driver (XWL2) 358 may include a first region (N) 414 and a second region (P) 416. The output driver (XWL3) 378 may include a first region (P) 418 and a second region (N) 420. In general, the regions 408, 410, 416 and 418 may be utilized to form a transistor, such as the pull up transistors 320, 340, 360, and 380 in FIG. 3. The regions 406, 412, 414, and 420 may cooperate with the regions 408, 410, 416 and 418 to form the inverters 322, 342, 362, and 382 of FIG. 3.

[0037] By arranging the layout 400 of the wordline drivers 306, 308, 310 and 312 on the substrate as shown, capacitive noise-coupling immunity of the structure is improved. In particular, if the same clock signal is applied to each of the wordline drivers, any of the wire traces 324, 344, 364, and 384 and the corresponding circuit devices may be active. In such an instance, there may be undesired cross-coupling between the wire traces, such that a signal applied to one trace may experience inductive function error and power loss caused by capacitive coupling between the wire traces. However, a conditional clock, such as the conditional clock 110 in FIG. 1, activates only one wire trace and one corresponding set of structures at any given time. The exclusive nature of the application of a signal to the traces ensures that only one of the four wordline drivers 306, 308, 310 and 312 are in a dynamic evaluation state at any given time, and that the other wordline drivers are in a static "precharge" state. The particular arrangement places data line (ddh0) 314 and the wordline output 202 adjacent to the data line (ddh1) 334. The data line (ddh0) 314 and its associated wordline output 202 are inverted with respect to each other. Thus, a

voltage applied to the data line (ddh0) 314 is inverted at the wordline 202. While the data line (ddh1) 334 might ordinarily experience capacitive coupling with the data line (ddh0) 314, resulting in data errors and power loss, the opposite voltages of the data line (ddh0) 314 and the associated wordline 202 apply opposing capacitive influences on the adjacent data line (ddh1) 334, canceling capacitive noise coupling between the data lines (ddh0 and ddh1) 314 and 334, for example. The particular arrangement generally reduces capacitive noise coupling.

[0038] For example, if the clock signal is selectively applied to the clock output 130 in FIG. 3, the line (ddh0) 324 is in a dynamic evaluation state. The line (wire trace) (ddh1) 344, the line (ddh2) 364, and the line (ddh3) 384 are in a static precharge state. The line (ddh1) 344 is closest in proximity to the line (ddh0) 324, so the line (ddh0) 324 and wordline (WL<0>) 202 may be aggressors relative to the line (ddh1) 344. When a voltage on the line (ddh0) 324 is decreasing, the wordline (WL<0>) 202 is rising. The rising voltage at the wordline 202 is cross-coupled with the line (ddh1) 344, helping to offset or cancel coupling between the line (ddh1) 344 and the line (ddh0). The lines (ddh1, ddh2, and ddh3) 344, 364, and 384 are statically held by the transistors (Mp1, Mp2, and Mp3) 334, 354, and 374, respectively. The wordlines (WL<1>, WL<2>, and WL<3>) 204, 206, and 208 are statically inverted relative to the lines (ddh1, ddh2, and ddh3) 344, 364, and 384, respectively. Thus, the layout 400 contributes to the robustness of the circuit design, by reducing capacitive noise coupling between the wordline drivers 306, 308, 310, and 312.

[0039] Table 1 below illustrates a relationship between the data lines (ddh0, ddh1, ddh2, and ddh3) 324, 344, 364, and 384 that enhances capacitive noise immunity.

TABLE 1.

Dynamic nodes	**Situation**	**Aggressor**	**Note:**
data line (ddh0) 324	clk<0> 130 =active; dynamic evaluation state	not applicable.	
data line (ddh1) 344	clk<1> 128 =0; static precharged state	When the data line (ddh0) 324 is falling, the wordline (WL<0>) 202 is rising.	The data line (ddh1) is statically held by the clocked p-channel transistor (Mp1) 334. The overlap of the rising wordline (WL<0>) 202 assists the data line (ddh1) 344 in resisting the

			capacitive coupling from (ddh0) 324 falling.
data line (ddh2) 364	clk<2> 126 =0; static precharged state	none.	The data line (ddh2) is statically held by the clocked p-channel transistor (Mp2) 354.
data line (ddh3) 384	clk<3> 124 =0; static precharged state	none.	The data line (ddh3) is statically held by the clocked p-channel transistor (Mp3) 374.

[0040] In FIG. 4, the data line (ddh0) 324 and the wordline (WL<0>) 202 are adjacent to the data line (ddh1) 344, but are not adjacent to the other data lines (ddh2 and ddh3) 364 and 384. Thus, only the data line (ddh1) 344 may be influenced by capacitive coupling with the data line (ddh0) 324.

[0041] Table 2 below illustrates a relationship between the data lines (ddh0, ddh1, ddh2, and ddh3) 324, 344, 364, and 384 that enhances capacitive noise immunity when more than one data line is adjacent to the data line that is in a dynamic evaluation state.

TABLE 2.

Dynamic nodes	**Situation**	**Aggressor**	**Note:**
data line (ddh0) 324	clk<0> 130 = 0; static precharged state	When the data line (ddh1) 344 is falling, the wordline (WL<1>) 204 is rising.	The data line (ddh0) is statically held by the clocked p-channel transistor (Mp0) 314. The overlap of the rising wordline (WL<1>) 204 assists the data line (ddh0) 324 in resisting the capacitive coupling from (ddh0) 344 falling.
data line (ddh1) 344	clk<1> 128 =active; dynamic evaluation state	Not applicable.	
data line (ddh2) 364	clk<2> 126=0; static precharged state	When the data line (ddh1) 344 is falling, the wordline (WL<1>) 204 is rising.	The data line (ddh2) is statically held by the clocked p-channel transistor (Mp2) 354. The overlap of the rising wordline (WL<1>) 204 assists the data line (ddh2) 364 in resisting the capacitive coupling from (ddh1) 344 falling.
data line (ddh3) 384	clk<3> 124=0; static precharged state	none.	The data line (ddh3) is statically held by the clocked p-channel transistor (Mp3) 374.

[0042] In general, the data lines (ddh1 and ddh3) 344 and 384 are assisted by the output of the wordline (WL<2>) 206 and the data lines (ddh0 and ddh2) 324 and 364 are assisted by the output of the wordline (WL<1>) 204 in reducing capacitive coupling. As shown in Table 1, the output value or voltage of the wordline 202 is inverted relative to its associated data line (ddh0) 324, and the adjacent data line (ddh1) 344 experiences reduced capacitive noise coupling.

[0043] FIG. 5 is a flow diagram of a particular illustrative embodiment of a method of selectively activating a wordline of a group of wordline drivers, such as the group of wordline drivers of FIG. 4. A partially decoded memory address is received at a wordline

driver of a memory array, at 500. A clock signal is selectively provided to a selected group of wordline drivers based on a first portion of the memory address of the memory array, where each wordline driver of the plurality of wordline drivers is associated with a wordline of the memory array, at 502. A particular wordline driver of the selected group of wordline drivers is activated according to a second portion of the memory address, at 504. Other wordline drivers of the selected group of wordline drivers are held in an inactive precharge state, at 506.

[0044] In a particular embodiment, the memory address includes six address bits. The first portion of the memory address may include two bits, and the second portion of the memory address may include the remaining four bits, for example. A two-to-four bit decoder, such as the two-to-four bit decoder 112 in FIG. 1, may decode the first portion of the address and provide the decoded first portion to a conditional clock generator, such as the conditional clock generator 110 in FIG. 1. The conditional clock generator may receive a clock input, such as the clock input 118 in FIG. 1, and may selectively apply the clock signal to a selected clock, such as one of the clocks 124, 126, 128 and 130 in FIGS. 1 and 3. The conditional clock generator may apply a zero voltage, a logic low, or ground voltage signal to the non-selected clocks.

[0045] The selected clock may activate a wordline driver, such as the wordline drivers 306, 308, 310 and 312 in FIG. 3, to provide an address input (such as the address 120 in FIG. 3) to an associated wordline (such as the wordlines 202, 204, 206, and 208 in FIGS. 2 and 3)

[0046] In a particular embodiment, a method is disclosed that may include receiving a clock signal (such as the clock input 118 in FIG. 1) and selectively applying the clock signal to one of a plurality of clocks or clock outputs (such as the clocks 124, 126, 128 and 130 in FIGS. 1 and 3) according to the decoded first portion of the memory address (e.g., according to at least two bits of the memory address using, for example, a two-to-four bit decoder, such as the two-to-four bit decoder 112 in FIG. 1). In another particular embodiment, the method may include determining a clock output (such as the clocks 124, 126, 128 and 130 in FIG. 1) according to the decoded first portion of the memory address using a conditional clock generator (such as the conditional clock generator 110 in FIG. 1). In another particular illustrative embodiment, a selected group of wordline drivers (such as the wordline drivers 306, 308, 310 and 312) includes a shared address input (e.g. the

address input 120 or the address input 122 in FIG. 1 or the address input 304 in FIG. 3) to receive the second portion of the memory address.

[0047] The various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, configurations, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0048] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present disclosure. Various modifications to such disclosed embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features as defined by the following claims.

WHAT IS CLAIMED IS:

1. A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

2. The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

3. The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

4. The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

5. The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

6. The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.

7. A method of selecting a particular wordline of a memory array, the method comprising:

selectively providing a clock signal to a selected group of a plurality of wordline drivers based on a first portion of a memory address of the memory array, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array; and

activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

8. The method of claim 7, further comprising:

receiving a clock signal;

selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

9. The method of claim 7, further comprising:

determining a clock output according to the first portion of the memory address using a conditional clock generator.

10. The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

11. A circuit device comprising:

means for selectively providing a clock signal to a selected group of wordline drivers based on a first portion of a memory address of a memory array; and

means for activating a particular wordline driver of the selected group of wordline drivers according to a second portion of the memory address.

12. The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

13. The circuit device of claim 12, further comprising:

a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal, the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

14. The circuit device of claim 12, further comprising a decoder to decode the memory address to determine the second portion of the memory address and to apply the second portion of the memory address to a shared address line.

15. The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

16. The circuit device of claim 15, wherein the integrated circuit includes the memory array.

17. A circuit device comprising:

a group of wordline drivers, each of the wordline drivers comprising a control terminal, an address terminal, and an output terminal, the output terminal coupled to a wordline of a memory array;

an inverter including an input to receive a memory address and including an inverted output coupled to the address terminal of each of the wordline drivers; and

a plurality of clock outputs, each of the plurality of clock outputs coupled to the control terminal of a respective one of the group of wordline drivers.

18. The circuit device of claim 17, further comprising logic to derive the plurality of clock outputs from a single clock.

19. The circuit device of claim 17, further comprising:

a clock generator to receive a clock signal and to selectively apply the clock signal to one of the plurality of clock outputs.

20. The circuit device of claim 19, wherein the wordline driver associated with the selected one of the plurality of clock outputs is in a dynamic evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

21. The circuit device of claim 20, wherein the state precharge state comprises a fixed voltage level.

22. A circuit device comprising:

an address input;

a plurality of clock outputs;

a group of wordline drivers coupled to a wordline of a memory array, each wordline driver of the group of wordline drivers coupled to the address input and coupled to a respective clock output of the plurality of clock outputs; and

logic to selectively apply a clock signal to one of the plurality of clock outputs to activate a selected wordline driver of the group of wordline drivers.

23. The circuit device of claim 22, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state and wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

24. The circuit device of claim 23, wherein a state of the wordline driver is determined by the selective application of the clock signal.

25. The circuit device of claim 22, wherein the logic comprises a conditional clock generator.

26. An integrated circuit comprising:

a substrate; and

a plurality of circuit devices comprising:

a first wordline driver comprising a first transistor, a third transistor, and a first wordline output;

a second wordline driver comprising a second transistor, a fourth transistor, and a second wordline output;

wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the first wordline output and the second wordline output are disposed on the substrate in a single row;

wherein the first wire trace couples the first transistor to the third transistor and the third transistor to the first wordline output;

wherein the second wire trace couples the second transistor to the fourth transistor and the fourth transistor to the second wordline output; and

wherein the first wire trace and the second wire trace are substantially parallel.

27. The integrated circuit of claim 26, further comprising:

a first output associated with the first wire trace; and

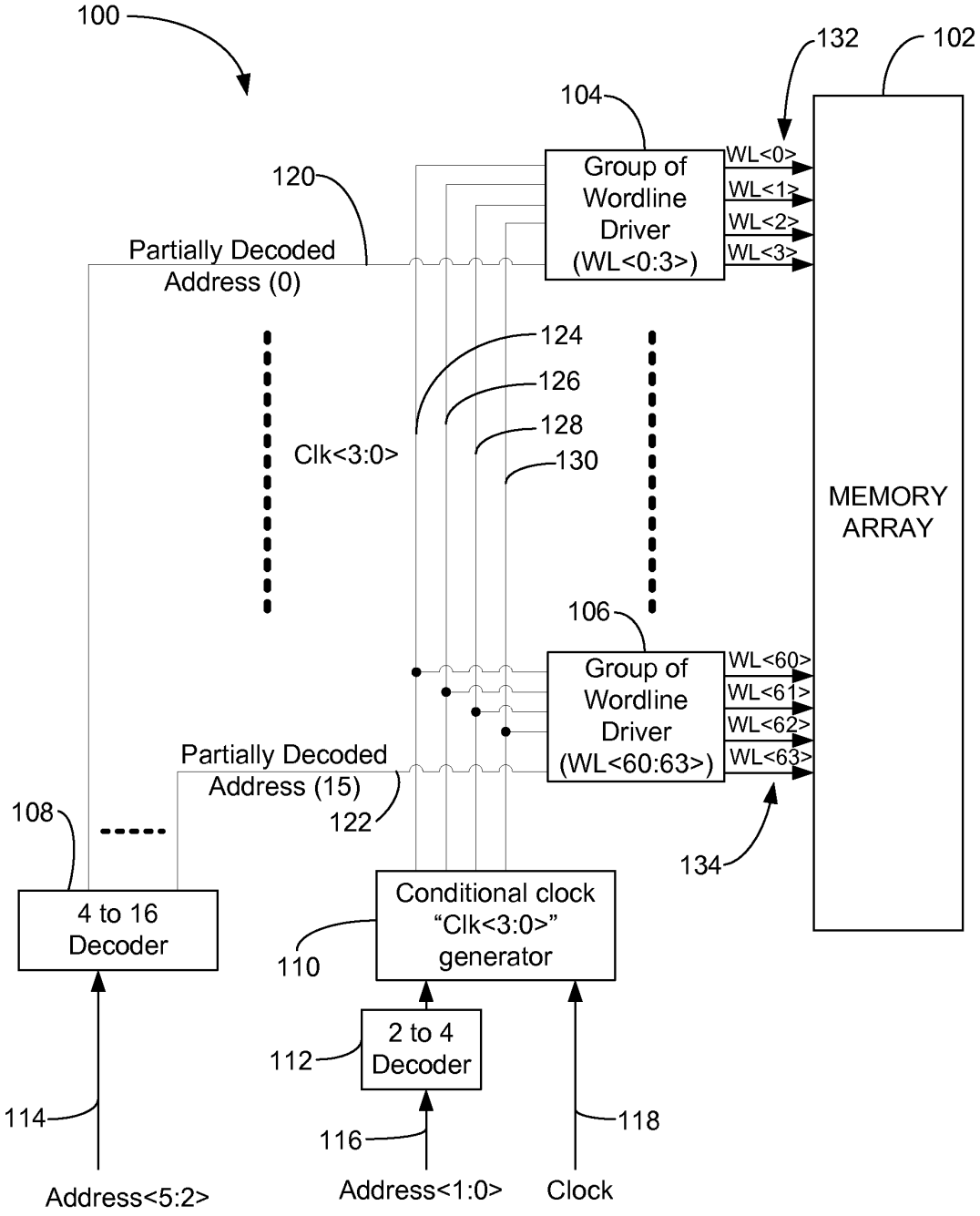
a second output associated with the second wire trace;

wherein a voltage on the first output opposes capacitive coupling between the first wire trace and the second wire trace.

DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS

ABSTRACT

[0049] In a particular illustrative embodiment, a circuit device that includes first logic and second logic is disclosed. The first logic receives a clock signal and a first portion of a memory address of a memory array, decodes the first portion of the memory address, and selectively applies the clock signal to a selected group of wordline drivers associated with the memory array. The second logic decodes a second portion of the memory address and selectively activates a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.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104
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WL<1>
WL<2>
WL<3>
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Partially Decoded Address (0)
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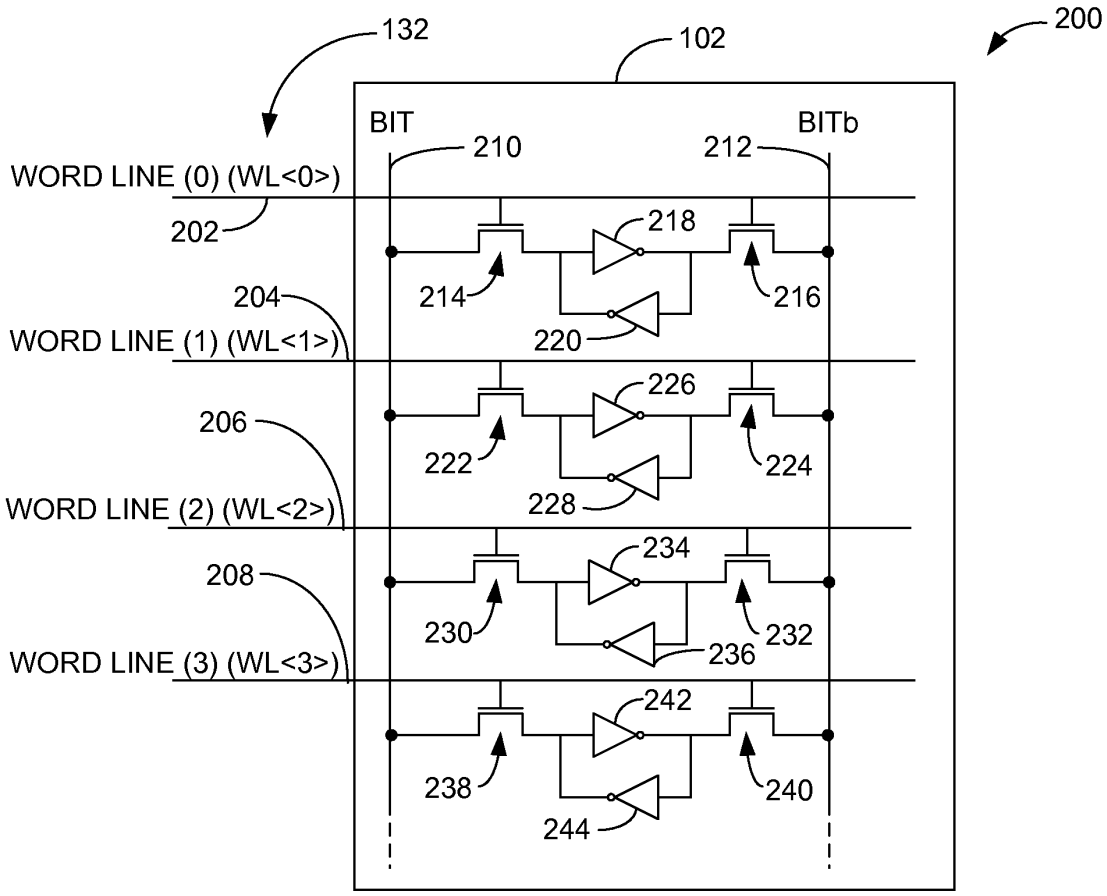
126
128
130
Clk<3:0>
MEMORY ARRAY
106
Group of Wordline Driver (WL<60:63>)
WL<60>
WL<61>
WL<62>
WL<63>
Partially Decoded Address (15)
122
108
134
4 to 16 Decoder
Conditional clock "Clk<3:0>" generator
110
2 to 4 Decoder
112
114
116
118
Address<5:2>
Address<1:0>
Clock

FIG. 1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BITb
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226
206
222
224
WORD LINE (2) (WL<2>)
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WORD LINE (3) (WL<3>)
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242
238
240
244

FIG. 2

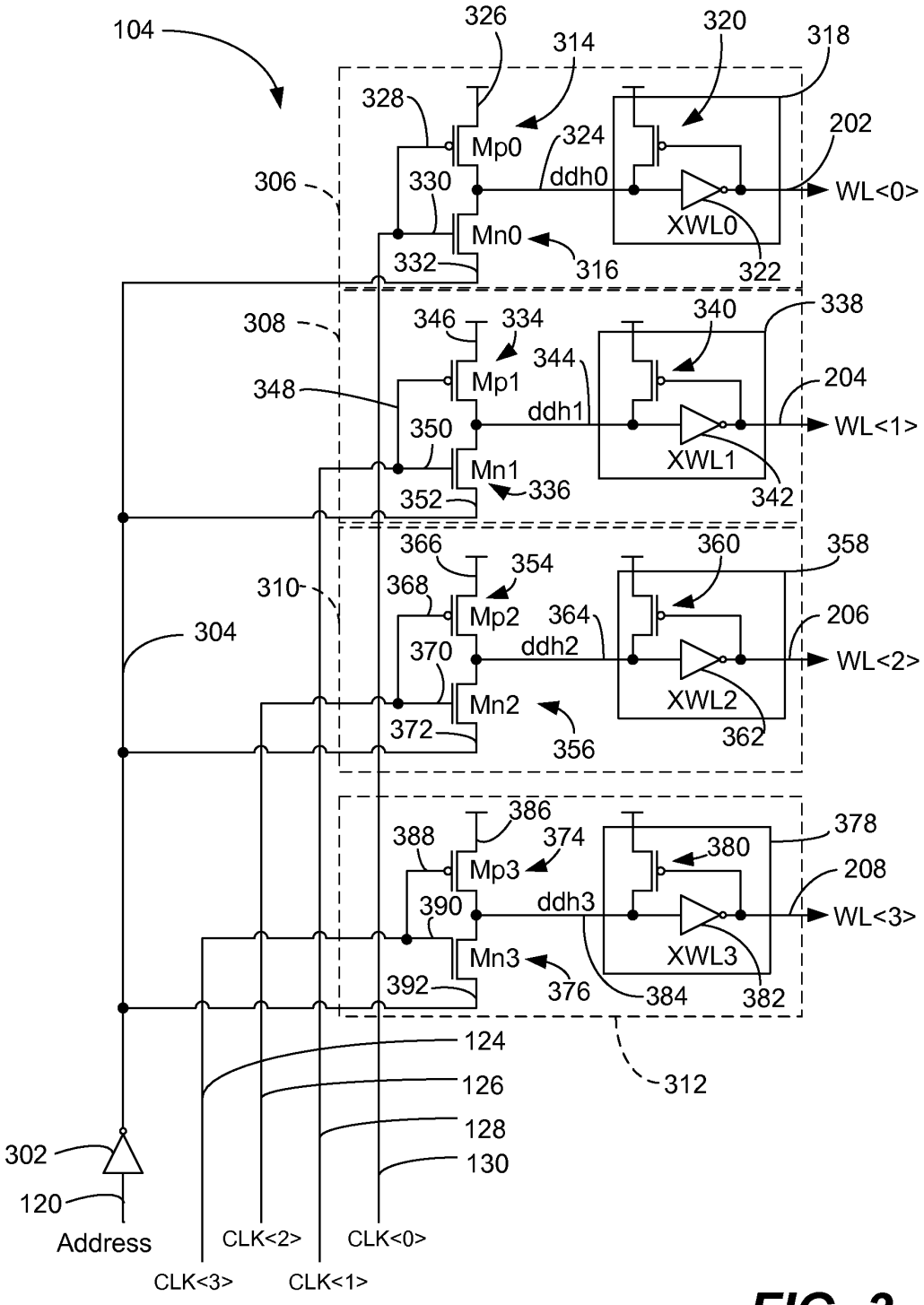
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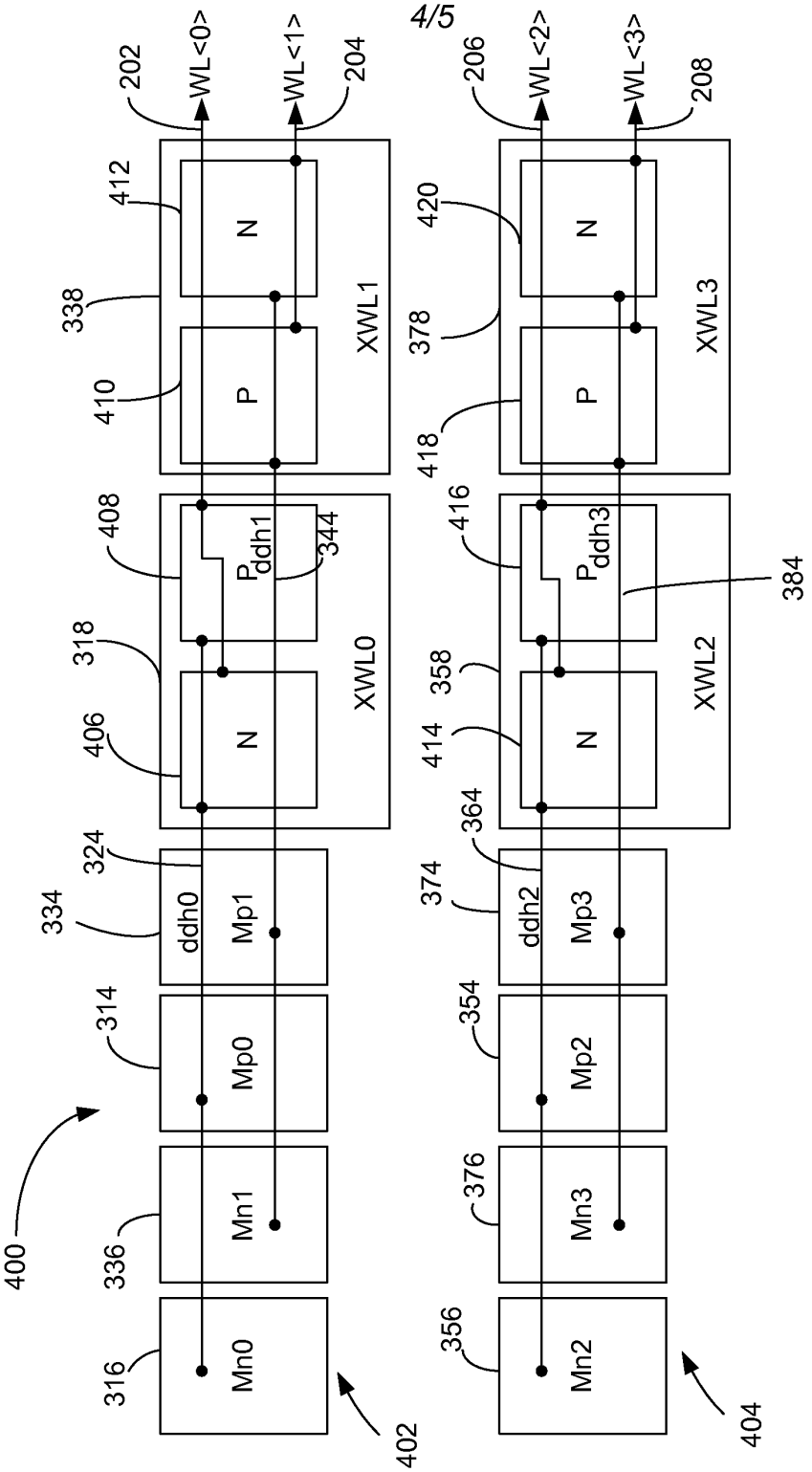
FIG. 3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354
336
376
316
356
400
402
404
N
P
XWL1
XWL3
Pddh1
Pddh3
344
384
XWL0
XWL2
ddh0
ddh2
Mp1
Mp3
Mp0
Mp2
Mn1
Mn3
Mn0
Mn2

FIG. 4

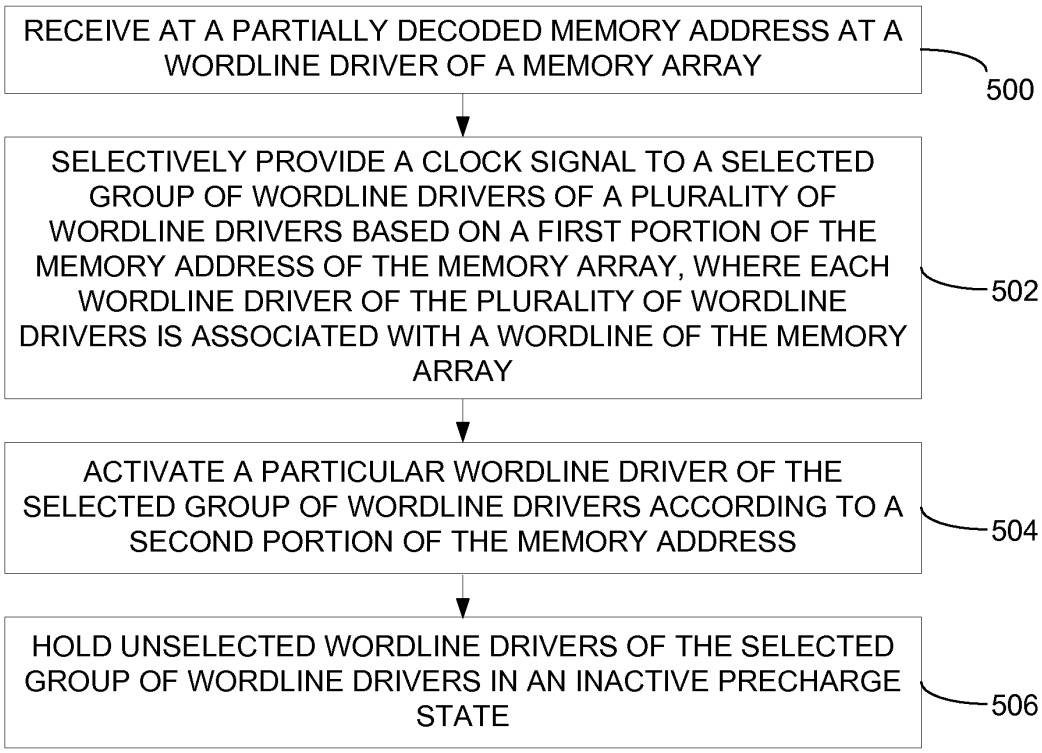
RECEIVE AT A PARTIALLY DECODED MEMORY ADDRESS AT A WORDLINE DRIVER OF A MEMORY ARRAY
500
SELECTIVELY PROVIDE A CLOCK SIGNAL TO A SELECTED GROUP OF WORDLINE DRIVERS OF A PLURALITY OF WORDLINE DRIVERS BASED ON A FIRST PORTION OF THE MEMORY ADDRESS OF THE MEMORY ARRAY, WHERE EACH WORDLINE DRIVER OF THE PLURALITY OF WORDLINE DRIVERS IS ASSOCIATED WITH A WORDLINE OF THE MEMORY ARRAY
502
ACTIVATE A PARTICULAR WORDLINE DRIVER OF THE SELECTED GROUP OF WORDLINE DRIVERS ACCORDING TO A SECOND PORTION OF THE MEMORY ADDRESS
504
HOLD UNSELECTED WORDLINE DRIVERS OF THE SELECTED GROUP OF WORDLINE DRIVERS IN AN INACTIVE PRECHARGE STATE
506

FIG. 5

PTO/SB/14 (08-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	
	Application Number	
Title of Invention	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jentsung		Lin	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	Ca	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i US

Mailing Address of Applicant:

Address 1	
Address 2	

City		State/Province	
Postal Code		Country i	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23696		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS		
Attorney Docket Number		Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	
	Application Number	
Title of Invention	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS	

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ US Representative (37 CFR 11.9)
Customer Number	23696		

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Priority Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

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Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☐

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	
	Application Number	
Title of Invention	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:			
Address 1			
Address 2			
City		**State/Province**	
Country [i]		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Timothy F. Loomis/			Date (YYYY-MM-DD)	2006-10-10
First Name	Loomis	Last Name	Timothy	Registration Number	37383

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor:	Jentsung Lin
Filer:	George Christ Pappas/Darla Kasmedo
Attorney Docket Number:	061478

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Claims in excess of 20	1202	7	50	350
Independent claims in excess of 3	1201	3	200	600
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1950**

Electronic Acknowledgement Receipt

EFS ID:	1245287
Application Number:	11548132
Confirmation Number:	4884
Title of Invention:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS
First Named Inventor:	Jentsung Lin
Customer Number:	23696
Filer:	George Christ Pappas/Darla Kasmedo
Filer Authorized By:	George Christ Pappas
Attorney Docket Number:	061478
Receipt Date:	10-OCT-2006
Filing Date:	
Time Stamp:	16:41:11
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1950
RAM confirmation Number	404
Deposit Account	170026
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		061478application.pdf	172312	yes	21
	Multipart Description				
	Doc Desc		Start	End	
	Specification		1	14	
	Claims		15	20	
	Abstract		21	21	
Warnings:					
Information:					
2	Drawings	Figures_final.pdf	90650	no	5
Warnings:					
Information:					
3	Application Data Sheet	US_ADS_Form_SB_14.pdf	3271733	no	4
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	8548	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3543243		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 11/548,132

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							200
TOTAL CLAIMS (37 CFR 1.16(i))	27	* 7	X$ 25=		OR	X$50=	350
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6 minus 3 =	* 3	X$100=			X$200=	600
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1950

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI- TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI- TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.