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**Renous**

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(54) **POWER SUPPLY CIRCUIT WITH A VOLTAGE SELECTOR**

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(52) **U.S. Cl.** ..... **327/408**; 327/530; 307/80; 307/126
(58) **Field of Search** ..... 327/407, 408, 327/530, 546; 307/64, 80, 87, 126, 130

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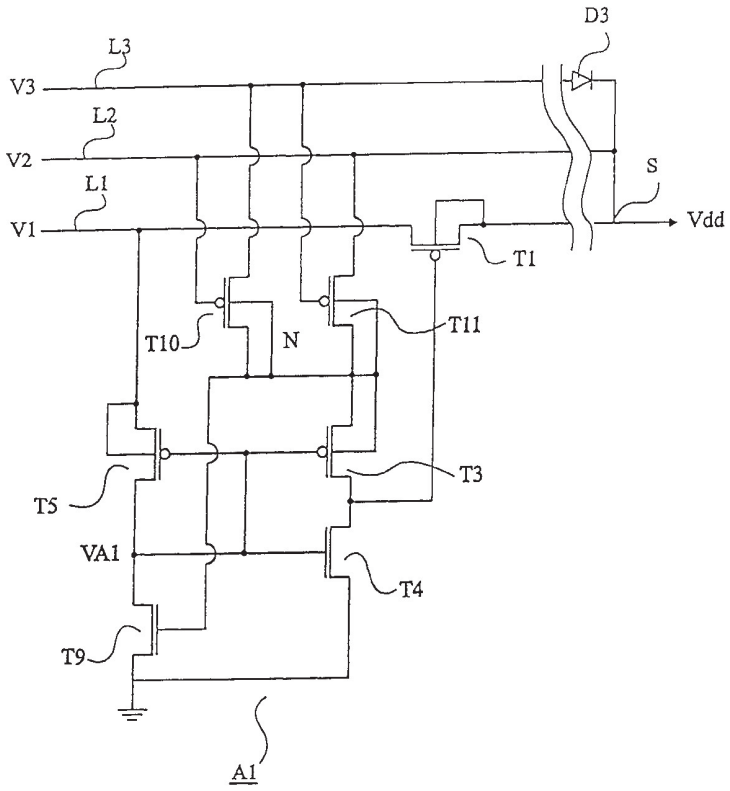
(57) **ABSTRACT**

A power supply circuit receiving several supply voltages on respective switches, at least one of the switches being a first PMOS transistor connected between one of the supply voltages and a common output terminal, this switch being associated with a second PMOS transistor connected between the gate of the first transistor and a power supply node maintained at the highest of the other supply voltages, with a third NMOS transistor, which is less conductive in the on state than the second transistor, connected between the gate of the first transistor and the ground, and with a fourth PMOS transistor having its source connected to the power supply line of the switch and its drain connected to ground via a current source, and to the gates of the second, third, and fourth transistors.

**17 Claims, 3 Drawing Sheets**



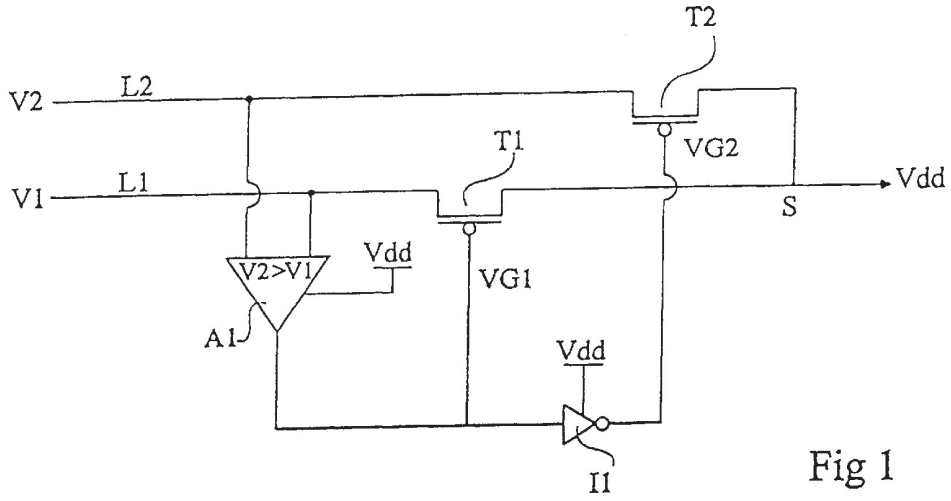



Fig 1

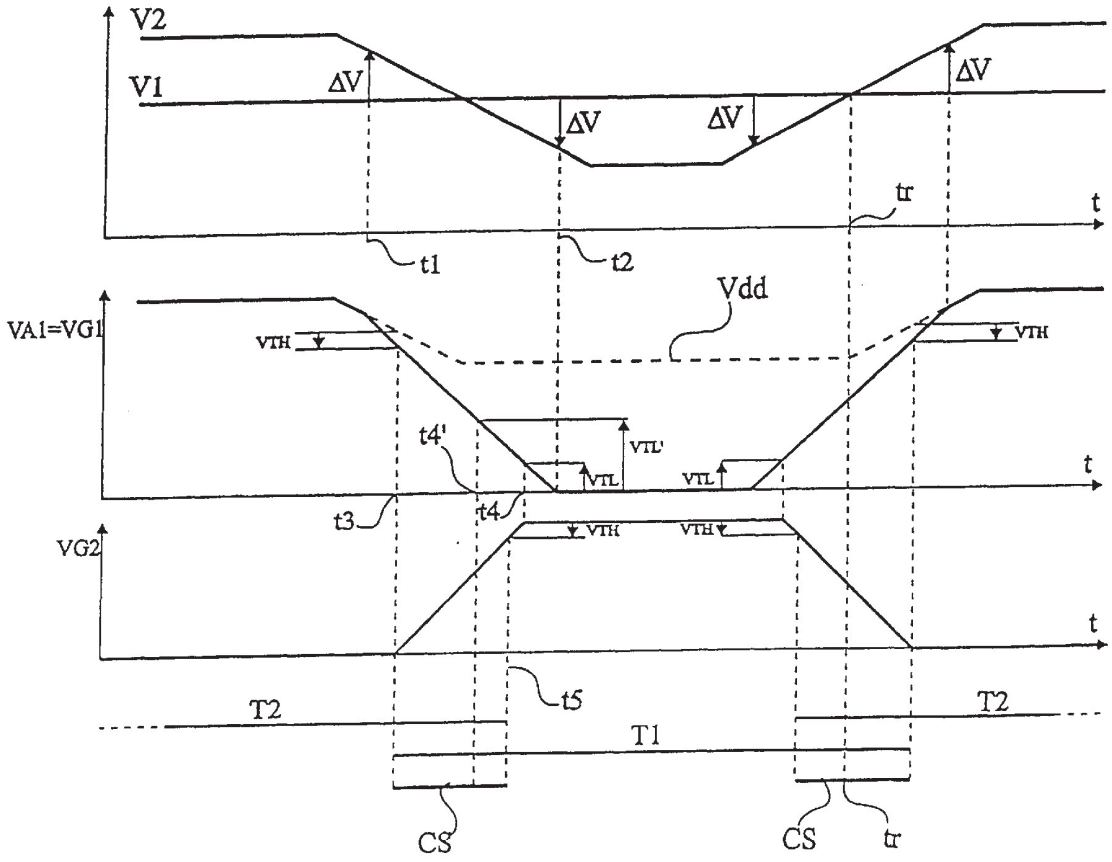



Fig 2

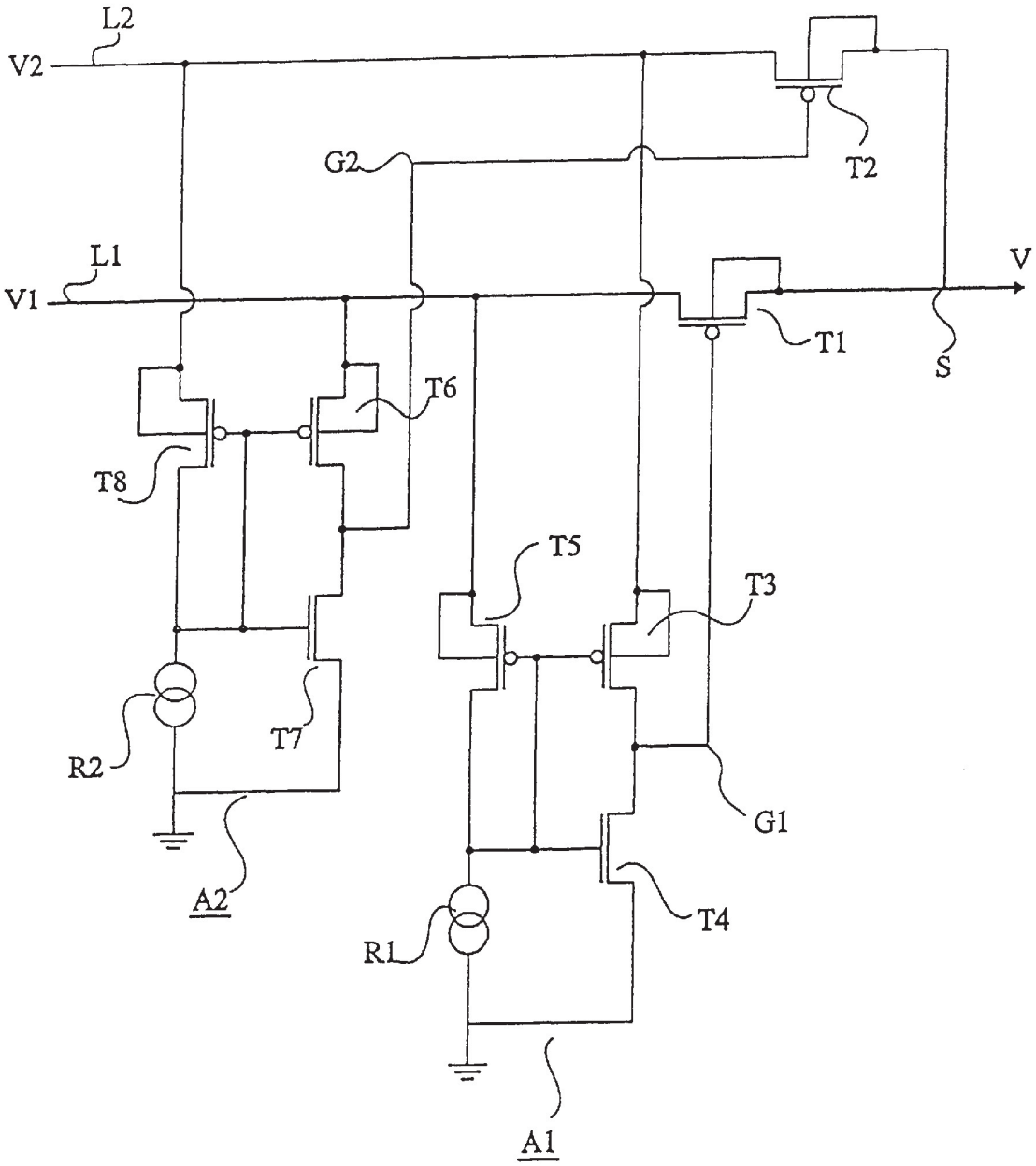



Fig 3

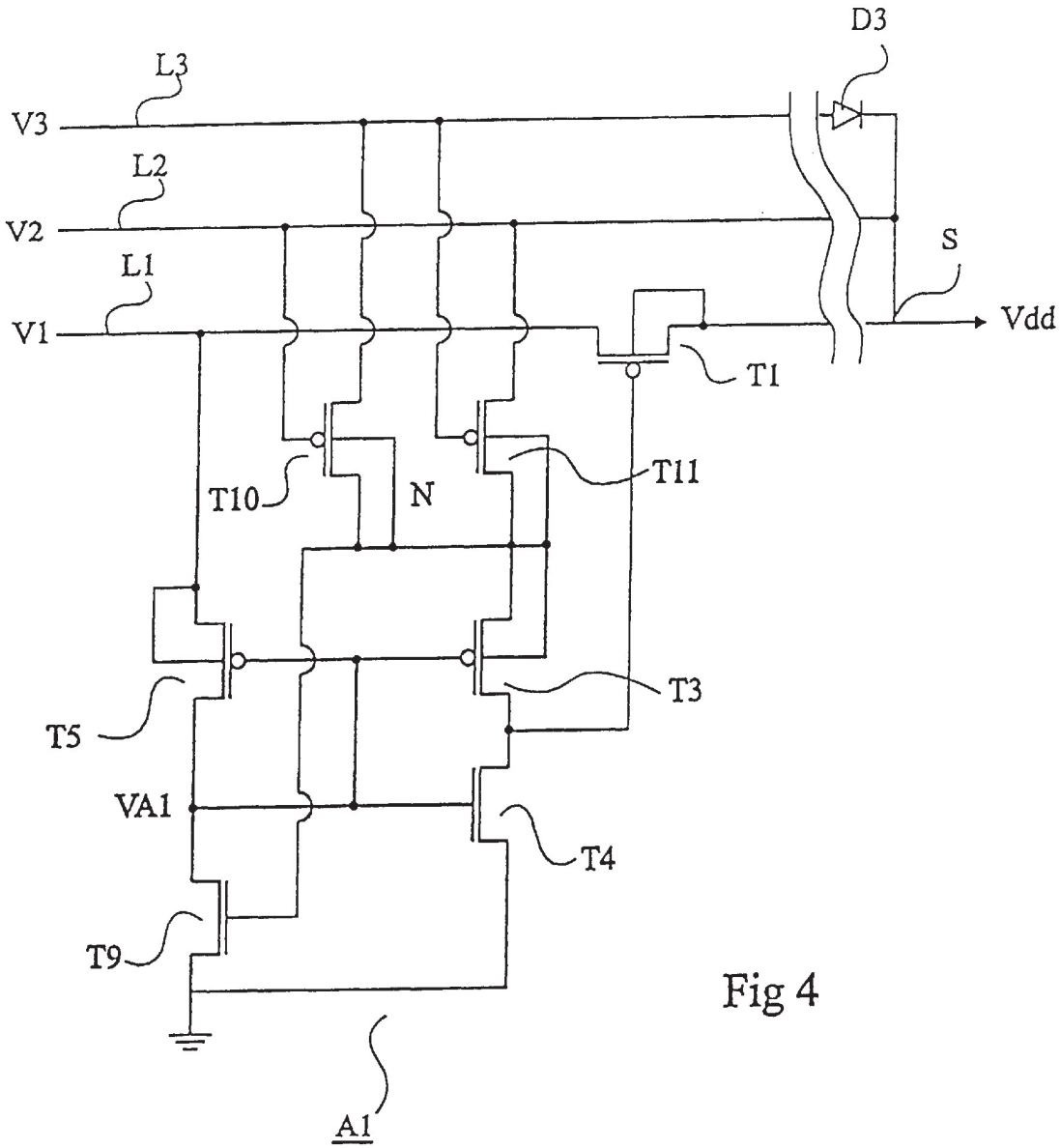



Fig 4

# POWER SUPPLY CIRCUIT WITH A VOLTAGE SELECTOR

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to power supply circuits, and especially to power supply circuits that receive several supply voltages and that select the highest supply voltage. Such power supply circuits are used, for example, in a rechargeable battery device for supplying the device from the battery or from an external power source, if any.

2. Discussion of the Related Art

FIG. **1** shows a conventional power supply circuit receiving two supply voltages V**1** and V**2** on two respective supply lines L**1** and L**2**, and providing a voltage Vdd on an output node S. The two supply lines are connected to the output node by two P-channel MOS transistors (PMOS), respectively T**1** and T**2**. A comparator A**1** has two inputs respectively connected to the two supply lines so that the output of comparator A**1** is at a low level when voltage V**1** is greater than voltage V**2** and at a high level otherwise. The output of comparator A**1** is directly connected to the gate of transistor T**1**, and is connected to the gate of transistor T**2** via an inverter I**1**.

Such power supply circuits are used when it is desired to obtain a small voltage drop between voltage V**1** or V**2** and voltage Vdd. In the cases where a high voltage drop can be tolerated, diodes are used instead of transistors T**1** and T**2**.

FIG. **2**A shows the variation of gate voltages VGI and VG**2** of transistors TI and T**2** for an example of relative variation of supply voltages V**1** and V**2**. Voltage V**1** remains constant while voltage V**2** crosses voltage V**1** as it decreases, then as it increases. It is assumed that comparator A**1** and inverter I**1** are both supplied between voltage Vdd and the ground.

When voltage V**2** exceeds voltage V**1** by a threshold ΔV characteristic of comparator A**1**, voltage VA**1** provided by the comparator is equal to voltage Vdd. Thus, gates G**1** and G**2** are respectively at voltage Vdd and at ground. As a result, transistor T**2** conducts and transistor T**1** is off, transistor T**2** transmitting voltage V**2** on output node S. Similarly, when voltage V**2** is smaller than voltage V**1** by threshold ΔV, voltage VA**1** provided by the comparator is at ground, whereby transistor T**2** is off and transistor T**1** is on, transistor T**1** transmitting voltage V**1** on output node S.

Range ±ΔV is a range in which the comparator, which is by nature imperfect, behaves linearly. The comparator behaves linearly between times t**1** and t**2** when voltage V**2** progressively decreases from voltage V**1**+ΔV to voltage V**1**−ΔV and voltage VG**1** progressively decreases from voltage Vdd to the ground.

Inverter I**1** includes a PMOS transistor and an N-channel MOS transistor (NMOS). The threshold voltage of the PMOS transistor of inverter I**1** is called VTH, which voltage is also that of PMOS transistors T**1** and T**2**. Similarly, the threshold voltage of the NMOS transistor is called VTL.

At a time t**3**, voltage VG**1** is equal to voltage Vdd−VTH, and at a time t**4**, voltage VG**1** reaches voltage VTL. Gate voltage VG**2**, at the output of inverter I**1**, progressively varies between a zero level at time t**3** and a level Vdd at time t**4**.

Transistor T**1** starts conducting when its gate voltage VG**1** reaches voltage Vdd−VTH, that is, at time t**3**.

At a time t**5**, gate voltage VG**2** reaches voltage Vdd−VTH. Transistor T**2** stops conducting at time t**5**.



Thus, there is a range of simultaneous conduction (CS) of transistors T**1** and T**2** between times t**3** and t**5**. There is a similar range of simultaneous conduction CS on either side of a time tr when voltage V**2** becomes greater than voltage V**1** again.

During a simultaneous conduction, the power supply sources generating voltages V**1** and V**2** are shorted, which is not desirable. Further, if the power supply source providing the highest supply voltage exhibits a high impedance, the shorting of the power supply sources results in a drop of the highest supply voltage to the level of the other supply voltage, and comparator A**1** can no longer determine which of the supply voltages is greater. The power supply selection circuit is then blocked in an intermediary state and no longer properly ensures its function.

On the other hand, the principle used in the circuit of FIG. **1** does not enable selecting the highest of three supply voltages or more.

## SUMMARY OF THE INVENTION

An object of the present invention is to provide a circuit for selecting the highest of two supply voltages or more, which can operate without short-circuiting power supply lines.

To achieve this object, as well as others, the present invention provides a power supply circuit receiving several supply voltages on respective power supply lines, each of which is connected to a respective switch, at least one of the switches being a first MOS transistor of a first conductivity type, connected between the associated power supply line and a common output terminal, which includes, for said at least one switch: a second transistor, of the first conductivity type, connected between the gate of the first transistor and a power supply node maintained at the highest of the other supply voltages, a third transistor, of a second conductivity type, which is less conductive in the on state than the second transistor, connected between the gate of the first transistor and a reference potential, and a fourth transistor, of the first conductivity type, having its source connected to the power supply line associated with the switch and its drain connected to the reference potential via a current source, and to the gates of the second, third, and fourth transistors.

According to an embodiment of the present invention, said current source is a fifth transistor, of the second conductivity type, having its gate connected to said power supply node.

According to an embodiment of the present invention, the power supply circuit includes two power supply lines and two respective switches, the power supply node associated with a switch being directly connected to the power supply line associated with the other switch.

According to an embodiment of the present invention, the power supply circuit includes three power supply lines, a sixth transistor connected between the third power supply line and the power supply node, and having its gate connected to the second power supply line, and a seventh transistor connected between the second power supply line and the power supply node and having its gate connected to the third power supply line.

According to an embodiment of the present invention, at least one of the switches is a diode.

According to an embodiment of the present invention, the second transistor has a width-to-length ratio of 20/2, and the third transistor has a W/L ratio of 3/25.

According to an embodiment of the present invention, the fourth transistor has a W/L ratio of 40/2, and the fifth transistor has a W/L ratio of 3/50.

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