

A 50MHz Bandwidth Multi-Mode PA Supply Modulator for GSM, EDGE and UMTS Application

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Abstract — This paper describes the design and measurement results of a supply modulator for a PA for GSM, EDGE and UMTS application. The modulator combines a high-bandwidth class-AB linear regulator with an efficient DC/DC converter in a master-slave configuration. The DC/DC converter is current-mode controlled and has been designed to operate at switching frequencies between 1MHz and 25MHz. A damped dual-inductor LCR filter has been inserted in the output branch of the DC/DC converter for ripple suppression. The chip has been fabricated in a 0.25 μ m CMOS process with an additional gate oxide for 6V transistors and has an active area of 1.5mm². It achieves a bandwidth of 50MHz (for UMTS) with a peak output power of 3.2W (for GSM) and output rms ripple of less than 4mV.

Index Terms — current-mode control, DC/DC converter, EDGE, envelope tracking, GSM, linear regulator, polar modulation, slope compensation, UMTS.

I. INTRODUCTION

The demand for higher data rates in limited available bandwidth has led to the use of non-constant-envelope modulation schemes in various wireless communication systems. In order to meet stringent signal-quality requirements at the antenna, the transmitter needs to be sufficiently linear. Conventionally this is achieved by operating the PA in ‘back-off’, leading to a lower efficiency than available at maximum saturated output power. To increase efficiency, transmitter architectures like envelope tracking and polar modulation have been developed, based on modulating the supply voltage of the PA. For this purpose, an efficient supply modulator with sufficient bandwidth is needed.

High-efficiency voltage conversion can be obtained with a switched-mode inductive DC/DC buck converter, but its bandwidth is limited due to practical limits to the switching frequency. Alternatively, linear regulators enable higher bandwidth at the cost of efficiency. As a good compromise between efficiency and bandwidth, hybrid supply modulators have been proposed combining a switched-mode DC/DC converter in parallel to a linear regulator [1],[2]. One reported hybrid supply modulator achieves 10MHz bandwidth for an EDGE polar transmitter [1], whereas

another one achieves 20MHz bandwidth for a WLAN envelope-tracking PA [2].

With the increase in the number of available wireless communication standards, mobile devices have become available that combine several of these standards in one terminal. To reduce system complexity, multi-mode building blocks that can handle various standards using a single circuit are attractive. Therefore, this paper focuses on a multi-mode hybrid supply modulator suitable for use in GSM, EDGE and UMTS modes, as opposed to the single-mode supply modulators reported earlier [1],[2]. As a result, the combination of possible UMTS application and polar modulation leads to a bandwidth target [3] of 50MHz for the supply modulator, which is higher than that of earlier results [1],[2].

Section II describes the supply-modulator architecture. Section III discusses the linear-regulator design, and section IV concentrates on the DC/DC converter. Section V addresses the design of the complete IC and section VI describes obtained measurement results.

II. SUPPLY-MODULATOR ARCHITECTURE

The supply-modulator topology is shown in Fig. 1 [1], [2],[4],[5]. It contains a linear regulator and a DC/DC converter in master-slave configuration. The linear regulator is formed by a Miller-compensated two-stage amplifier built with class-A input transconductor g_m and class-AB output transconductor g_o . A sensing resistor in the output branch of the linear regulator [2] would require a high common-mode rejection in the sensing amplifier. Instead, a scaled class-AB output stage $g_{o,c}$ is used to generate a control signal for the DC/DC converter. The output current of $g_{o,c}$ is a scaled estimate of the linear regulator output current and is integrated by the capacitor C_{int} . The capacitor voltage can only be finite if the average current supplied by the copy output stage is zero, which implies that the average linear regulator output current is zero as well. Hence the DC/DC converter supplies the DC and low-frequency part of the load current, and the linear regulator supplies the high-frequency part.

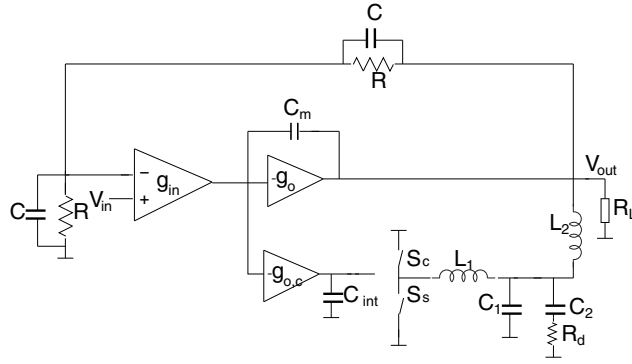


Fig. 1. Supply-modulator topology.

For frequencies below the DC/DC converter bandwidth, the DC/DC converter with its output filter acts as a transconductor g_{DCDC} , converting a control voltage across the integrating capacitor C_{int} into an output current through inductor L_2 . The crossover frequency where the contributions to the load current by DC/DC converter and by linear regulator are equal is

$$f_x = \frac{g_{DCDC}}{2\pi C_{int}} \frac{g_{o,c}}{g_o}. \quad (1)$$

Its value was chosen to be 200kHz.

A closed-loop bandwidth of 50MHz is targeted for UMTS polar modulation experiments [3]. A feedback network with an attenuation factor of $\frac{1}{2}$ is used. The gain-bandwidth product of the supply-modulator is

$$GB = \frac{g_{in}}{2\pi C_m} \frac{g_o R_L}{1 + g_o R_L}. \quad (2)$$

Its target value is 100MHz at a load resistance of 10 Ω .

A simple single-inductor and single-capacitor filter cannot meet the bandwidth and output-ripple requirements simultaneously. Therefore a dual-inductor filter containing inductors L_1 , L_2 and capacitor C_2 is used. Resonant currents in the inductors are damped by adding a resistor R_d in series with the capacitor C_2 . Capacitor C_1 of lower value than C_2 is added to improve ripple suppression [6].

III. DESIGN OF THE LINEAR REGULATOR

Fig. 2 shows a simplified circuit diagram of the linear regulator. The input stage is a class-A folded-cascode amplifier with a tail current of 3mA. The output stage is a rail-to-rail class-AB common-source amplifier. Clamping techniques are applied to prevent the output transistors from cutting off [7], thus reducing crossover distortion at high frequencies. Two capacitors are inserted for Miller frequency compensation. A scaled copy output stage is

added as discussed in section II. The layouts of the copy output transistors (1) and power transistors (m) are built using the same unit cells for matching considerations.

The voltage gain of the output stage is $g_o R_L$, where R_L is the resistive part of the load impedance. The output stage transconductance g_o depends on the currents through the output transistors; it is lowest in the quiescent situation and can be above 1A/V for output currents of several hundreds of milliamps. The load resistance R_L can be as low as 3 Ω in the peak-power GSM case, 9 Ω in the peak-power UMTS case and can exceed 200 Ω in the low-power UMTS case. In order to minimize the effects of these variations on the closed-loop bandwidth indicated by (2) and to avoid feedback stability problems, the quiescent current of the class-AB stage has been chosen to be several tens of milliamps. This design choice reduces the efficiency. The authors see this as a consequence of the multi-mode application, which distinguishes this paper from single-mode modulators [1],[2].

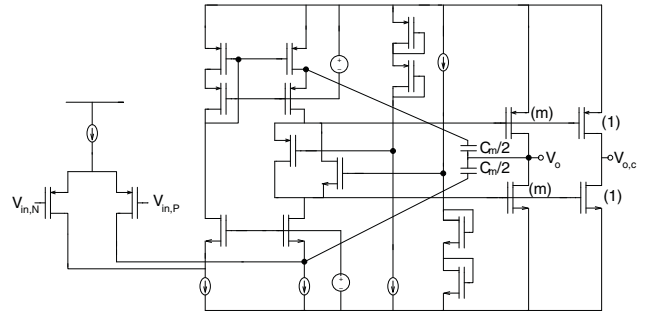


Fig. 2. Linear regulator with copy output stage.

IV. DESIGN OF THE DC/DC CONVERTER

The bandwidth of the DC/DC converter should be larger than the crossover frequency of 200kHz. To achieve the highest possible bandwidth for a given switching frequency, fixed-frequency peak current-mode control was selected.

The current-mode control loop is shown in Fig.3. At the positive edge of the clock, the NMOST is disabled and the PMOST is activated. Break-before-make logic avoids cross-conduction. A transconductor g_4 converts the input voltage across the integrating capacitor to control current $i_{control}$. A slope-compensation current i_{sc} is subtracted from $i_{control}$ to allow for duty cycles above 50% [8]. The slope-compensation current develops quadratically over the switching cycle, and is adapted to the switching frequency (1-25MHz) by a separate control loop. The resulting current is conducted by the sense MOST which is scaled with respect to the power PMOST by a factor m. The resulting DC/DC converter transconductance is $g_{DCDC} = m \cdot g_4$.

A fast comparator trips when the drain-source voltage of the power PMOST exceeds that of the sense MOST. Then the logic turns off the power PMOST and subsequently turns on the power NMOST obeying the break-before-make principle.

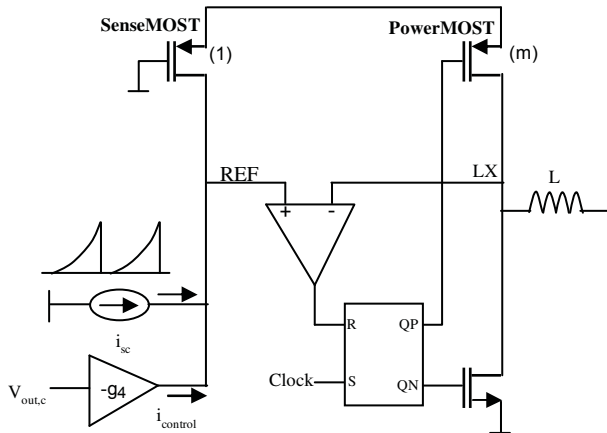


Fig. 3. DC/DC converter with peak current-mode control.

Each power transistor is sub-divided into 6 identical unit transistors. An external 2-bit control signal selects whether 2, 4 or 6 transistor pairs are activated.

V. DESIGN OF THE COMPLETE IC

Fig. 4 shows a micrograph of the 4mm^2 chip fabricated in a $0.25\mu\text{m}$ CMOS process with an additional gate oxide for 6V transistors. The active area is 1.5mm^2 . In the DC/DC converter, the total gate width of the power PMOST is 115mm and that of the NMOST is 60mm .

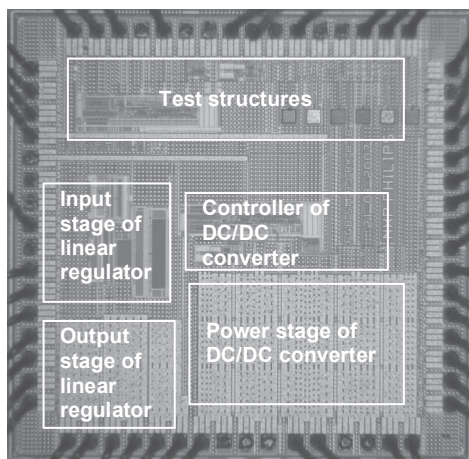


Fig. 4. Die photograph of the supply-modulator IC.

VI. MEASUREMENT RESULTS

Both the DC/DC converter and the linear regulator have their own supply bond-pads and supply-decoupling capacitors on the PCB. Each of these supplies has been connected to the common PCB supply by beads-on-wire each with a 1Ω damping resistor in parallel. The two inductors in the damped LCR filter have been physically separated on the PCB to avoid magnetic coupling.

Fig. 5 shows the measured efficiency of the DC/DC converter alone, at 4V supply and 1V, 2V and 3V DC output levels at 10MHz switching frequency. At 3V output a maximum efficiency of 89% is achieved at 0.6A of output current. Maximum switching frequency for 4V to 2V conversion is more than 30MHz

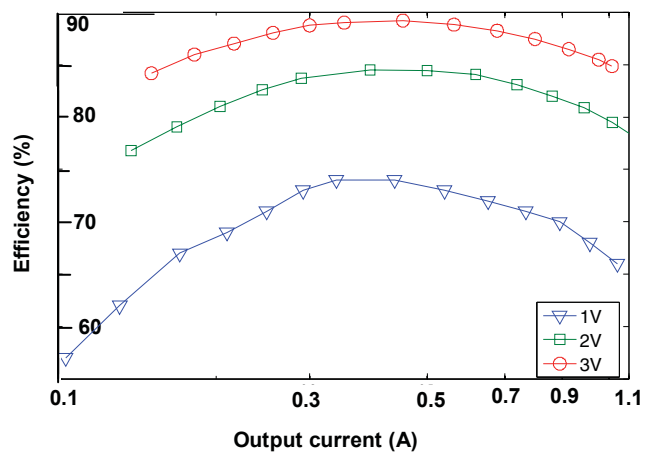


Fig. 5. Measured efficiency of the DC/DC converter at various output voltages.

Fig. 6 shows the measured efficiency of the hybrid modulator at 4V supply and 2V and 3V DC output levels at 10MHz switching frequency. A maximum efficiency of 79% is achieved at 3V output voltage and 0.8A of load current. The high quiescent current of the linear regulator reduces the efficiency with respect to that of the DC/DC converter.

Fig. 7 shows the measured closed-loop voltage gain of the supply modulator at load resistances of 3Ω , 10Ω and 50Ω . A low-frequency gain of 6dB is achieved. Unintended RC feedback-attenuator mismatch causes the gain at 3MHz to be slightly higher than 6dB. At a 10Ω load a -3dB bandwidth exceeding 50MHz is measured.

Fig. 8 shows the measured rms output spectrum at a switching frequency of 5MHz. First harmonic switching ripple is less than 4mV rms, which is comparable to that reported in [1]. Suppression of 2nd and 3rd-order harmonics is as designed. 4th and higher-order harmonics are less than 2.5mV rms and are believed to be caused by either parasitic magnetic coupling on the PCB or substrate coupling in the chip.

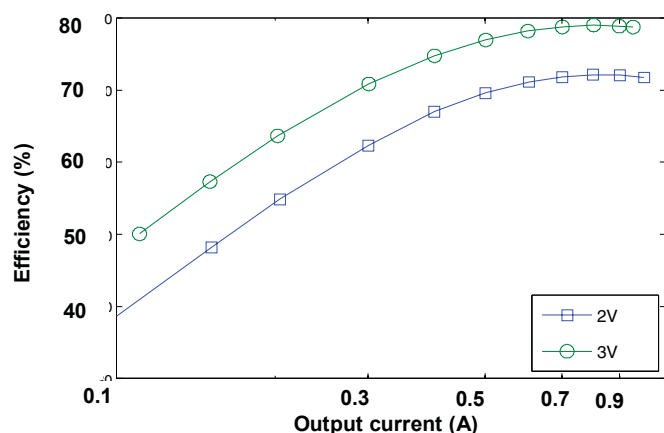


Fig. 6. Measured modulator efficiency at 2V, 3V DC output.

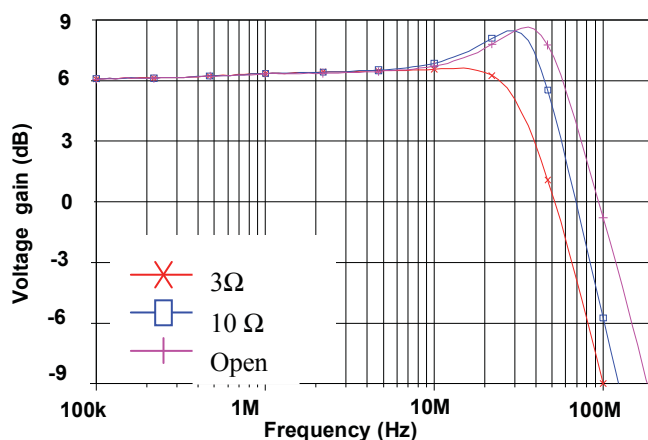


Fig. 7. Measured voltage gain of hybrid supply modulator at different load resistances.

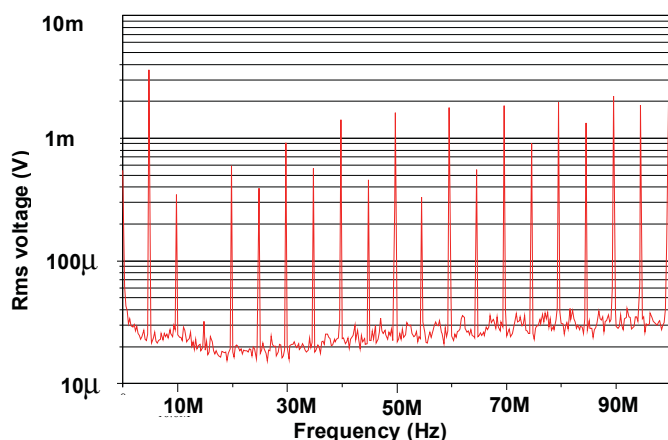


Fig. 8. Measured output spectrum of the supply modulator .

TABLE I
SUMMARY OF PERFORMANCE

-3dB Bandwidth	50MHz
Switching Frequency	5MHz-10MHz
DC/DC converter Efficiency	89% @ 10MHz
Hybrid Modulator Efficiency	79% @ 10MHz
Output rms Ripple	< 4mV
Peak output power	3.2W
Mobile Standards	GSM, EDGE, UMTS

VII. CONCLUSION

A multi-mode supply modulator with 50MHz bandwidth has been realized for GSM, EDGE and UMTS standards. An rms ripple voltage of less than 4mV has been achieved. The requirement of being able to drive the PA at maximum output power or at low output power, while maintaining the 50MHz bandwidth requirement for UMTS, implies a large quiescent current in the output stage of the linear regulator, which affects overall efficiency.

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