[DOCKET NO. 101005]

LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

BACKGROUND

I. Field

[0001] The present disclosure relates generally to electronics, and more specifically to techniques for generating a power supply for an amplifier and/or other circuits.

II. Background

[0002] In a communication system, a transmitter may process (e.g., encode and modulate) data to generate output samples. The transmitter may further condition (e.g., convert to analog, filter, frequency upconvert, and amplify) the output samples to generate an output radio frequency (RF) signal. The transmitter may then transmit the output RF signal via a communication channel to a receiver. The receiver may receive the transmitted RF signal and perform the complementary processing on the received RF signal to recover the transmitted data.

[0003] The transmitter typically includes a power amplifier (PA) to provide high transmit power for the output RF signal. The power amplifier should be able to provide high output power and have high power-added efficiency (PAE). Furthermore, the power amplifier may be required to have good performance and high PAE even with a low battery voltage.

SUMMARY

[0004] Techniques for efficiently generating a power supply for a power amplifier and/or other circuits are described herein. In one exemplary design, an apparatus (e.g., an integrated circuit, a wireless device, a circuit module, etc.) may include an envelope amplifier and a boost converter. The boost converter may receive a first supply voltage (e.g., a battery voltage) and generate a boosted supply voltage having a higher voltage than the first supply voltage. The envelope amplifier may receive an envelope signal and the boosted supply voltage and may generate a second supply voltage based on the envelope signal and the boosted supply voltage. The apparatus may further include a power amplifier, which may operate based on the second supply voltage from the envelope amplifier. In one design, the envelope amplifier may further receive the first supply voltage and may generate the second supply voltage based on either the first

supply voltage or the boosted supply voltage. For example, the envelope amplifier may generate the second supply voltage (i) based on the boosted supply voltage if the envelope signal exceeds a first threshold and/or if the first supply voltage is below a second threshold or (ii) based on the first supply voltage otherwise.

[0005] In another exemplary design, an apparatus may include a switcher, an envelope amplifier, and a power amplifier. The switcher may receive a first supply voltage (e.g., a battery voltage) and provide a first supply current. The envelope amplifier may receive an envelope signal and provide a second supply current based on the envelope signal. The power amplifier may receive a total supply current comprising the first supply current and the second supply current. The first supply current may include direct current (DC) and low frequency components. The second supply current may include higher frequency components. The apparatus may further include a boost converter, which may receive the first supply voltage and provide a boosted supply voltage. The envelope amplifier may then operate based on either the first supply voltage or the boosted supply voltage.

[0006] In yet another exemplary design, an apparatus may include a switcher that may sense an input current and generate a switching signal to charge and discharge an inductor providing a supply current. The switcher may add an offset to the input current to generate a larger supply current than without the offset. The apparatus may further include an envelope amplifier, a boost converter, and a power amplifier, which may operate as described above.

[0007] Various aspects and features of the disclosure are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 shows a block diagram of a wireless communication device.

[0009] FIGS. 2A, 2B and 2C show diagrams of operating a power amplifier based on a battery voltage, an average power tracker, and an envelope tracker, respectively.

[0010] FIG. 3 shows a schematic diagram of a switcher and an envelope amplifier.

[0011] FIGS. 4A, 4B and 4C show plots of PA supply current and inductor current versus time for different supply voltages for the switcher and the envelope amplifier.

[0012] FIG. 5 shows a schematic diagram of a switcher with offset in a current sensing path.

[0013] FIG. 6 shows a schematic diagram of a boost converter.

DETAILED DESCRIPTION

[0014] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other designs.

[0015] Techniques for generating a power supply for an amplifier and/or other circuits are described herein. The techniques may be used for various types of amplifiers such as power amplifiers, driver amplifiers, etc. The techniques may also be used for various electronic devices such as wireless communication devices, cellular phones, personal digital assistants (PDAs), handheld devices, wireless modems, laptop computers, cordless phones, Bluetooth devices, consumer electronic devices, etc. For clarity, the use of the techniques to generate a power supply for a power amplifier in a wireless communication device is described below.

[0016] **FIG. 1** shows a block diagram of a design of a wireless communication device 100. For clarity, only a transmitter portion of wireless device 100 is shown in FIG. 1, and a receiver portion is not shown. Within wireless device 100, a data processor 110 may receive data to be transmitted, process (e.g., encode, interleave, and symbol map) the data, and provide data symbols. Data processor 110 may also process pilot and provide pilot symbols. Data processor 110 may also process the data symbols and pilot symbols for code division multiple access (CDMA), time division multiple access (TDMA), frequency division multiple access (FDMA), orthogonal FDMA (OFDMA), single-carrier FDMA (SC-FDMA), and/or some other multiplexing scheme and may provide output symbols.

[0017] A modulator 112 may receive the output symbols from data processor 110, perform quadrature modulation, polar modulation, or some other type of modulation, and provide output samples. Modulator 112 may also determine the envelope of the output samples, e.g., by computing the magnitude of each output sample and averaging the magnitude across output samples. Modulator 112 may provide an envelope signal indicative of the envelope of the output samples.

[0018] An RF transmitter 120 may process (e.g., convert to analog, amplify, filter, and frequency upconvert) the output samples from modulator 112 and provide an input RF signal (RFin). A power amplifier (PA) 130 may amplify the input RF signal to obtain the desired output power level and provide an output RF signal (RFout), which may be transmitted via an antenna (not shown in FIG. 1). RF transmitter 120 may also include

circuits to generate the envelope signal, instead of using modulator 112 to generate the envelope signal.

[0019] A PA supply generator 150 may receive the envelope signal from modulator 112 and may generate a power supply voltage (Vpa) for power amplifier 130. PA supply generator 150 may also be referred to as an envelope tracker. In the design shown in FIG. 1, PA supply generator 150 includes a switcher 160, an envelope amplifier (Env Amp) 170, a boost converter 180, and an inductor 162. Switcher 160 may also be referred to as a switching-mode power supply (SMPS). Switcher 160 receives a battery voltage (Vbat) and provides a first supply current (Iind) comprising DC and low frequency components at node A. Inductor 162 stores current from switcher 160 and provides the stored current to node A on alternating cycles. Boost converter 180 receives the Vbat voltage and generates a boosted supply voltage (Vboost) that is higher than the Vbat voltage. Envelope amplifier 170 receives the envelope signal at its signal input, receives the Vbat voltage and the Vboost voltage at its two power supply inputs, and provides a second supply current (Ienv) comprising high frequency components at node A. The PA supply current (Ipa) provided to power amplifier 130 includes the Iind current from switcher 160 and the Ienv current from envelope amplifier 170. Envelope amplifier 170 also provides the proper PA supply voltage (Vpa) at Node A for power amplifier 130. The various circuits in PA supply generator 150 are described in further detail below.

[0020] A controller 140 may control the operation of various units within wireless device 100. A memory 142 may store program codes and data for controller 140 and/or other units within wireless device 100. Data processor 110, modulator 112, controller 140, and memory 142 may be implemented on one or more application specific integrated circuits (ASICs) and/or other ICs.

[0021] FIG. 1 shows an exemplary design of wireless device 100. Wireless device 100 may also be implemented in other manners and may include different circuits than those shown in FIG. 1. All or a portion of RF transmitter 120, power amplifier 130, and PA supply generator 150 may be implemented on one or more analog integrated circuits (ICs), RF ICs (RFICs), mixed-signal ICs, etc.

[0022] It may be desirable to operate wireless device 100 with a low battery voltage in order to reduce power consumption, extend battery life, and/or obtain other advantages. New battery technology may be able to provide energy down to 2.5 volts (V) and below in the near future. However, a power amplifier may need to operate with a PA supply

voltage (e.g., 3.2V) that is higher than the battery voltage. A boost converter may be used to boost the battery voltage to generate the higher PA supply voltage. However, the use of the boost converter to directly supply the PA supply voltage may increase cost and power consumption, both of which are undesirable.

[0023] PA supply generator 150 can efficiently generate the PA supply voltage with envelope tracking to avoid the disadvantages of using a boost converter to directly provide the PA supply voltage. Switcher 160 may provide the bulk of the power for power amplifier 130 and may be connected directly to the battery voltage. Boost converter 180 may provide power to only envelope amplifier 170. PA supply generator 150 can generate the PA supply voltage to track the envelope of the RFin signal provided to power amplifier 130, so that just the proper amount of PA supply voltage is supplied to power amplifier 130.

[0024] **FIG. 2A** shows a diagram of using a battery voltage for a power amplifier 210. The RFout signal (which follows the RFin signal) has a time-varying envelope and is shown by a plot 250. The battery voltage is shown by a plot 260 and is higher than the largest amplitude of the envelope in order to avoid clipping of the RFout signal from power amplifier 210. The difference between the battery voltage and the envelope of the RFout signal represents wasted power that is dissipated by power amplifier 210 instead of delivered to an output load.

[0025] **FIG. 2B** shows a diagram of generating a PA supply voltage (Vpa) for power amplifier 210 with an average power tracker (APT) 220. APT 220 receives a power control signal indicating the largest amplitude of the envelope of the RFout signal in each time interval. APT 220 generates the PA supply voltage (which is shown by a plot 270) for power amplifier 210 based on the power control signal. The difference between the PA supply voltage and the envelope of the RFout signal represents wasted power. APT 220 can reduce wasted power since it can generate the PA supply voltage to track the largest amplitude of the envelope in each time interval.

[0026] **FIG. 2C** shows a diagram of generating a PA supply voltage for power amplifier 210 with an envelope tracker 230. Envelope tracker 230 receives an envelope signal indicative of the envelope of the RFout signal and generates the PA supply voltage (which is shown by a plot 280) for power amplifier 210 based on the envelope signal. The PA supply voltage closely tracks the envelope of the RFout signal over time. Hence, the difference between the PA supply voltage and the envelope of the RFout

signal is small, which results in less wasted power. The power amplifier is operated in saturation for all envelope amplitudes in order to maximize PA efficiency.

[0027] PA supply generator 150 in FIG. 1 can implement envelope tracker 230 in FIG. 2C with high efficiency. This is achieved by a combination of (i) an efficient switcher 160 to generate a first supply current (Iind) with a switch mode power supply and (ii) a linear envelope amplifier 170 to generate a second supply current (Ienv).

[0028] **FIG. 3** shows a schematic diagram of a switcher 160a and an envelope amplifier 170a, which are one design of switcher 160 and envelope amplifier 170, respectively, in FIG. 1. Within envelope amplifier 170a, an operational amplifier (op-amp) 310 has its non-inverting input receiving the envelope signal, its inverting input coupled to an output of envelope amplifier 170a (which is node E), and its output coupled to an input of a class AB driver 312. Driver 312 has its first output (R1) coupled to the gate of a P-channel metal oxide semiconductor (PMOS) transistor 314 and its second output (R2) coupled to the gate of an N-channel MOS (NMOS) transistor 316. NMOS transistor 316 has its drain coupled to node E and its source coupled to circuit ground. PMOS transistor 314 has its drain coupled to node E and its source coupled to the drains of PMOS transistors 318 and 320. PMOS transistor 318 has its gate receiving a C1 control signal and its source receiving the Vboost voltage. PMOS transistor 320 has its gate receiving a C2 control signal and its source receiving the Vbat voltage.

[0029] A current sensor 164 is coupled between node E and node A and senses the Ienv current provided by envelope amplifier 170a. Sensor 164 passes most of the Ienv current to node A and provides a small sensed current (Isen) to switcher 160a. The Isen current is a small fraction of the Ienv current from envelope amplifier 170a.

[0030] Within switcher 160a, a current sense amplifier 330 has its input coupled to current sensor 164 and its output coupled to an input of a switcher driver 332. Driver 332 has its first output (S1) coupled to the gate of a PMOS transistor 334 and its second output (S2) coupled to the gate of an NMOS transistor 336. NMOS transistor 336 has its drain coupled to an output of switcher 160a (which is node B) and its source coupled to circuit ground. PMOS transistor 334 has its drain coupled to node B and its source receiving the Vbat voltage. Inductor 162 is coupled between nodes A and B.

[0031] Switcher 160a operates as follows. Switcher 160a is in an On state when current sensor 164 senses a high output current from envelope amplifier 170a and provides a low sensed voltage to driver 332. Driver 332 then provides a low voltage to the gate of PMOS transistor 334 and a low voltage to the gate of NMOS transistor 336. PMOS

transistor 334 is turned on and couples the Vbat voltage to inductor 162, which stores energy from the Vbat voltage. The current through inductor 162 rises during the On state, with the rate of the rise being dependent on (i) the difference between the Vbat voltage and the Vpa voltage at node A and (ii) the inductance of inductor 162. Conversely, switcher 160a is in an Off state when current sensor 164 senses a low output current from envelope amplifier 170a and provides a high sensed voltage to driver 332. Driver 332 then provides a high voltage to the gate of PMOS transistor 334 and a high voltage to the gate of NMOS transistor 336. NMOS transistor 336 is turned on, and inductor 162 is coupled between node A and circuit ground. The current through inductor 162 falls during the Off state, with the rate of the fall being dependent on the Vpa voltage at node A and the inductance of inductor 162. The Vbat voltage thus provides current to power amplifier 130 via inductor 162 during the On state, and inductor 120 provides its stored energy to power amplifier 130 during the Off state.

[0032] In one design, envelope amplifier 170a operates based on the Vboost voltage only when needed and based on the Vbat voltage the remaining time in order to improve efficiency. For example, envelope amplifier 170a may provide approximately 85% of the power based on the Vbat voltage and only approximately 15% of the power based on the Vboost voltage. When a high Vpa voltage is needed for power amplifier 130 due to a large envelope on the RFout signal, the C1 control signal is at logic low, and the C2 control signal is at logic high. In this case, boost converter 180 is enabled and generates the Vboost voltage, PMOS transistor 318 is turned on and provides the Vboost voltage to the source of PMOS transistor 314, and PMOS transistor 320 is turned off. Conversely, when a high Vpa voltage is not needed for power amplifier 130, the C1 control signal is at logic high, and the C2 control signal is at logic low. In this case, boost converter 180 is disabled, PMOS transistor 318 is turned off, and PMOS transistor 320 is turned on and provides the Vbat voltage to the source of PMOS transistor 314.

[0033] Envelope amplifier 170a operates as follows. When the envelope signal increases, the output of op-amp 310 increases, the R1 output of driver 312 deceases and the R2 output of driver 312 decreases until NMOS transistor 316 is almost turned off, and the output of envelope amplifier 170a increases. The converse is true when the envelope signal decreases. The negative feedback from the output of envelope amplifier 170a to the inverting input of op-amp 310 results in envelope amplifier 170a having unity gain. Hence, the output of envelope amplifier 170a follows the envelope signal, and the Vpa voltage is approximately equal to the envelope signal. Driver 312

may be implemented with a class AB amplifier to improve efficiency, so that large output currents can be supplied even though the bias current in transistors 314 and 316 is very low.

[0034] A control signal generator 190 receives the envelope signal and the Vbat voltage and generates the C1 and C2 control signals. The C1 control signal is complementary to the C2 control signal. In one design, generator 190 generates the C1 and C2 control signals to select the Vboost voltage for envelope amplifier 170 when the magnitude of the envelope signal exceeds a first threshold. The first threshold may be a fixed threshold or may be determined based on the Vbat voltage. In another design, generator 190 generates the C1 and C2 control signals to select the Vboost voltage for envelope amplifier 170 when the magnitude of the envelope signal exceeds the first threshold and the Vbat voltage is below a second threshold. Generator 190 may also generate the C1 and C2 signals based on other signals, other voltages, and/or other criteria.

[0035] FIG. 3 shows an exemplary design of switcher 160 and envelope amplifier 170 in FIG. 1. Switcher 160 and envelope amplifier 170 may also be implemented in other manners. For example, envelope amplifier 170 may be implemented as described in U.S. Patent No. 6,300,826, entitled "Apparatus and Method for Efficiently Amplifying Wideband Envelope Signals," issued October 9, 2001.

[0036] Switcher 160a has high efficiency and delivers a majority of the supply current for power amplifier 130. Envelope amplifier 170a operates as a linear stage and has relatively high bandwidth (e.g., in the MHz range). Switcher 160a operates to reduce the output current from envelope amplifier 170a, which improves overall efficiency.

[0037] It may be desirable to support operation of wireless device 100 with a low battery voltage (e.g., below 2.5V). This may be achieved by operating switcher 160 based on the Vbat voltage and operating envelope amplifier 170 based on the higher Vboost voltage. However, efficiency may be improved by operating envelope amplifier 170 based on the Vboost voltage only when needed for large amplitude envelope and based on the Vbat voltage the remaining time, as shown in FIG. 3 and described above.

[0038] **FIG. 4A** shows plots of an example of the PA supply current (Ipa) and the inductor current (Iind) from inductor 162 versus time for a case in which switcher 160a has a supply voltage (Vsw) of 3.7V and envelope amplifier 170a has a supply voltage (Venv) of 3.7V. The Iind current is the current through inductor 162 and is shown by a plot 410. The Ipa current is the current provided to power amplifier 130 and is shown by a plot 420. The Ipa current includes the Iind current as well as the Ienv current from

envelope amplifier 170a. Envelope amplifier 170a provides output current whenever the Ipa current is higher than the Iind current. The efficiency of switcher 160a and envelope amplifier 170a is approximately 80% in one exemplary design.

[0039] **FIG. 4B** shows plots of the PA supply current (Ipa) and the inductor current (Iind) versus time for a case in which switcher 160a has a supply voltage of 2.3V and envelope amplifier 170a has a supply voltage of 3.7V. The Iind current is shown by a plot 412, and the Ipa current is shown by plot 420. When the supply voltage of switcher 160a is reduced to 2.3V, inductor 162 charges more slowly, which results in a lower average Iind current as compared to the case in which the supply voltage of switcher 160a is at 3.7V in FIG. 4A. The lower Iind current causes envelope amplifier 170a to provide more of the Ipa current. This reduces the overall efficiency to approximately 65% in one exemplary design because envelope amplifier 170a is less efficient than switcher 160a. The drop in efficiency may be ameliorated by increasing the Iind current from the switcher.

[0040] **FIG. 5** shows a schematic diagram of a switcher 160b, which is another design of switcher 160 in FIG. 1. Switcher 160b includes current sense amplifier 330, driver 332, and MOS transistors 334 and 336, which are coupled as described above for switcher 160a in FIG. 3. Switcher 160b further includes a current summer 328 having a first input coupled to current sensor 164, a second input receiving an offset (e.g., an offset current), and an output coupled to the input of current sense amplifier 330. Summer 328 may be implemented with a summing circuit (e.g., an amplifier), a summing node, etc.

[0041] Switcher 160b operates as follows. Summer 328 receives the Isen current from current sensor 164, adds an offset current, and provides a summed current that is lower than the Isen current by the offset current. The remaining circuits within switcher 160b operate as described above for switcher 160a in FIG. 3. Summer 328 intentionally reduces the Isen current provided to current sense amplifier 330, so that switcher 160 is turned On for a longer time period and can provide a larger Iind current, which is part of the Ipa current provided to power amplifier 130. The offset provided to summer 328 determines the amount by which the Iind current is increased by switcher 160b relative to the Iind current provided by switcher 160a in FIG. 3.

[0042] In general, a progressively larger offset may be used to generate a progressively larger inductor current than without the offset. In one design, the offset may be a fixed value selected to provide good performance, e.g., good efficiency. In another design,

the offset may be determined based on the battery voltage. For example, a progressively larger offset may be used for a progressively lower battery voltage. The offset may also be determined based on the envelope signal and/or other information.

[0043] An offset to increase the inductor current may be added via summer 328, as shown in FIG. 5. An offset may also be added by increasing the pulse width of an output signal from current sense amplifier via any suitable mechanism.

[0044] **FIG. 4C** shows plots of the PA supply current (Ipa) and the inductor current (Iind) versus time for a case in which switcher 160b in FIG. 5 has a supply voltage of 2.3V and envelope amplifier 170a has a supply voltage of 3.7V. The Iind current is shown by a plot 414, and the Ipa current is shown by plot 420. When the supply voltage of switcher 160b is reduced to 2.3V, inductor 162 charges more slowly, which results in a lower Iind current as shown in FIG. 4B. The offset added by summer 328 in FIG. 5 reduces the sensed current provided to current sense amplifier 330 and results in switcher 160b being turned On longer. Hence, switcher 160b with offset in FIG. 5 can provide a higher Iind current than switcher 160a without offset in FIG. 3. The overall efficiency for switcher 160b and envelope amplifier 170a is improved to approximately 78% in one exemplary design.

[0045] **FIG. 6** shows a schematic diagram of a design of boost converter 180 in FIGS. 1, 3 and 5. Within boost converter 180, an inductor 612 has one end receiving the Vbat voltage and the other end coupled to node D. An NMOS transistor 614 has its source coupled to circuit ground, its gate receiving a Cb control signal, and its drain coupled to node D. A diode 616 has its anode coupled to node D and its cathode coupled to the output of boost converter 180. A capacitor 618 has one end coupled to circuit ground and the other end coupled to the output of boost converter 180.

[0046] Boost converter 180 operates as follows. In an On state, NMOS transistor 614 is closed, inductor 612 is coupled between the Vbat voltage and circuit ground, and the current via inductor 612 increases. In an Off state, NMOS transistor 614 is opened, and the current from inductor 612 flows via diode 616 to capacitor 618 and a load at the output of boost converter 180 (not shown in FIG. 6). The Vboost voltage may be expressed as:

$$\text{Vboost} = \text{Vbat} \cdot \frac{1}{1 - \text{Duty\_Cycle}}, \qquad \text{Eq (1)}$$

where Duty_Cycle is the duty cycle in which NMOS transistor 614 is turned on. The duty cycle may be selected to obtain the desired Vboost voltage and to ensure proper operation of boost converter 180.

[0047] The techniques described herein enable an envelope tracker to operate at a lower battery voltage (e.g., 2.5V or lower). The envelope tracker includes switcher 160 and envelope amplifier 170 for the design shown in FIG. 1. In one design of supporting operation with a lower battery voltage, as shown in FIG. 3, switcher 160 is connected to the Vbat voltage and envelope amplifier 170 is connected to either the Vbat voltage or the Vboost voltage. Switcher 160 provides power most of the time, and envelope amplifier 170 provides power during peaks in the envelope of the RFout signal. The overall efficiency of the envelope tracker is reduced by the efficiency of boost converter 180 (which may be approximately 85%) only during the time in which envelope amplifier 170 provides power.

[0048] In another design of supporting operation with a lower battery voltage, the entire envelope tracker is operated based on the Vboost voltage from boost converter 180. In this design, boost converter 180 provides high current required by power amplifier 130 (which may be more than one Ampere), and efficiency is reduced by the efficiency of boost converter 180 (which may be approximately 85%).

[0049] In yet another design of supporting operation with a lower battery voltage, a field effect transistor (FET) switch is used to connect the envelope tracker to (i) the Vbat voltage when the Vbat voltage is greater than a Vthresh voltage or (ii) the Vboost voltage when the Vbat voltage is less than the Vthresh voltage. Efficiency would then be reduced by losses in the FET switch. However, better efficiency may be obtained for envelope amplifier 170 due to a lower input voltage.

[0050] In one exemplary design, an apparatus (e.g., an integrated circuit, a wireless device, a circuit module, etc.) may comprise an envelope amplifier and a boost converter, e.g., as shown in FIGS. 1 and 3. The boost converter may receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage. The first supply voltage may be a battery voltage, a line-in voltage, or some other voltage available to the apparatus. The envelope amplifier may receive an envelope signal and the boosted supply voltage and may generate a second supply voltage (e.g., the Vpa voltage in FIG. 3) based on the envelope signal and the boosted supply voltage. The apparatus may further comprise a power amplifier, which may

operate based on the second supply voltage from the envelope amplifier. The power amplifier may receive and amplify an input RF signal and provide an output RF signal.

[0051] In one design, the envelope amplifier may further receive the first supply voltage and may generate the second supply voltage based on the first supply voltage or the boosted supply voltage. For example, the envelope amplifier may generate the second supply voltage (i) based on the boosted supply voltage if the envelope signal exceeds a first threshold, or if the first supply voltage is below a second threshold, or both or (ii) based on the first supply voltage otherwise.

[0052] In one design, the envelope amplifier may include an op-amp, a driver, a PMOS transistor, and an NMOS transistor, e.g., op-amp 310, driver 312, PMOS transistor 314, and NMOS transistor 316 in FIG. 3. The op-amp may receive the envelope signal and provide an amplified signal. The driver may receive the amplified signal and provide a first control signal (R1) and a second control signal (R2). The PMOS transistor may have a gate receiving the first control signal, a source receiving the boosted supply voltage or the first supply voltage, and a drain providing the second supply voltage. The NMOS transistor may have a gate receiving the second control signal, a drain providing the second supply voltage, and a source coupled to circuit ground. The envelope amplifier may further comprise second and third PMOS transistors (e.g., PMOS transistors 318 and 320). The second PMOS transistor may have a gate receiving a third control signal (C1), a source receiving the boosted supply voltage, and a drain coupled to the source of the PMOS transistor. The third PMOS transistor may have a gate receiving a fourth control signal (C2), a source receiving the first supply voltage, and a drain coupled to the source of the PMOS transistor.

[0053] In another exemplary design, an apparatus (e.g., an integrated circuit, a wireless device, a circuit module, etc.) may comprise a switcher, an envelope amplifier, and a power amplifier, e.g., as shown in FIGS. 1 and 3. The switcher may receive a first supply voltage (e.g., a battery voltage) and provide a first supply current (e.g., the Iind current in FIG. 3). The envelope amplifier may receive an envelope signal and provide a second supply current (e.g., the Ienv current) based on the envelope signal. The power amplifier may receive a total supply current (e.g., the Ipa current) comprising the first supply current and the second supply current. The first supply current may comprise DC and low frequency components. The second supply current may comprise higher frequency components. The apparatus may further comprise a boost converter, which may receive the first supply voltage and provide a boosted supply voltage having

a higher voltage than the first supply voltage. The envelope amplifier may operate based on the first supply voltage or the boosted supply voltage.

[0054] In one design, the switcher may comprise a current sense amplifier, a driver, a PMOS transistor, and an NMOS transistor, e.g., current sense amplifier 330, driver 332, PMOS transistor 334, and NMOS transistor 336 in FIG. 3. The current sense amplifier may sense the first supply current, or the second supply current (e.g., as shown in FIG. 3), or the total supply current and may provide a sensed signal. The driver may receive the sensed signal and provide a first control signal (S1) and a second control signal (S2). The PMOS transistor may have a gate receiving the first control signal, a source receiving the first supply voltage, and a drain providing a switching signal for an inductor providing the first supply current. The NMOS transistor may have a gate receiving the second control signal, a drain providing the switching signal, and a source coupled to circuit ground. The inductor (e.g., inductor 162) may be coupled to the drains of the PMOS transistor and the NMOS transistor, may receive the switching signal at one end, and may provide the first supply current at the other end.

[0055] In yet another exemplary design, an apparatus (e.g., an integrated circuit, a wireless device, a circuit module, etc.) may comprise a switcher, e.g., switcher 160b in FIG. 5. The switcher may sense an input current (e.g., the Ienv current in FIG. 5) and generate a switching signal to charge and discharge an inductor providing a supply current (e.g., the Iind current). The switcher may add an offset to the input current to generate a larger supply current than without the offset. The switcher may operate based on a first supply voltage (e.g., a battery voltage). In one design, the offset may be determined based on the first supply voltage. For example, a larger offset may be used for a smaller first supply voltage, and vice versa.

[0056] In one design, the switcher may comprise a summer, a current sense amplifier, and a driver, e.g., summer 328, current sense amplifier 330, and driver 332 in FIG. 5. The summer may sum the input current and an offset current and provide a summed current. The current sense amplifier may receive the summed current and provide a sensed signal. The driver may receive the sensed signal and provide at least one control signal used to generate the switching signal. In one design, the at least one control signal may comprise a first control signal (S1) and a second control signal (S2), and the switcher may further comprise a PMOS transistor and an NMOS transistor, e.g., PMOS transistor 334 and NMOS transistor 336 in FIG. 5. The PMOS transistor may have a gate receiving the first control signal, a source receiving first supply voltage, and a drain

providing the switching signal. The NMOS transistor may have a gate receiving the second control signal, a drain providing the switching signal, and a source coupled to circuit ground.

[0057] In one design, the apparatus may further comprise an envelope amplifier, a boost converter, and a power amplifier. The envelope amplifier may receive an envelope signal and provide a second supply current (e.g., the Ienv current in FIG. 5) based on the envelope signal. The boost converter may receive the first supply voltage and provide a boosted supply voltage. The envelope amplifier may operate based on the first supply voltage or the boosted supply voltage. The power amplifier may receive a total supply current (e.g., the Ipa current) comprising the supply current from the switcher and the second supply current from the envelope amplifier.

[0058] The circuits (e.g., the envelope amplifier, the switcher, the boost converter, etc.) described herein may be implemented on an IC, an analog IC, an RF IC (RFIC), a mixed-signal IC, an ASIC, a printed circuit board (PCB), an electronic device, etc. The circuits may be fabricated with various IC process technologies such as complementary metal oxide semiconductor (CMOS), NMOS, PMOS, bipolar junction transistor (BJT), bipolar-CMOS (BiCMOS), silicon germanium (SiGe), gallium arsenide (GaAs), etc.

[0059] An apparatus implementing any of the circuits described herein may be a stand-alone device or may be part of a larger device. A device may be (i) a stand-alone IC, (ii) a set of one or more ICs that may include memory ICs for storing data and/or instructions, (iii) an RFIC such as an RF receiver (RFR) or an RF transmitter/receiver (RTR), (iv) an ASIC such as a mobile station modem (MSM), (v) a module that may be embedded within other devices, (vi) a receiver, cellular phone, wireless device, handset, or mobile unit, (vii) etc.

[0060] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

[0061] **WHAT IS CLAIMED IS:**

CLAIMS

1. An apparatus comprising:

a boost converter operative to receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage; and

an envelope amplifier operative to receive an envelope signal and the boosted supply voltage and generate a second supply voltage based on the envelope signal and the boosted supply voltage.

2. The apparatus of claim 1, wherein the envelope amplifier is operative to further receive the first supply voltage and generate the second supply voltage based on the first supply voltage or the boosted supply voltage.

3. The apparatus of claim 2, wherein the envelope amplifier is operative to generate the second supply voltage based on the boosted supply voltage if the envelope signal exceeds a first threshold, or if the first supply voltage is below a second threshold, or both.

4. The apparatus of claim 2, wherein the envelope amplifier comprises

an operational amplifier (op-amp) operative to receive the envelope signal and provide an amplified signal,

a driver operative to receive the amplified signal and provide a first control signal and a second control signal,

a P-channel metal oxide semiconductor (PMOS) transistor having a gate receiving the first control signal, a source receiving the boosted supply voltage or the first supply voltage, and a drain providing the second supply voltage, and

an N-channel metal oxide semiconductor (NMOS) transistor having a gate receiving the second control signal, a drain providing the second supply voltage, and a source coupled to circuit ground.

5. The apparatus of claim 4, wherein the envelope amplifier further comprises

a second PMOS transistor having a gate receiving a third control signal, a source receiving the boosted supply voltage, and a drain coupled to the source of the PMOS transistor, and

a third PMOS transistor having a gate receiving a fourth control signal, a source receiving the first supply voltage, and a drain coupled to the source of the PMOS transistor.

6. The apparatus of claim 1, further comprising:

a power amplifier operative to receive the second supply voltage from the envelope amplifier and to receive and amplify an input radio frequency (RF) signal and provide an output RF signal.

7. The apparatus of claim 1, wherein the first supply voltage is a battery voltage for the apparatus.

8. An integrated circuit comprising:

a boost converter operative to receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage; and

an envelope amplifier operative to receive an envelope signal and the boosted supply voltage and generate a second supply voltage based on the envelope signal and the boosted supply voltage.

9. The apparatus of claim 8, wherein the envelope amplifier is operative to further receive the first supply voltage and generate the second supply voltage based on the first supply voltage or the boosted supply voltage.

10. An apparatus for wireless communication, comprising:

a power amplifier operative to receive and amplify an input radio frequency (RF) signal and provide an output RF signal; and

a supply generator operative to receive an envelope signal and a first supply voltage, to generate a boosted supply voltage having a higher voltage than the first

supply voltage, and to generate a second supply voltage for the power amplifier based on the envelope signal and the boosted supply voltage.

11. The apparatus of claim 10, wherein the supply generator is operative to generate the second supply voltage based on the envelope signal and either the boosted supply voltage or the first supply voltage.

12. A method of generating supply voltages, comprising:

generating a boosted supply voltage based on a first supply voltage, the boosted supply voltage having a higher voltage than the first supply voltage; and

generating a second supply voltage based on an envelope signal and the boosted supply voltage.

13. The method of claim 12, wherein the generating the second supply voltage comprises generating the second supply voltage based on the envelope signal and either the boosted supply voltage or the first supply voltage.

14. An apparatus for generating supply voltages, comprising:

means for generating a boosted supply voltage based on a first supply voltage, the boosted supply voltage having a higher voltage than the first supply voltage; and

means for generating a second supply voltage based on the envelope signal and the boosted supply voltage.

15. The apparatus of claim 14, wherein the means for generating the second supply voltage comprises means for generating the second supply voltage based on an envelope signal and either the boosted supply voltage or the first supply voltage.

16. An apparatus comprising:

a switcher operative to receive a first supply voltage and provide a first supply current;

an envelope amplifier operative to receive an envelope signal and provide a second supply current based on the envelope signal; and

a power amplifier operative to receive a total supply current comprising the first supply current and the second supply current.

17. The apparatus of claim 16, further comprising:

a boost converter operative to receive the first supply voltage and provide a boosted supply voltage having a higher voltage than the first supply voltage, wherein the envelope amplifier operates based on the first supply voltage or the boosted supply voltage.

18. The apparatus of claim 16, wherein the switcher comprises

a current sense amplifier operative to sense the first supply current, or the second supply current, or the total supply current and provide a sensed signal,

a driver operative to receive the sensed signal and provide a first control signal and a second control signal,

a P-channel metal oxide semiconductor (PMOS) transistor having a gate receiving the first control signal, a source receiving the first supply voltage, and a drain providing a switching signal for an inductor providing the first supply current, and

an N-channel metal oxide semiconductor (NMOS) transistor having a gate receiving the second control signal, a drain providing the switching signal, and a source coupled to circuit ground.

19. The apparatus of claim 16, wherein the first supply current comprises direct current (DC) and low frequency components, and wherein the second supply current comprises higher frequency components.

20. An apparatus comprising:

an inductor operative to receive a switching signal and provide a supply current; and

a switcher operative to sense an input current and generate the switching signal to charge and discharge the inductor to provide the supply current, the switcher adding an offset to the input current to generate a larger supply current via the inductor than without the offset.

21. The apparatus of claim 20, wherein the switcher operates based on a first supply voltage, and wherein the offset is determined based on the first supply voltage.

22. The apparatus of claim 20, wherein the switcher comprises

a summer operative to sum the input current and an offset current and provide a summed current,

a current sense amplifier operative to receive the summed current and provide a sensed signal, and

a driver operative to receive the sensed signal and provide at least one control signal used to generate the switching signal for the inductor.

23. The apparatus of claim 22, wherein the at least one control signal comprises a first control signal and a second control signal, and wherein the switcher further comprises

a P-channel metal oxide semiconductor (PMOS) transistor having a gate receiving the first control signal, a source receiving a first supply voltage, and a drain providing the switching signal, and

an N-channel metal oxide semiconductor (NMOS) transistor having a gate receiving the second control signal, a drain providing the switching signal, and a source coupled to circuit ground.

24. The apparatus of claim 20, further comprising:

an envelope amplifier operative to receive an envelope signal and provide a second supply current based on the envelope signal, wherein a total supply current comprises the supply current from the switcher and the second supply current from the envelope amplifier.

25. The apparatus of claim 24, further comprising:

a boost converter operative to receive the first supply voltage and provide a boosted supply voltage having a higher voltage than the first supply voltage, wherein the envelope amplifier operates based on the first supply voltage or the boosted supply voltage.

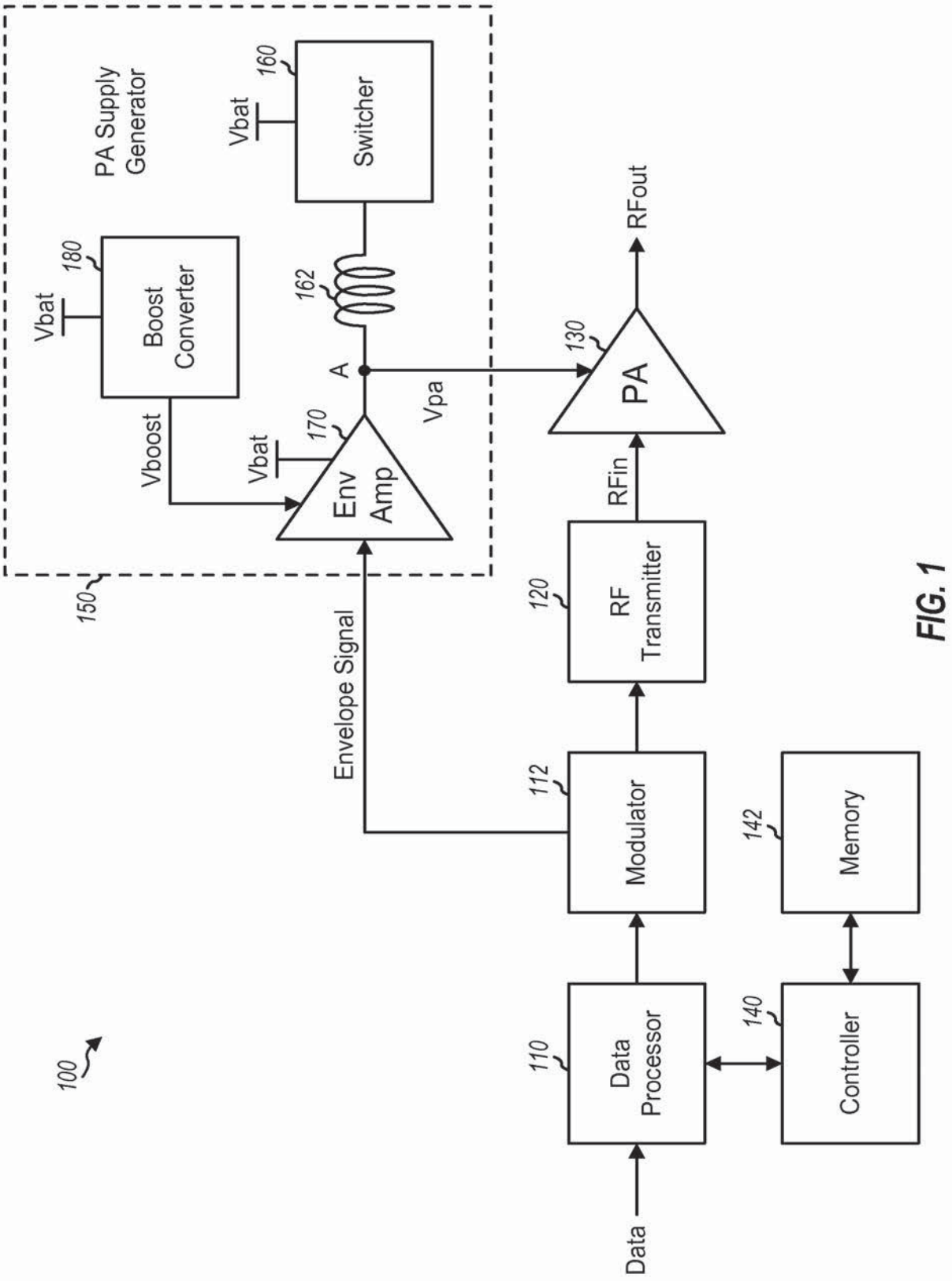
26. The apparatus of claim 20, further comprising:

a power amplifier operative to receive the supply current from the inductor and to receive and amplify an input radio frequency (RF) signal and provide an output RF signal.

ABSTRACT

Techniques for efficiently generating a power supply are described. In one design, an apparatus includes an envelope amplifier and a boost converter. The boost converter generates a boosted supply voltage having a higher voltage than a first supply voltage (e.g., a battery voltage). The envelope amplifier generates a second supply voltage based on an envelope signal and the boosted supply voltage (and also possibly the first supply voltage). A power amplifier operates based on the second supply voltage. In another design, an apparatus includes a switcher, an envelope amplifier, and a power amplifier. The switcher receives a first supply voltage and provides a first supply current. The envelope amplifier provides a second supply current based on an envelope signal. The power amplifier receives a total supply current including the first and second supply currents. In one design, the switcher detects the second supply current and adds an offset to generate a larger first supply current than without the offset.

1/6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Env Amp
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Vbat
Envelope Signal

FIG. 1

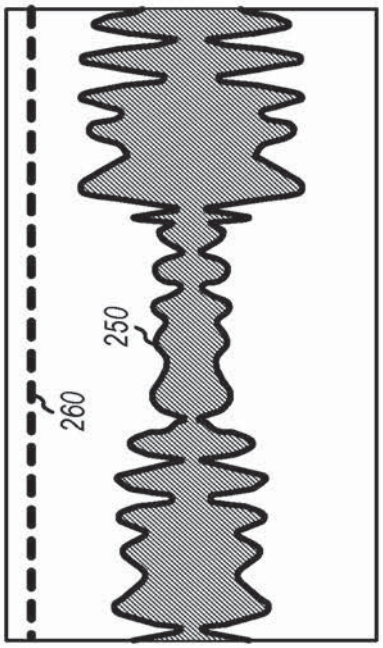


FIG. 2A

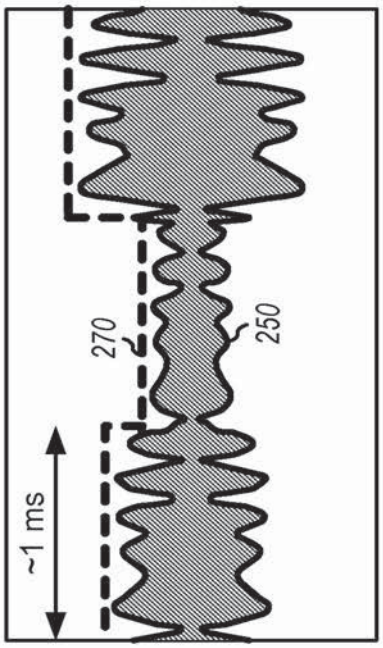
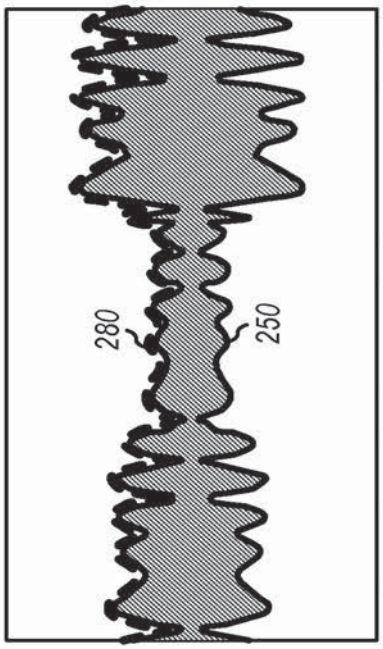


FIG. 2B



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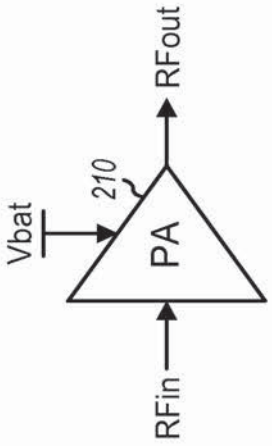

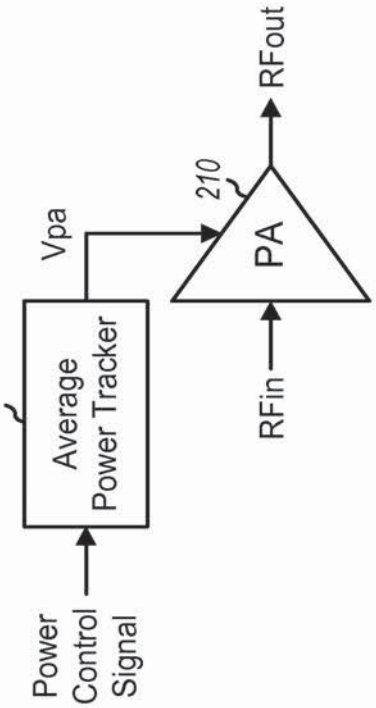

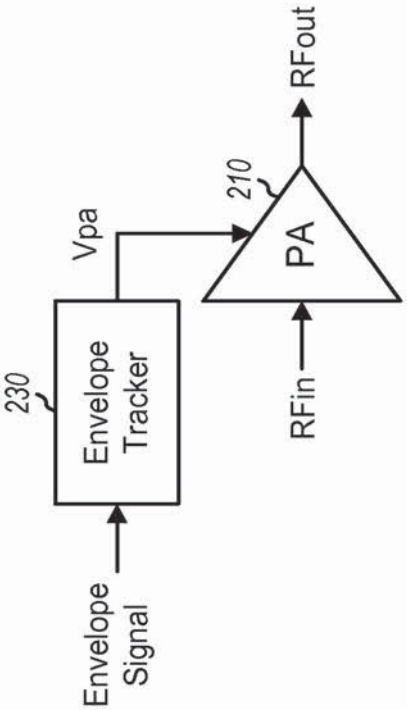

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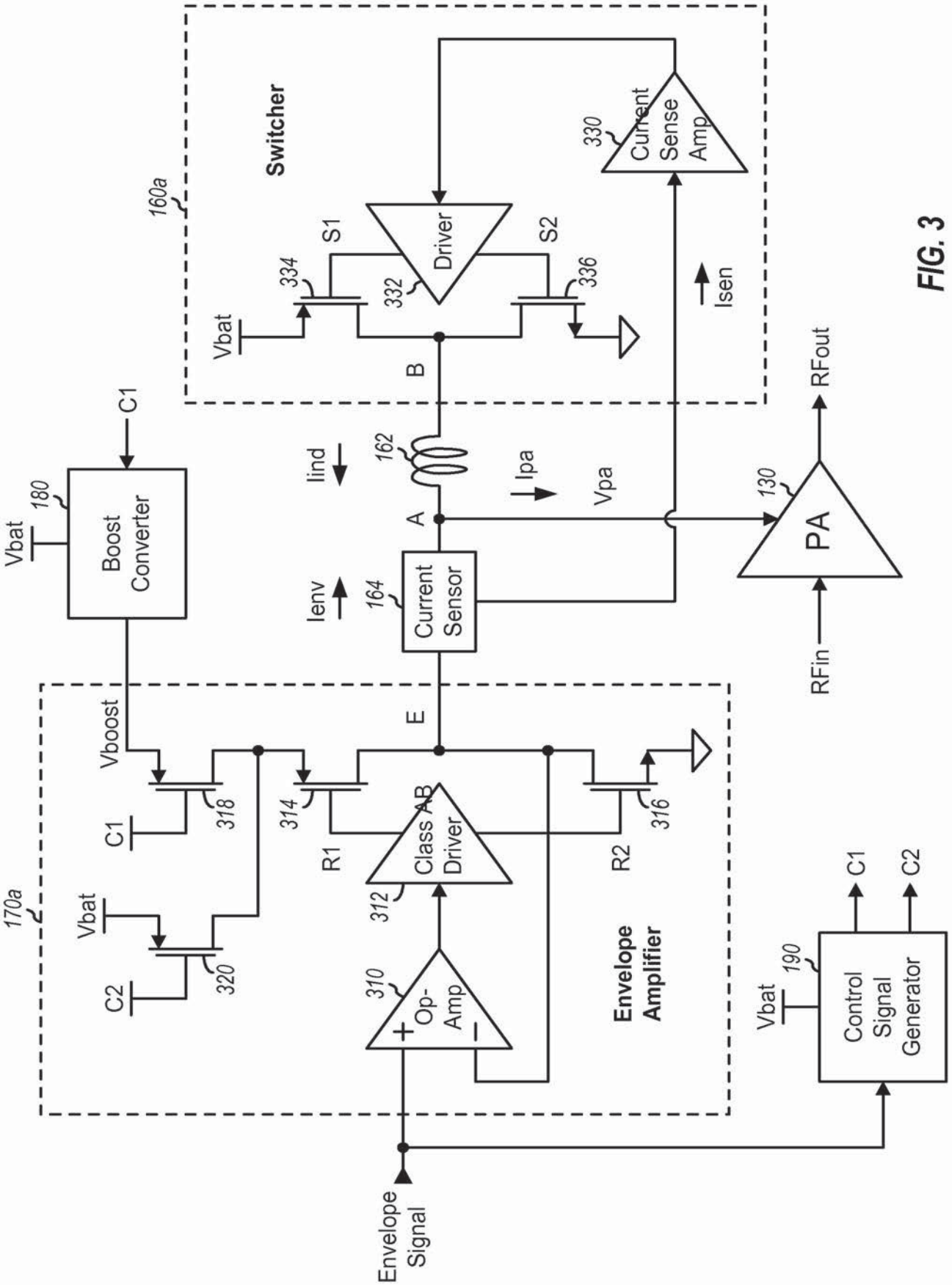
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B
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Vpa
RFout
Vbat
180
Boost Converter
A
130
PA
Ienv
164
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RFin
Vboost
E
C1
318
314
316
Class AB Driver
R1
R2
170a
Vbat
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Envelope Amplifier
Vbat
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Envelope Signal

FIG. 3

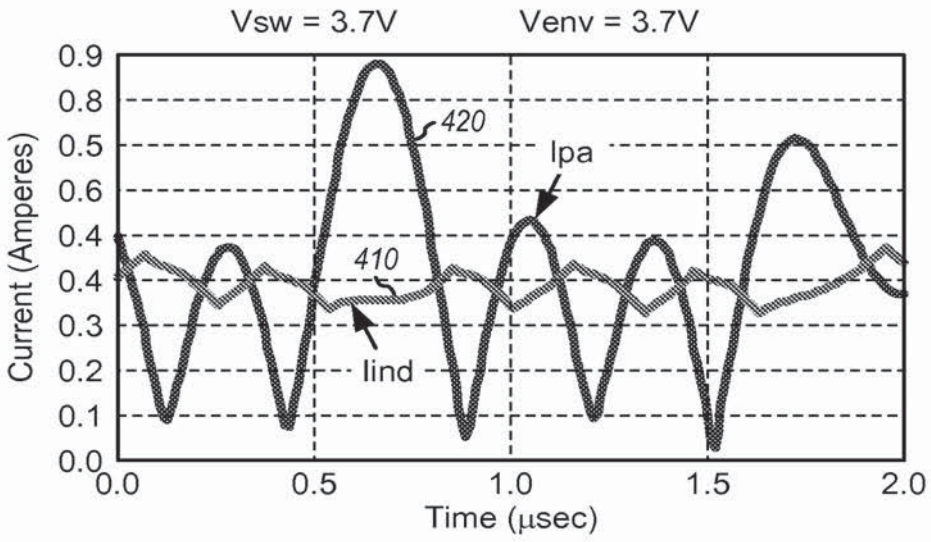
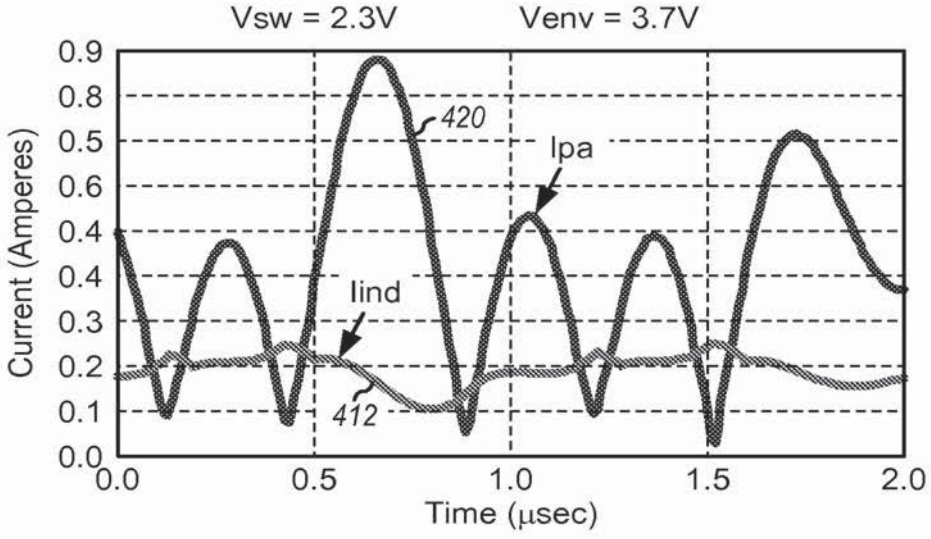


FIG. 4A



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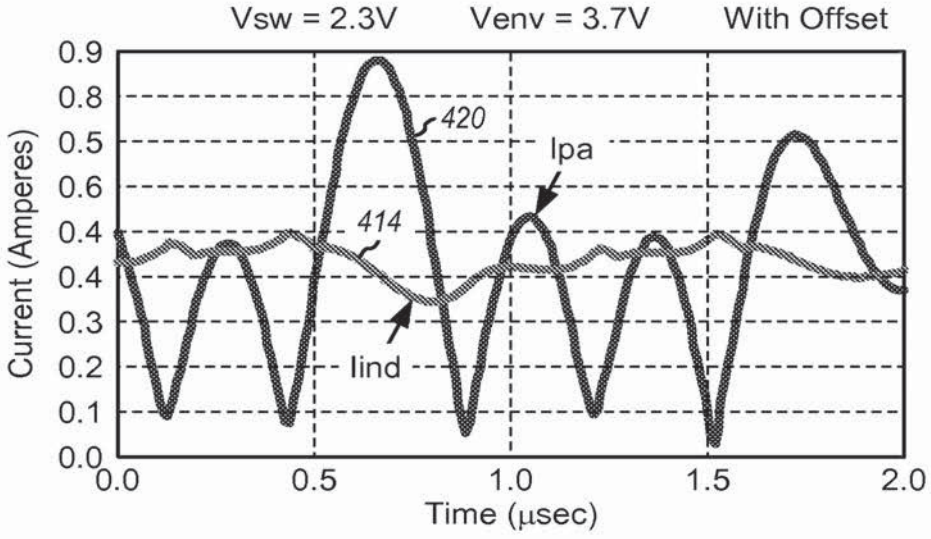
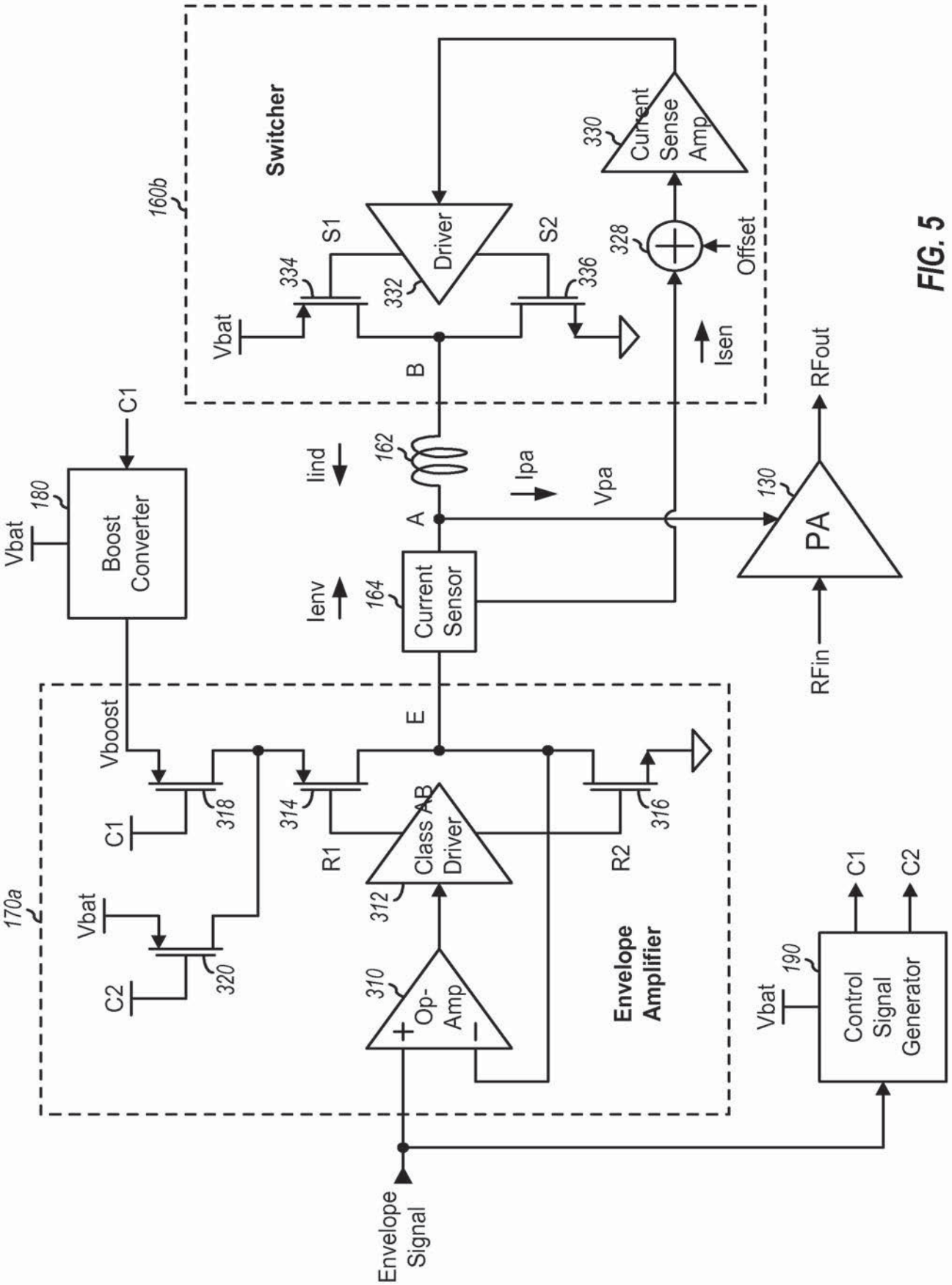


FIG. 4C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Vboost
C1
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R1
Class AB Driver
R2
170a
Vbat
C2
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Op-Amp
Envelope Amplifier
Vbat
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Control Signal Generator
C1
C2
Envelope Signal

FIG. 5

6/6

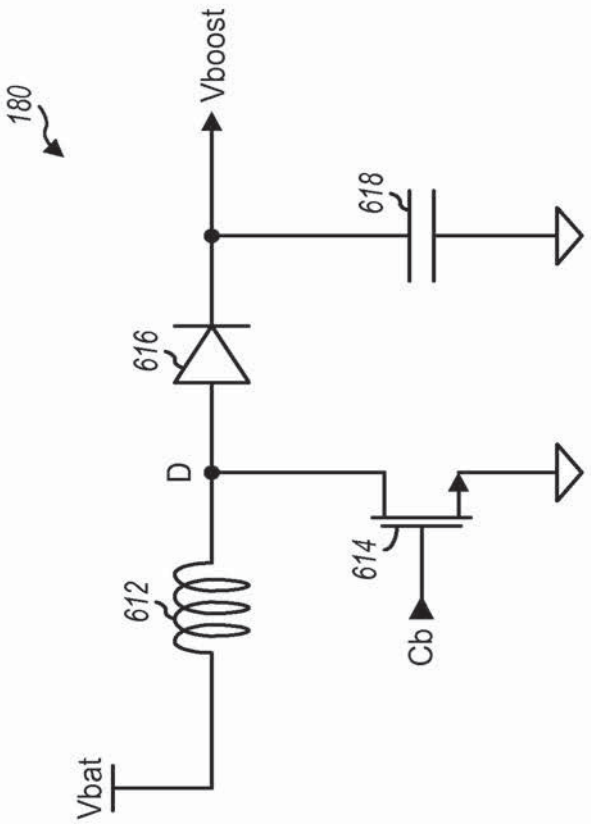

FIG. 6

PTO/SB/14 (11-08)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	101005
	Application Number	
Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Lennart	K	Mathe	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	SE

Mailing Address of Applicant:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country i	US

Applicant 2 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Thomas	D	Marra	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	US

Mailing Address of Applicant:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country i	US

Applicant 3 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Todd	R	Sutton	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Del Mar	State/Province	CA	Country of Residence i	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	101005
	Application Number	
Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER	

Citizenship under 37 CFR 1.41(b) [i]	US		
Mailing Address of Applicant:			
Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country**[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23696		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER		
Attorney Docket Number	101005	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	3

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	101005
	Application Number	
Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER	

Customer Number	23696

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			(•) Yes ( ) No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. [X]

Organization Name	QUALCOMM Incorporated		
Mailing Address Information:			
Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Country [i] US		Postal Code	92121
Phone Number	858-845-4265	Fax Number	
Email Address	us-docketing@qualcomm.com		

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

PTO/SB/14 (11-08)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	101005
	Application Number	
Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER	

Signature	/William Marcus Hooks/			Date (YYYY-MM-DD)	2011-06-23
First Name	William M.	Last Name	Hooks	Registration Number	48857

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER
First Named Inventor/Applicant Name:	Lennart K Mathe
Filer:	William M. Hooks/Sheryl Schoen
Attorney Docket Number:	101005

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	6	52	312
Independent claims in excess of 3	1201	4	220	880
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	2282

Electronic Acknowledgement Receipt

EFS ID:	10377238
Application Number:	13167659
International Application Number:	
Confirmation Number:	8529
Title of Invention:	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER
First Named Inventor/Applicant Name:	Lennart K Mathe
Customer Number:	23696
Filer:	William M. Hooks/Sheryl Schoen
Filer Authorized By:	William M. Hooks
Attorney Docket Number:	101005
Receipt Date:	23-JUN-2011
Filing Date:	
Time Stamp:	21:12:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2282
RAM confirmation Number	8002
Deposit Account	170026
Authorized User	

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Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

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Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		101005_2011-06-23_APP.pdf	136650 15c1b740d7e6ffff755c770ce8423388c3cad265	yes	20

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	14
Claims	15	19
Abstract	20	20

Warnings:					
Information:					
2	Drawings-only black and white line drawings	101005_2011-06-23_DWGS.pdf	119132 31f82858ab14fb281d6ffce788e41e0239bef5b4	no	6
Warnings:					
Information:					
3	Application Data Sheet	101005_2011-06-23_ADS.pdf	1031676 1a388f9805dff772558147d71b10c680a57c6aad	no	5
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	37846 a334f6b25393f98e441141ff9c9352ba52de5667	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1325304		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 13167659 Document Date: 6/23/2011

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/167,659	06/23/2011	2821	2282	101005	26	7

CONFIRMATION NO. 8529

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

FILING RECEIPT

OC000000048700431

Date Mailed: 07/19/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Lennart K. Mathe, San Diego, CA;
Thomas D. Marra, San Diego, CA;
Todd R. Sutton, Del Mar, CA;

Assignment For Published Patent Application

QUALCOMM INCORPORATED, San Diego, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 07/11/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/167,659**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

Preliminary Class

315

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/167,659	06/23/2011	Lennart K. Mathe	101005

CONFIRMATION NO. 8529

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

FORMALITIES LETTER

OC000000048700432

Date Mailed: 07/19/2011

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $**130** for a non-small entity
- $**130** Surcharge.

Replies should be mailed to:

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Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

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https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

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/tgebre/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/167,659

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 52 =	312
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4				x 220 =	880
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2282

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PATENT
Docket No. 101005

PTO/SB/01A (01-09)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☐ The attached application, or

☒ Application No. 13/167,659 filed on 06/23/2011

☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Lennart K. Mathe Date: Aug-8 2011

Signature: Lennart K. Mathe Citizen of: SE

Inventor two: Thomas Domenick Marra Date: 8/8/11

Signature: Thomas D. Marra Citizen of: US

☒ Additional inventors or a legal representative are being named on 1 of 2 additional form(s) attached hereto.

PATENT
Docket No. 101005

PTO/SB/01A (01-09)
Approved for use through 06/30/2010. OMB 0651-0032
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

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This declaration is directed to:

☐ The attached application, or

☒ Application No. 13/167,659 filed on 06/23/2011

☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

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FULL NAME OF INVENTOR(S)

Inventor one: Todd R. Sutton Date: 2/14/2011

Signature: _____ Citizen of: US

Inventor two: _____ Date: _____

Signature: _____ Citizen of: _____

☒ Additional inventors or a legal representative are being named on 2 of 2 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	13167659
Filing Date:	23-Jun-2011
Title of Invention:	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER
First Named Inventor/Applicant Name:	Lennart K. Mathe
Filer:	William M. Hooks/Sheryl Schoen
Attorney Docket Number:	101005

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt

EFS ID:	10982634
Application Number:	13167659
International Application Number:	
Confirmation Number:	8529
Title of Invention:	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER
First Named Inventor/Applicant Name:	Lennart K. Mathe
Customer Number:	23696
Filer:	William M. Hooks/Sheryl Schoen
Filer Authorized By:	William M. Hooks
Attorney Docket Number:	101005
Receipt Date:	19-SEP-2011
Filing Date:	23-JUN-2011
Time Stamp:	18:28:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$130
RAM confirmation Number	13274
Deposit Account	170026
Authorized User	

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	101005_2011-08-17_decl_Signed.pdf	1059328 56b45074b4c1df8e68d77b92f022e8f28bbca980	no	2

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Information:

2	Fee Worksheet (SB06)	fee-info.pdf	29994 3a519b7e21b74a755023c904cb4090eb4d1be433	no	2

Warnings:

Information:

Total Files Size (in bytes):	1089322

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/167,659	06/23/2011	2821	2412	101005	26	7

CONFIRMATION NO. 8529

UPDATED FILING RECEIPT

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

Date Mailed: 09/28/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Lennart K. Mathe, San Diego, CA;
Thomas Domenick Marra, San Diego, CA;
Todd R. Sutton, Del Mar, CA;

Assignment For Published Patent Application

QUALCOMM INCORPORATED, San Diego, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 07/11/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/167,659**

Projected Publication Date: 12/27/2012

Non-Publication Request: No

Early Publication Request: No

Title

LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

Preliminary Class

315

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/167,659

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 60 =	360
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4				x 250 =	1000
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2610

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	13/167,659
Filing Date	2011-06-23
First Named Inventor	Lennart K. Mathe
Art Unit	2821
Examiner Name	Unknown

Sheet	1	of	3	**Attorney Docket No:** 101005

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	001	US6300826	10-09-2001	MATHE; Lennart et al.	
	002	US6661217	12-09-2003	KIMBALL; Donald Felt et al.	
	003	US6792252	09-14-2004	KIMBALL; Donald Felt et al.	
	004	US7061313	06-13-2006	KIMBALL; Donald Felt et al.	
	005	US7068984	06-27-2006	MATHE; Lennart et al.	
	006	US7368985	05-06-2008	KUSUNOKI; Shigeo	
	007	US7679433	03-16-2010	LI; Yushan	
	008	US7932780	04-26-2011	ELIA; Avner	
	009	US20080278136	11-13-2008	MURTOJARVI; Simo	
	010	US20100001793	01-07-2010	VAN ZEIJL; Paulus Thomas Maria et al.	
	011	US20110095827	04-28-2011	TANAKA; Satoshi et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
	012	CHOI, et al., "Envelope Tracking Power Amplifier Robust to Battery Depletion," 2010 IEEE	☐

EXAMINER SIGNATURE **DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes ofUSPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by theUSPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	13/167,659
Filing Date	2011-06-23
First Named Inventor	Lennart K. Mathe
Art Unit	2821
Examiner Name	Unknown

Sheet	2	of	3	**Attorney Docket No:** 101005

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
		MTT-S International Microwave SYmposium Digest (MTT), May 2010.	

EXAMINER SIGNATURE **DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes ofUSPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by theUSPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08a (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	3	of	3

Complete if Known

Application Number	13/167,659
Filing Date	2011-06-23
First Named Inventor	Lennart K. Mathe
Art Unit	2821
Examiner Name	Unknown
Attorney Docket No:	101005

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/William Marcus Hooks/	Date (YYYY-MM-DD)	2011-10-20
Name/Print	William M. Hooks	Registration Number	48857

Electronic Acknowledgement Receipt

EFS ID:	11227892
Application Number:	13167659
International Application Number:	
Confirmation Number:	8529
Title of Invention:	LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER
First Named Inventor/Applicant Name:	Lennart K. Mathe
Customer Number:	23696
Filer:	William M. Hooks/Sheryl Schoen
Filer Authorized By:	William M. Hooks
Attorney Docket Number:	101005
Receipt Date:	20-OCT-2011
Filing Date:	23-JUN-2011
Time Stamp:	13:19:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	101005_2011-10-20_IDS.pdf	128873 662755695ed6f1e5bca1e72d06f4ea20ec35e69e	no	3

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	CHOI_ENVELOPE_TRACKING_YEAR_2010.PDF	4457957 cb4831e3879d29de98d853d8f937cf319ac93ee3	no	4
Warnings:					
Information:					
			Total Files Size (in bytes):	4586830	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/167,659	06/23/2011	Lennart K. Mathe	101005	8529

23696 7590 11/23/2012
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
NGUYEN, KHANH V	
ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
11/23/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	13/167,659	MATHE ET AL.	
	Examiner	Art Unit	
	KHANH V. NGUYEN	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-26* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-3,6-17,19-21 and 24-26* is/are rejected.

8)☒ Claim(s) *4,5,18,22 and 23* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *23 June 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/11*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

(B) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

The conditions where the envelope amplifier operated according to "first threshold" and/or "second threshold" is not seen disclosed in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 6-17, 19-21, 24-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Kim et al. (RMO3D-1), titled “High Efficiency and Wideband Envelope Tracking Power Amplifier with Sweet Spot Tracking”.

Regarding claims 1, 2, 8, 9, 12-15, Kim et al. (Fig. 3) disclose a block diagram of a hybrid switching supply modulator with boost converter comprising: a Boost Converter to receive a first supply voltage (3.4V) and generate a boosted supply voltage having a higher voltage (5V) than the first supply voltage; and a linear amplifier operable as an envelope amplifier to receive an envelope signal via non-inverting terminal (+) and the boosted supply voltage (5V) and generate a second supply voltage.

Regarding claim 6, further comprising a power amplifier (RF PA).

Regarding claim 7, wherein voltage supply (3.4V) operable as a battery.

Regarding claims 10, 11, Kim et al. (Fig. 3) disclose a block diagram of a hybrid switching supply modulator with boost converter comprising: a power amplifier (RF PA), a Boost Converter to receive a first supply voltage (3.4V) and generate a boosted supply voltage having a higher voltage (5V) than the first supply voltage; and a linear amplifier operable as an envelope amplifier to receive an envelope signal via non-inverting terminal (+) and the boosted supply voltage (5V) and generate a second supply voltage.

Regarding claims 16, Kim et al. (Fig. 3) disclose a block diagram of a hybrid switching supply modulator with boost converter comprising: field effect transistors operable as a switcher; a linear amplifier operable as an envelope amplifier to receive an envelope signal via non-inverting terminal (+) and a power amplifier (RF PA) having the functions as claimed.

Regarding claim 17, further comprising a Boost Converter having the functions as claimed.

Regarding claim 19, wherein current output from linear amplifier can be DC and low frequency components and current output from switch transistors (FETs) to inductor can be a higher frequency components.

Regarding claims 20, 21, Kim et al. (Fig. 3) disclose a block diagram of a hybrid switching supply modulator with boost converter comprising: an inductor operable to receive a switching signal and provide a supply current from switch transistors (FETs) having the functions thereof.

Regarding claim 24, further comprising a linear amplifier which can be read as an envelope amplifier.

Regarding claim 25, further comprising a Boost Converter.

Regarding claim 26, further comprising a power amplifier (RF PA).

Allowable Subject Matter

Claims 4, 5, 18, 22, 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 4, 5 and 18, call for, among others, an operational amplifier (op-amp) operative to receive the envelope signal and provide an amplified signal, a driver operative to receive the amplified signal and provide a first control signal and a second

control signal, a P-channel metal oxide semiconductor (PMOS) transistor having a gate receiving the first control signal, a source receiving the boosted supply voltage or the first supply voltage, and a drain providing the second supply voltage, and an N-channel metal oxide semiconductor (NMOS) transistor having a gate receiving the second control signal, a drain providing the second supply voltage, and a source coupled to circuit ground.

Claims 22 and 23 call for, among others, a summer operative to sum the input current and an offset current and provide a summed current, a current sense amplifier operative to receive the summed current and provide a sensed signal, and a driver operative to receive the sensed signal and provide at least one control signal used to generate the switching signal for the inductor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional references cited in PTO-892 show further analogous prior art circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is 571-272-1767. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khanh Van Nguyen/
Primary Examiner, Art Unit 2817

Notice of References Cited	Application/Control No. 13/167,659	Applicant(s)/Patent Under Reexamination MATHE ET AL.	
	Examiner KHANH V. NGUYEN	Art Unit 2817	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,905,407 A	05-1999	Midya, Pallab	330/10
*	B	US-6,838,931 B2	01-2005	Midya et al.	330/10
*	C	US-7,755,431 B2	07-2010	Sun, Kae-Oh	330/297
*	D	US-7,932,780 B2	04-2011	Elia, Avner	330/136
*	E	US-8,030,995 B2	10-2011	Okubo et al.	330/297
*	F	US-8,237,499 B2	08-2012	Chen et al.	330/136
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13167659	MATHE ET AL.
	Examiner	Art Unit
	KHANH V NGUYEN	2817

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/17/2012								
	1	✓								
	2	✓								
	3	✓								
	4	O								
	5	O								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	O								
	19	✓								
	20	✓								
	21	✓								
	22	O								
	23	O								
	24	✓								
	25	✓								
	26	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13167659	MATHE ET AL.
	Examiner	Art Unit
	KHANH V NGUYEN	2817

SEARCHED			
Class	Subclass	Date	Examiner
330	10,136,207A,251,297	11/5/2012	NKV

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Receipt date: 10/20/2011

13167659 - GAU: 2817

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	13/167,659
Filing Date	2011-06-23
First Named Inventor	Lennart K. Mathe
Art Unit	~~2824~~
Examiner Name	~~Unknown~~ /Khanh Nguyen/

Sheet	1	of	3

Attorney Docket No: 101005

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	001	US6300826	10-09-2001	MATHE; Lennart et al.	
	002	US6661217	12-09-2003	KIMBALL; Donald Felt et al.	
	003	US6792252	09-14-2004	KIMBALL; Donald Felt et al.	
	004	US7061313	06-13-2006	KIMBALL; Donald Felt et al.	
	005	US7068984	06-27-2006	MATHE; Lennart et al.	
	006	US7368985	05-06-2008	KUSUNOKI; Shigeo	
	007	US7679433	03-16-2010	LI; Yushan	
	008	US7932780	04-26-2011	ELIA; Avner	
	009	US20080278136	11-13-2008	MURTOJARVI; Simo	
	010	US20100001793	01-07-2010	VAN ZEIJL; Paulus Thomas Maria et al.	
	011	US20110095827	04-28-2011	TANAKA; Satoshi et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
	012	CHOI, et al., "Envelope Tracking Power Amplifier Robust to Battery Depletion," 2010 IEEE	☐

EXAMINER SIGNATURE /Khanh Nguyen/ **DATE CONSIDERED** 11/05/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes ofUSPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by theUSPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /K.N./

Receipt date: 10/20/2011

13167659 - GAU: 2817

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	13/167,659
Filing Date	2011-06-23
First Named Inventor	Lennart K. Mathe
Art Unit	2821
Examiner Name	Unknown

Sheet	2	of	3	**Attorney Docket No:** 101005

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
		MTT-S International Microwave SYmposium Digest (MTT), May 2010.	

EXAMINER SIGNATURE /Khanh Nguyen/ **DATE CONSIDERED** 11/05/2012

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Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 8529

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/167,659	06/23/2011	330	2817	101005

APPLICANTS

Lennart K. Mathe, San Diego, CA;
Thomas Domenick Marra, San Diego, CA;
Todd R. Sutton, Del Mar, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/11/2011

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /KHANH V NGUYEN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	26	7

ADDRESS

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121
UNITED STATES

TITLE

LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

FILING FEE RECEIVED		
2412	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	11	(("8030995") or ("5929776") or ("7932780") or ("2009027860") or ("5905407") or ("6838931") or ("20040208262") or ("7755431") or ("7808323") or ("20090191826") or ("7932780") or ("20110273235") or ("8237499") or ("8030995")).PN.	US-PGPUB; USPAT	OR	OFF	2012/11/17 17:41
L3	3	(("5414614") or ("6055168") or ("6198645")).PN.	US-PGPUB; USPAT	OR	OFF	2012/11/17 18:11
L4	163605	((Dongsu near1 Kim) or (Jinsung or Choi) or (Daehyun near1 Kang) or (Bumman near1 Kim)).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/17 18:14
L5	7	((Dongsu near1 Kim) or (Jinsung or Choi) or (Daehyun near1 Kang) or (Bumman near1 Kim)).in. and (envelope adj1 tracking)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/17 18:15
L6	11	Wideband with Envelope with Tracking with (Power adj1 Amplifier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/17 18:16
L7	121	boost$4 with (linear$4 adj1 (amplif$4 or amplification))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/17 18:20
L8	2	("6300826").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/11/17 18:55
S1	2	("6893101").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2012/11/05 13:41

			IBM_TDB			
S2	11	(("20080278136") or ("20100001793") or ("20110095827") or ("6300826") or ("6661217") or ("6792252") or ("7061313") or ("7068984") or ("7368985") or ("7679433") or ("7932780")).PN.	US-PGPUB; USPAT	OR	OFF	2012/11/05 13:45
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S6	58	("20050110562" | "20060119425" | "20070019446" | "20070024360" | "20070126408" | "20080030174" | "20080224769" | "20080237705" | "20090091305" | "3600667" | "3970953" | "4378530" | "4502152" | "4516080" | "5682303" | "5905407" | "5939867" | "6009000" | "6043707" | "6121761" | "6215290" | "6281666" | "6292378" | "6300826" | "6346798" | "6362607" | "6362608" | "6404175" | "6424129" | "6449174" | "6509722" | "6534962" | "6583664" | "6642631" | "6650096" | "6661210" | "6674274" | "6781452" | "6825726" | "6833760" | "6850045" | "6992353" | "7058373" | "7071662" | "7091777" | "7109689" | "7116946" | "7126315" | "7126317" | "7183755" | "7183856" | "7190150" | "7229886" | "7499502" | "7551688" | "7583149" | "7602155").PN. OR ("7808313").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/06 12:11
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			DERWENT; IBM_TDB			
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S15	36	("4152670" | "4446440" | "4523152" | "4600891" | "5329245" | "5352986" | "5543753").PN. OR ("5905407").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/12 18:04
S16	4	("5905407" | "6838931" | "7116947").PN. OR ("7755431").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/12 18:27
S17	6	(("20090289720") or ("6300826") or ("6583664")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/11/12 19:09
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S19	7	("20080074207" | "7449954" | "7679433" | "7755422").PN. OR ("7808323").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/12 19:11
S20	5	("20030146791" | "6437641" | "6621350" | "6975166" | "7091777").PN.	US-PGPUB; USPAT;	OR	ON	2012/11/12 19:43

		OR ("8274328").URPN.	USOCR			
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S22	229	"330"/$.ccls. and (((step$4 adj1 up) or boost$3) with converter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/13 09:33
S23	76	"330"/$.ccls. and ((DC adj1 DC) adj1 convert$4) same (envelop$3 with (amplif$4 or amplification))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/13 12:29
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S25	11	("20020153940" | "20040251968" | "20050057308" | "6437641" | "6492867" | "6566944" | "6831519" | "6985039" | "7193470" | "7405618" | "7420415").PN. OR ("7932780").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/13 13:46
S26	86	330/10,136,207A,251,297.ccls. and (envelop$4 adj1 (amplif$4 or amplification))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/13 20:22
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S29	60	("20020171477" | "20020186079" | "20030214355" | "20040174212" | "20050242875" | "3900823" | "4320350" | "4346349" | "5142240" | "5287069" | "5757229" | "5777519" | "5786727" | "5789984" | "5793253" | "5929702" | "6043707" | "6081161" | "6112062" | "6157253" | "6239656" | "6268768" | "6297696" | "6300826" | "6362685" | "6437641" | "6515541" | "6566944" | "6583664" | "6590451" | "6617920" | "6617929" | "6661284" | "6677819" | "6735419").PN. OR ("7440733").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/13 20:36
S30	4	("20090191826" | "20090289720" | "6583664" | "7808323").PN. OR ("8030995").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/11/13 20:51

EAST Search History (Interference)

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11/17/2012 7:37:13 PM
C:\Users\knguyen7\Documents\EAST\Workspaces\13167659.wsp

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/167,659	06/23/2011	Lennart K. Mathe	101005

CONFIRMATION NO. 8529

23696
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

PUBLICATION NOTICE

OC000000058353519

Title:LOW-VOLTAGE POWER-EFFICIENT ENVELOPE TRACKER

Publication No.US-2012-0326783-A1
Publication Date:12/27/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln. No.: 13/167,659 Applicant: Lennart K. Mathe et al. Filed: June 23, 2011 Examiner: Khanh V. Nguyen Art Unit: 2817 Customer No.: 23696 Confirm. No.: 8529 Docket No.: 101005	**Certificate of Transmission/Mailing** I hereby certify that this correspondence is being transmitted to the USPTO, transmitted via the Office electronic filing system addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below: 22 Feb 2013 /Sheryl Schoen/ Date Sheryl Schoen

Mail Stop **Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action dated November 23, 2012, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Canceled)

3. (Currently Amended) The apparatus of claim 4[[2]], wherein the envelope amplifier is operative to generate the second supply voltage based on the boosted supply voltage if the envelope signal exceeds a first threshold, or if the first supply voltage is below a second threshold, or both.

4. (Currently Amended) ~~The apparatus of claim 2~~ An apparatus comprising:

a boost converter operative to receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage; and

an envelope amplifier operative to receive an envelope signal and the boosted supply voltage and generate a second supply voltage based on the envelope signal and the boosted supply voltage, wherein the envelope amplifier is operative to further receive the first supply voltage and generate the second supply voltage based on the first supply voltage and generate the second supply voltage based on the first supply voltage or the boosted supply voltage, and further wherein the envelope amplifier comprises

an operational amplifier (op-amp) operative to receive the envelope signal and provide an amplified signal,

a driver operative to receive the amplified signal and provide a first control signal and a second control signal,

a P-channel metal oxide semiconductor (PMOS) transistor having a gate receiving the first control signal, a source receiving the boosted supply voltage or the first supply voltage, and a drain providing the second supply voltage, and

an N-channel metal oxide semiconductor (NMOS) transistor having a gate receiving the second control signal, a drain providing the second supply voltage, and a source coupled to circuit ground.

5. (Original) The apparatus of claim 4, wherein the envelope amplifier further comprises

a second PMOS transistor having a gate receiving a third control signal, a source receiving the boosted supply voltage, and a drain coupled to the source of the PMOS transistor, and

a third PMOS transistor having a gate receiving a fourth control signal, a source receiving the first supply voltage, and a drain coupled to the source of the PMOS transistor.

6. (Currently Amended) The apparatus of claim 4 ~~1~~, further comprising:

a power amplifier operative to receive the second supply voltage from the envelope amplifier and to receive and amplify an input radio frequency (RF) signal and provide an output RF signal.

7. (Currently Amended) The apparatus of claim 4 ~~1~~, wherein the first supply voltage is a battery voltage for the apparatus.

8. (Currently Amended) An integrated circuit comprising:

a boost converter operative to receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage; and

an envelope amplifier operative to receive an envelope signal and the boosted supply voltage and generate a second supply voltage based on the envelope signal and the boosted supply voltage, wherein the envelope amplifier is operative to further receive the first supply voltage and generate the second supply voltage based on the first supply voltage and generate the second supply voltage based on the first supply voltage or the boosted supply voltage, and further

a boost converter operative to receive a first supply voltage and generate a boosted supply voltage having a higher voltage than the first supply voltage; and