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Renous

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- (54) **POWER SUPPLY CIRCUIT WITH A VOLTAGE SELECTOR**
- (75) Inventor: **Claude Renous**, Grenoble (FR)
- (73) Assignee: **STMicroelectronics S.A.**, Gently (FR)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Primary Examiner—Terry D. Cunningham

(74) *Attorney, Agent, or Firm*—Wolf, Greenfield & Sacks, P.C.; James H. Morris

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- (58) **Field of Search** 327/407, 408, 327/530, 546; 307/64, 80, 87, 126, 130
- (56) **References Cited**

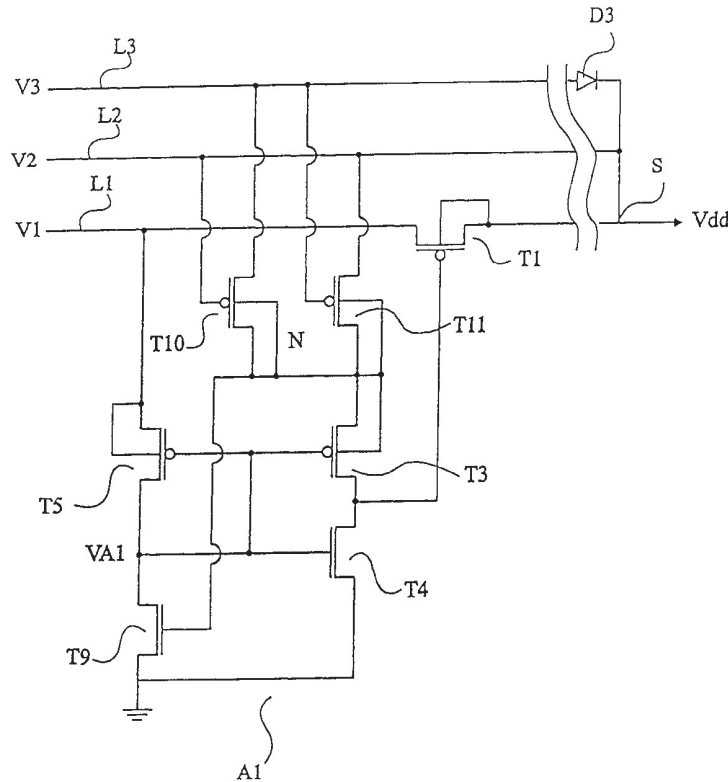
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(57) **ABSTRACT**

A power supply circuit receiving several supply voltages on respective switches, at least one of the switches being a first PMOS transistor connected between one of the supply voltages and a common output terminal, this switch being associated with a second PMOS transistor connected between the gate of the first transistor and a power supply node maintained at the highest of the other supply voltages, with a third NMOS transistor, which is less conductive in the on state than the second transistor, connected between the gate of the first transistor and the ground, and with a fourth PMOS transistor having its source connected to the power supply line of the switch and its drain connected to ground via a current source, and to the gates of the second, third, and fourth transistors.

17 Claims, 3 Drawing Sheets



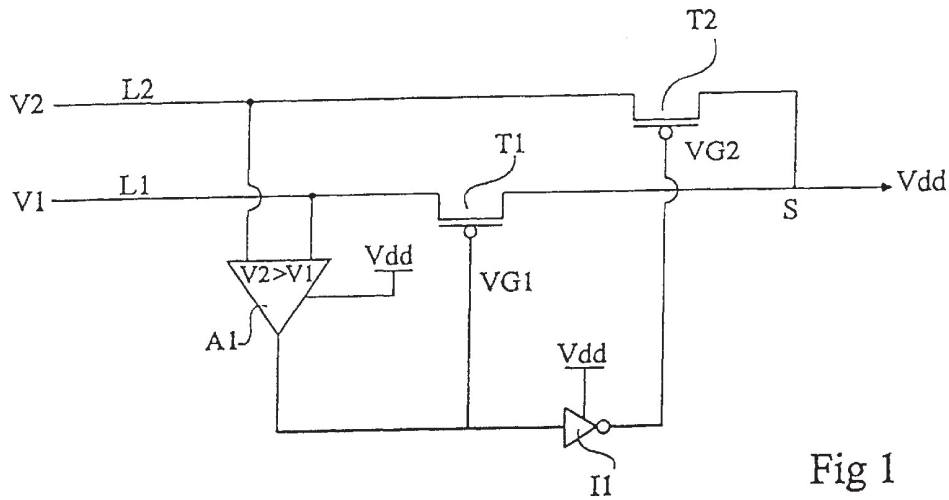


Fig 1

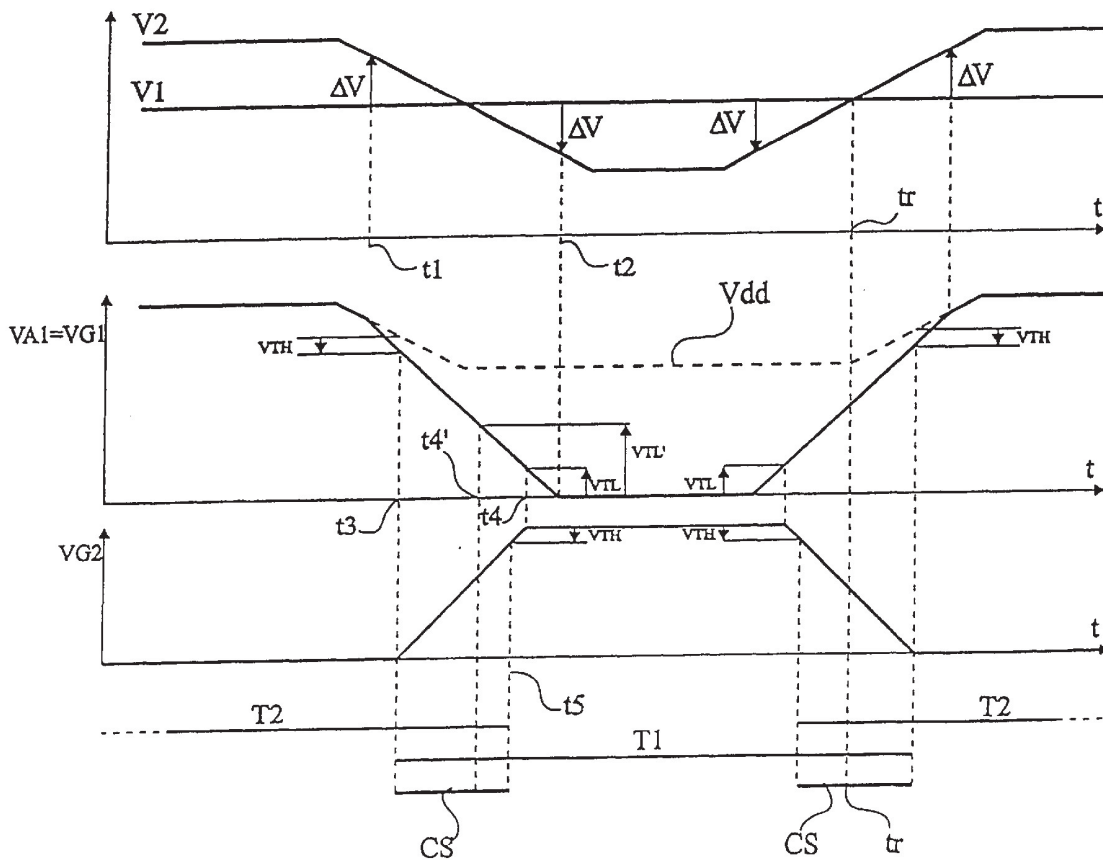


Fig 2

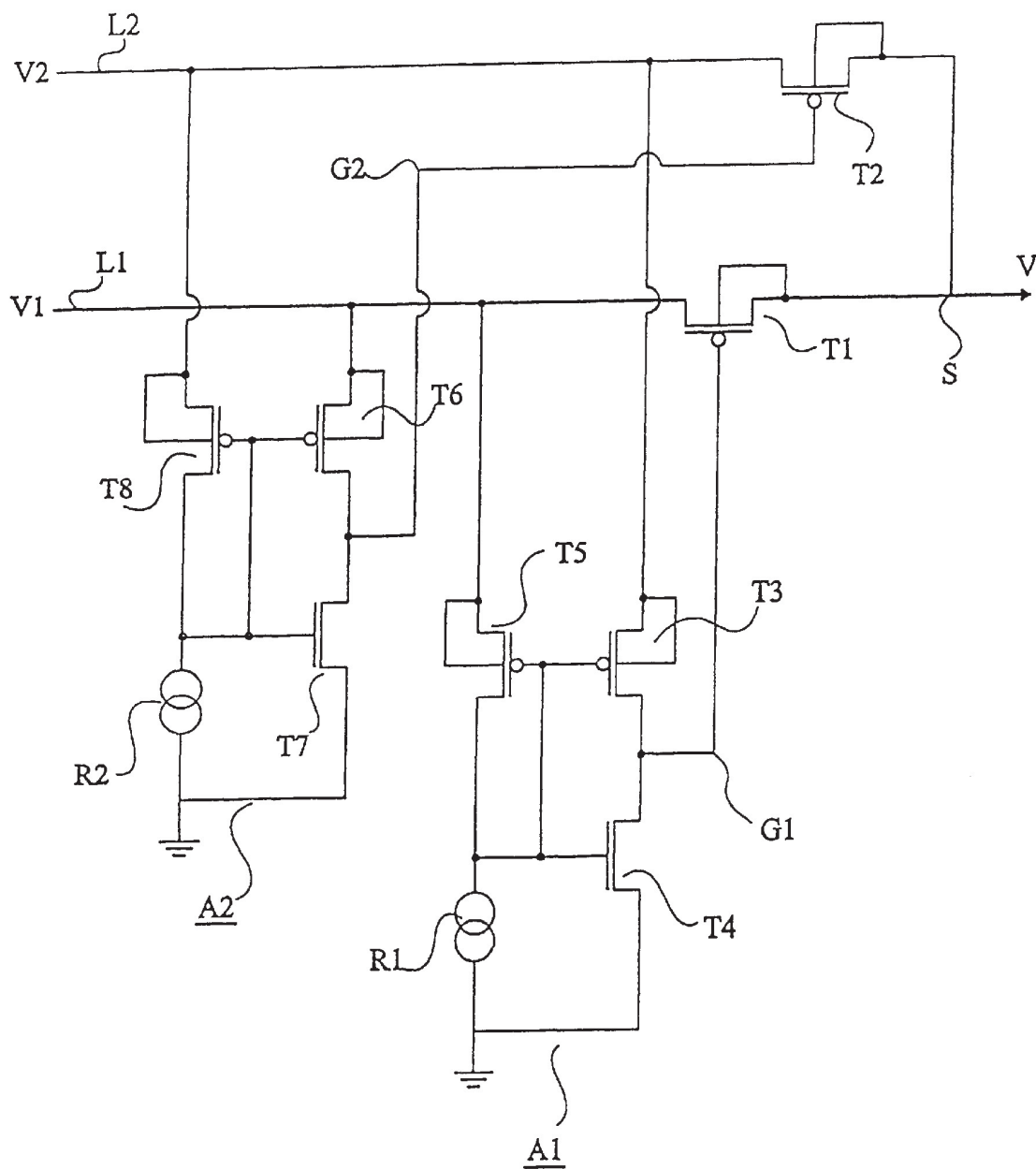


Fig 3

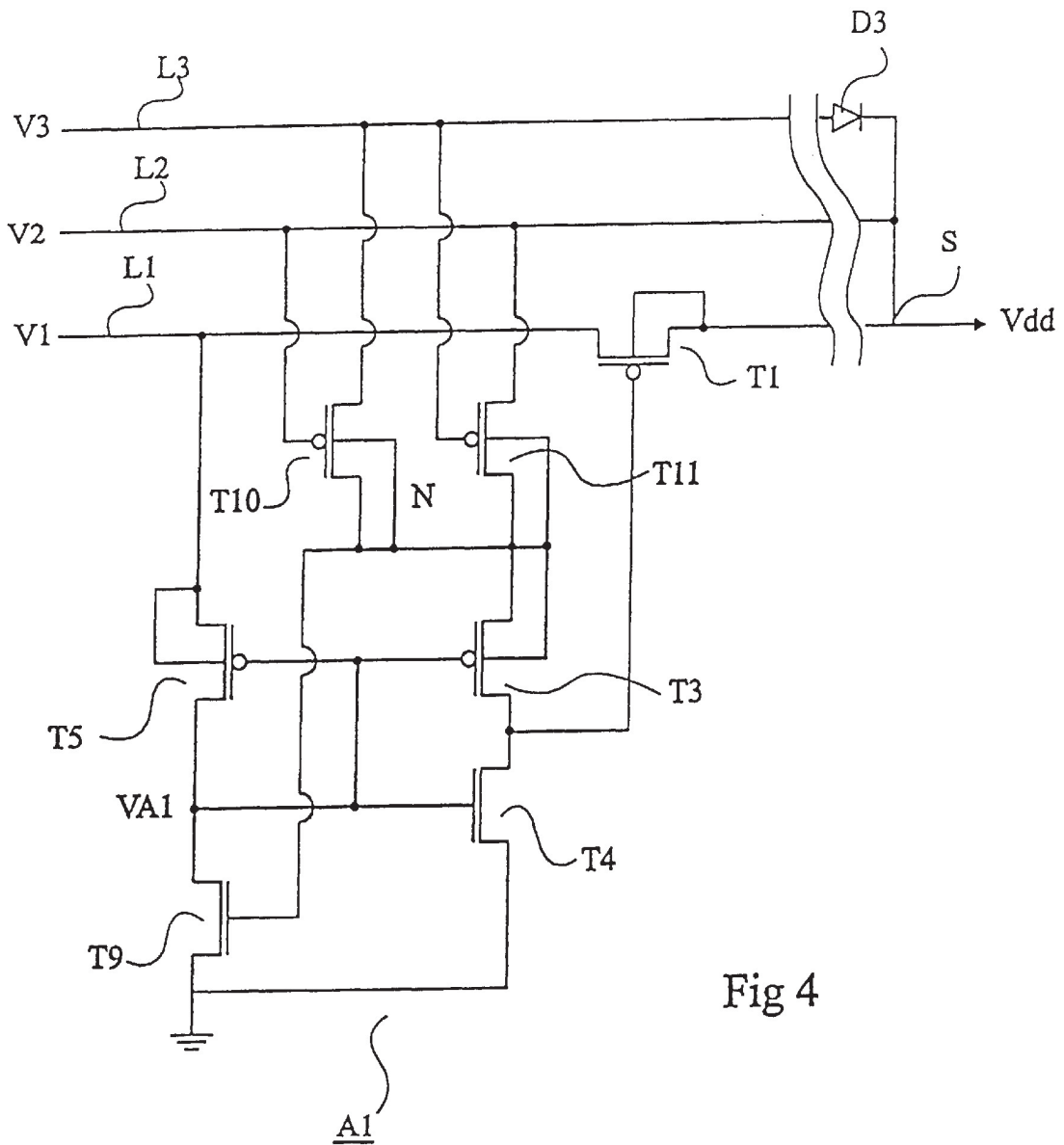


Fig 4

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POWER SUPPLY CIRCUIT WITH A VOLTAGE SELECTOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to power supply circuits, and especially to power supply circuits that receive several supply voltages and that select the highest supply voltage. Such power supply circuits are used, for example, in a rechargeable battery device for supplying the device from the battery or from an external power source, if any.

2. Discussion of the Related Art

FIG. 1 shows a conventional power supply circuit receiving two supply voltages V1 and V2 on two respective supply lines L1 and L2, and providing a voltage Vdd on an output node S. The two supply lines are connected to the output node by two P-channel MOS transistors (PMOS), respectively T1 and T2. A comparator A1 has two inputs respectively connected to the two supply lines so that the output of comparator A1 is at a low level when voltage V1 is greater than voltage V2 and at a high level otherwise. The output of comparator A1 is directly connected to the gate of transistor T1, and is connected to the gate of transistor T2 via an inverter I1.

Such power supply circuits are used when it is desired to obtain a small voltage drop between voltage V1 or V2 and voltage Vdd. In the cases where a high voltage drop can be tolerated, diodes are used instead of transistors T1 and T2.

FIG. 2A shows the variation of gate voltages VG1 and VG2 of transistors T1 and T2 for an example of relative variation of supply voltages V1 and V2. Voltage V1 remains constant while voltage V2 crosses voltage V1 as it decreases, then as it increases. It is assumed that comparator A1 and inverter I1 are both supplied between voltage Vdd and the ground.

When voltage V2 exceeds voltage V1 by a threshold ΔV characteristic of comparator A1, voltage VA1 provided by the comparator is equal to voltage Vdd. Thus, gates G1 and G2 are respectively at voltage Vdd and at ground. As a result, transistor T2 conducts and transistor T1 is off, transistor T2 transmitting voltage V2 on output node S. Similarly, when voltage V2 is smaller than voltage V1 by threshold ΔV , voltage VA1 provided by the comparator is at ground, whereby transistor T2 is off and transistor T1 is on, transistor T1 transmitting voltage V1 on output node S.

Range $\pm\Delta V$ is a range in which the comparator, which is by nature imperfect, behaves linearly. The comparator behaves linearly between times t1 and t2 when voltage V2 progressively decreases from voltage V1+ ΔV to voltage V1- ΔV and voltage VG1 progressively decreases from voltage Vdd to the ground.

Inverter I1 includes a PMOS transistor and an N-channel MOS transistor (NMOS). The threshold voltage of the PMOS transistor of inverter I1 is called VTH, which voltage is also that of PMOS transistors T1 and T2. Similarly, the threshold voltage of the NMOS transistor is called VTL.

At a time t3, voltage VG1 is equal to voltage Vdd-VTH, and at a time t4, voltage VG1 reaches voltage VTL. Gate voltage VG2, at the output of inverter I1, progressively varies between a zero level at time t3 and a level Vdd at time t4.

Transistor T1 starts conducting when its gate voltage VG1 reaches voltage Vdd-VTH, that is, at time t3.

At a time t5, gate voltage VG2 reaches voltage Vdd-VTH. Transistor T2 stops conducting at time t5.

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Thus, there is a range of simultaneous conduction (CS) of transistors T1 and T2 between times t3 and t5. There is a similar range of simultaneous conduction CS on either side of a time tr when voltage V2 becomes greater than voltage V1 again.

During a simultaneous conduction, the power supply sources generating voltages V1 and V2 are shorted, which is not desirable. Further, if the power supply source providing the highest supply voltage exhibits a high impedance, the shorting of the power supply sources results in a drop of the highest supply voltage to the level of the other supply voltage, and comparator A1 can no longer determine which of the supply voltages is greater. The power supply selection circuit is then blocked in an intermediary state and no longer properly ensures its function.

On the other hand, the principle used in the circuit of FIG. 1 does not enable selecting the highest of three supply voltages or more.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a circuit for selecting the highest of two supply voltages or more, which can operate without short-circuiting power supply lines.

To achieve this object, as well as others, the present invention provides a power supply circuit receiving several supply voltages on respective power supply lines, each of which is connected to a respective switch, at least one of the switches being a first MOS transistor of a first conductivity type, connected between the associated power supply line and a common output terminal, which includes, for said at least one switch: a second transistor, of the first conductivity type, connected between the gate of the first transistor and a power supply node maintained at the highest of the other supply voltages, a third transistor, of a second conductivity type, which is less conductive in the on state than the second transistor, connected between the gate of the first transistor and a reference potential, and a fourth transistor, of the first conductivity type, having its source connected to the power supply line associated with the switch and its drain connected to the reference potential via a current source, and to the gates of the second, third, and fourth transistors.

According to an embodiment of the present invention, said current source is a fifth transistor, of the second conductivity type, having its gate connected to said power supply node.

According to an embodiment of the present invention, the power supply circuit includes two power supply lines and two respective switches, the power supply node associated with a switch being directly connected to the power supply line associated with the other switch.

According to an embodiment of the present invention, the power supply circuit includes three power supply lines, a sixth transistor connected between the third power supply line and the power supply node, and having its gate connected to the second power supply line, and a seventh transistor connected between the second power supply line and the power supply node and having its gate connected to the third power supply line.

According to an embodiment of the present invention, at least one of the switches is a diode.

According to an embodiment of the present invention, the second transistor has a width-to-length ratio of 20/2, and the third transistor has a W/L ratio of 3/25.

According to an embodiment of the present invention, the fourth transistor has a W/L ratio of 40/2, and the fifth transistor has a W/L ratio of 3/50.

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