

IEEE JOURNAL OF SOLID-STATE CIRCUITS

9844830 14/01/09 BOSTON SPA LS23 7BQ
IEEE JOURNAL OF SOLID STATE CIRCUITS.



4362.985500

Volume 43: Number 12 (2008: Dec.)
ET05 ESTAR9 PB FAST

1

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



DECEMBER 2008

VOLUME 43

NUMBER 12

IJSCBC

(ISSN 0018-9200)

SPECIAL ISSUE ON THE 2008 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC)

Introduction to the Special Issue on the 2008 IEEE International Solid-State Circuits Conference	<i>S. Tsukamoto, S.-I. Liu, S. Heinen, R. Thewes, and J. Lee</i>	2587
DATA CONVERTER PAPERS		
A 108 dB SNR, 1.1 mW Oversampling Audio DAC With A Three-level DEM Technique	<i>K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, and P. Baginski</i>	2592
A Noise-Coupled Time-Interleaved Delta-Sigma ADC With 4.2 MHz Bandwidth, -98 dB THD, and 79 dB SNDR	<i>K. Lee, J. Chae, M. Aniya, K. Hamashita, K. Takasuka, S. Takeuchi, and G. C. Temes</i>	2601
A 14-b 100-MS/s Pipelined ADC With a Merged SHA and First MDAC	<i>B.-G. Lee, B.-M. Min, G. Manganaro, and J. W. Valvano</i>	2613
An Over-60 dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain	<i>B. R. Gregoire and U. Moon</i>	2620
A 150 MS/s 133 μ W 7 bit ADC in 90 nm Digital CMOS	<i>G. Plas and B. Verbruggen</i>	2631
Highly Interleaved 5-bit, 250-MSample/s, 1.2-mW ADC With Redundant Channels in 65-nm CMOS	<i>B. P. Ginsburg and A. P. Chandrakasan</i>	2641
RF PAPERS		
A 52 GHz Phased-Array Receiver Front-End in 90 nm Digital CMOS	<i>K. Scheir, S. Bronckers, J. Borremans, P. Wambacq, and Y. Rolain</i>	2651
A Scalable 6-to-18 GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS	<i>S. Jeon, Y.-J. Wang, H. Wang, F. Bohn, A. Natarajan, A. Babakhani, and A. Hajimiri</i>	2660
Transmitter Architectures Based on Near-Field Direct Antenna Modulation	<i>A. Babakhani, D. B. Rutledge, and A. Hajimiri</i>	2674
A Compact Wideband Front-End Using a Single-Inductor Dual-Band VCO in 90 nm Digital CMOS	<i>J. Borremans, A. Bevilacqua, S. Bronckers, M. Dehan, M. Kuijk, P. Wambacq, and J. Craninckx</i>	2693
The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology	<i>S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta</i>	2706
Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise	<i>A. Mazzanti and P. Andreani</i>	2716
Terahertz CMOS Frequency Generator Using Linear Superposition Technique	<i>D. Huang, T. R. LaRocca, M.-C. F. Chang, L. Samoska, A. Fung, R. Campbell, and M. Andrews</i>	2730
A 56-65 GHz Injection-Locked Frequency Tripler With Quadrature Outputs in 90-nm CMOS	<i>W. L. Chan and J. R. Long</i>	2739
A Fully-Integrated Quad-Band GSM/GPRS CMOS Power Amplifier	<i>I. Aoki, S. Kee, R. Magoon, R. Aparicio, F. Bohn, J. Zachan, G. Hatcher, D. McClymont, and A. Hajimiri</i>	2747
ANALOG AND WIRELESS COMMUNICATION PAPERS		
A Field-Programmable Analog Array of 55 Digitally Tunable OTAs in a Hexagonal Lattice	<i>J. Becker, F. Henrici, S. Trendelenburg, M. Ortmanns, and Y. Manoli</i>	2759
A Current-Feedback Instrumentation Amplifier With 5 μ V Offset for Bidirectional High-Side Current-Sensing	<i>J. F. Witte, J. H. Huijsing, and K. A. A. Makinwa</i>	2769

(Contents Continued on Back Cover)



IEEE JOURNAL OF SOLID-STATE CIRCUITS

The IEEE JOURNAL OF SOLID-STATE CIRCUITS is published by the IEEE Solid-State Circuits Society. All IEEE members are eligible for membership and will receive this JOURNAL upon payment of the annual society membership fee of \$22.00. For information on receiving this JOURNAL, write to the IEEE Service Center at the address below. *Member copies of Transactions/Journals are for personal use only.*

SOLID-STATE CIRCUITS SOCIETY

<http://sscs.org>

President W. SANSEN K. U. Leuven Leuven, Belgium FAX: +32 16 321975	Vice President B. BOSER EECS Dept. Univ. of California Berkeley, CA 94720	Secretary D. A. JOHNS Univ. of Toronto Toronto, ON M5S 3G4 Canada FAX: (416) 971-2286	Treasurer R. KUMAR Technology Connexions Poway, CA 92064 FAX: (888) 386-2030	Past President R. C. JAEGER Alabama Microelectronics Ctr. Auburn Univ., AL 36849	Executive Office sscs@iecc.org Executive Director: A. O'NEILL (732) 981-3400 FAX: (732) 981-3401 a.oneill@iecc.org
--	--	--	---	--	--

ADMINISTRATIVE COMMITTEE

Elected for 2005-2008 Term W. GASS 6 Crownwood Ct. Dallas, TX 75225-2068	A. HAJIMIRI California Inst. of Technol. Pasadena, CA 91125-0001	P. J. HURST Univ. of California Dept. Elect. Comp. Eng. Davis, CA 95616	A. MATSUZAWA Tokyo Inst. of Technol. Ookayama, Meguro-ku Tokyo 152-8505, Japan	I. YOUNG Intel Corp. Hillsboro, OR 97124
Elected for 2007-2009 Term J. CORCORAN Agilent Technologies Palo Alto, CA 94303	K. KORNEGAY Sch. Electr. Comput. Eng. Georgia Inst. Technol. Atlanta, GA 30332-0250	H.-S. LEE Dept. Electr. Eng. Massachusetts Inst. Technol. Cambridge, MA 02139	T. H. LEE Ctr. Integr. Syst. Stanford Univ. Stanford, CA 94305-4070	J. VAN DER SPIEGEL Dept. Elect. Syst. Eng. Univ. of Pennsylvania Philadelphia, PA 19104
Elected for 2008-2010 Term T. FIEZ School of EECS Oregon State Univ. Corvallis, OR 97331-3736	B. NAUTA Univ. of Twente 7500 AE Enschede The Netherlands	T. KURODA Keio Univ. Kohoku-ku, Yokohama 223-8522, Japan	J. SEVENHANS AMIs Belgium B1804 Vilvoorde, Belgium	M. SOYUER IBM T. J. Watson Res. Ctr. Yorktown Heights, NY 10598

EDITOR

B. NAUTA, JSSC EDITOR
 University of Twente
 Enschede, The Netherlands
jssc@ewi.utwente.nl

Associate Editors

B. BAAS Dept. Elect. Comput. Eng. Univ. California Davis, CA 95616 bbaas@ucdavis.edu	P. GILLINGHAM Mosaid Technologies Inc. 11 Hines Road Kanata, ON K2K 2X1 Canada fax: (613) 591-8148 gillingham@mosaid.com	A. N. KARANICOLAS ZeroG Wireless, Inc. 255 San Geronimo Way Sunnyvale, CA 94085 (408) 738-7518 fax: (408) 738-7601 ank@zerogwireless.com	S. I. LIU Dept. Electr. Eng. National Taiwan Univ. Taipei 10617, Taiwan R.O.C. fax: (886) 02-2367-1909 lsi@cc.ee.ntu.edu.tw	B. RAZAVI Electr. Eng. Dept. Univ. of California, Los Angeles Los Angeles, CA 90095 (310) 206-1633 fax: (310) 206-8495 razavi@ee.ucla.edu	D. K. SHAEFFER Beceem Communications, Inc. 3960 Freedom Cir., First Floor Santa Clara, CA 95054 fax: (408) 496-0121 dshaeffer@beceem.com.com
A. R. BEHZAD Broadcom Corp. 16340 West Bernardo Dr. San Diego, CA 92127 fax: (858) 521-5622 arya@broadcom.com	K. A. I. HALONEN Dept. Micro & Nano Sci. Helsinki Univ. Technol. 02150 Espoo, Finland fax: +358 9 451 2269 karih@ecdl.tkk.fi	B. KIM Qualcomm Inc. 675 Campbell Technology Pkwy. Campbell, CA 95008 beomsupk@qualcomm.com	P. K. T. MOK Dept. Elect. Electron. Eng. Hong Kong Univ. Sci. Technol. Clearwater Bay, Hong Kong eemok@ee.ust.hk	S. RUSU Intel Corp. 2200 Mission College Blvd. Santa Clara, CA 95052	D. YOUNG Dept. Elect. Eng. Comput. Sci. Case Western Reserve Univ. Cleveland, OH 44106 fax: (216) 368-6039 djy@po.cwru.edu
M. P. FLYNN Dept. EECS Univ. Michigan Ann Arbor, MI 48109-2122 fax: (734) 763-9324 mpflynn@eeecs.umich.edu	S. JAMAL Marvell Semiconductor 5488 Marvell Lane MS 2-301 Santa Clara, CA 95054 sjamal@marvell.com	D. LEENAERTS NXP Semiconductors High Tech Campus 5 5656AE Eindhoven, The Netherlands fax: +31-40-27 44113 Domine.Leenarts@nxp.com	D. NAIRN Dept. Elect. Comput. Eng. Univ. Waterloo Waterloo, ON N2L 3G1, Canada nairn@uwaterloo.ca	J. SAVOJ Qualcomm, Inc. 3165 Kifer Rd. Santa Clara, CA 95051 (408) 216-4282 fax: (408) 533-9632 savoj@iecc.org	
R. GHARPUREY Dept. Elect. Comput. Eng. Univ. Texas at Austin Austin, TX 78712 (512) 232-7940 ranjit@mail.cerc.utexas.edu			S. NATARAJAN TSMC Design Technology 349 Terry Fox Dr. Kanata, ON K2K 2V6, Canada sn@emergingmemory.com		

LEWIS M. TERMAN, *President*
 JOHN R. VIG, *President-Elect*
 BARRY L. SHOOP, *Secretary*
 DAVID G. GREEN, *Treasurer*
 LEAH H. JAMIESON, *Past President*

IEEE Officers

EVANGELIA MICHELI-TZANAKOU, *Vice President, Educational Activities*
 JOHN BAILLIEUL, *Vice President, Publication Services and Products*
 JOSEPH V. LILLIE, *Vice President, Member and Geographic Activities*
 J. ROBERTO B. DE MARCA, *Vice President, Technical Activities*
 GEORGE W. ARNOLD, *President, IEEE Standards Association*
 RUSSELL J. LEFVRE, *President, IEEE-USA*

GIOVANNI (NANNI) DE MICHELI, *Director, Division 1*

IEEE Executive Staff

BETSY DAVIS, *SPHR, Human Resources*
 ANTHONY DURNIAK, *Publications Activities*
 JUDITH GORMAN, *Standards Activities*
 CECELIA JANKOWSKI, *Member and Geographic Activities*
 DOUGLAS GORHAM, *Educational Activities*

MATTHEW LOEB, *Corporate Strategy & Communications*
 RICHARD D. SCHWARTZ, *Business Administration*
 CHRIS BRANTLEY, *IEEE-USA*
 MARY WARD-CALLAN, *Technical Activities*

IEEE Periodicals

Transactions/Journals Department

Staff Director: FRAN ZAPPULLA

Editorial Director: DAWN MELLEY Production Director: PETER M. TUOHY

Managing Editor: MONA MITTRA Senior Editor: ELIZABETH STEWART

IEEE JOURNAL OF SOLID-STATE CIRCUITS (ISSN 0018-9200) is published monthly by The Institute of Electrical and Electronics Engineers, Inc. Responsibility for the contents rests upon the authors and not upon the IEEE, the Society/Council, or its members. **IEEE Corporate Office:** 3 Park Avenue, 17th Floor, New York, NY 10016-5997. **IEEE Operations Center:** 445 Hoes Lane Piscataway, NJ 08854-4141. **NJ Telephone:** +1 732 981 0060. **Price/Publication Information:** Individual copies: IEEE members \$20.00 (first copy only), nonmembers \$77.00 per copy. (Note: Postage and handling charge not included.) Member and nonmember subscription prices available on request. Available on CD-ROM and DVD (see <http://www.sscs.org/jssc/>) as well as in microfiche and microfilm. **Copyright and Reprint Permissions:** Abstracting is permitted with credit to the source. Libraries are permitted to photocopy for private use of patrons, provided the per-copy fee indicated in the code at the bottom of the first page, is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For all other copying, reprint, or republication permission, write to Copyrights and Permissions Department, IEEE Publications Administration, 445 Hoes Lane, Piscataway, NJ 08854-4141. Copyright © 2008 by The Institute of Electrical and Electronics Engineers, Inc. All rights reserved. Periodicals Postage Paid at New York, NY, and at additional mailing offices. **Postmaster:** Send address changes to IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE, 445 Hoes Lane, Piscataway, NJ 08854-4141. GST Registration No. 125634188. CPC Sales Agreement #40013087. Return undeliverable Canada addresses to: Pitney Bowes IMEX, P.O. Box 4332, Stanton Rd., Toronto, ON M5W 3J4, Canada. Printed in U.S.A.

IEEE JOURNAL OF SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



DECEMBER 2008

VOLUME 43

NUMBER 12

IJSCBC

(ISSN 0018-9200)

SPECIAL ISSUE ON THE 2008 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC)

Introduction to the Special Issue on the 2008 IEEE International Solid-State Circuits Conference		
 S. Tsukamoto, S.-I. Liu, S. Heinen, R. Thewes, and J. Lee	2587
DATA CONVERTER PAPERS		
A 108 dB SNR, 1.1 mW Oversampling Audio DAC With A Three-level DEM Technique K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, and P. Baginski	2592
A Noise-Coupled Time-Interleaved Delta-Sigma ADC With 4.2 MHz Bandwidth, -98 dB THD, and 79 dB SNDR K. Lee, J. Chae, M. Aniya, K. Hamashita, K. Takasuka, S. Takeuchi, and G. C. Temes	2601
A 14-b 100-MS/s Pipelined ADC With a Merged SHA and First MDAC B.-G. Lee, B.-M. Min, G. Manganaro, and J. W. Valvano		2613
An Over-60 dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain B. R. Gregoire and U. Moon	2620
A 150 MS/s 133 μ W 7 bit ADC in 90 nm Digital CMOS G. Plas and B. Verbruggen	2631
Highly Interleaved 5-bit, 250-MSample/s, 1.2-mW ADC With Redundant Channels in 65-nm CMOS B. P. Ginsburg and A. P. Chandrakasan	2641
RF PAPERS		
A 52 GHz Phased-Array Receiver Front-End in 90 nm Digital CMOS K. Scheir, S. Bronckers, J. Borremans, P. Wambacq, and Y. Rolain	2651
A Scalable 6-to-18 GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS S. Jeon, Y.-J. Wang, H. Wang, F. Bohn, A. Natarajan, A. Babakhani, and A. Hajimiri	2660
Transmitter Architectures Based on Near-Field Direct Antenna Modulation A. Babakhani, D. B. Rutledge, and A. Hajimiri	2674
A Compact Wideband Front-End Using a Single-Inductor Dual-Band VCO in 90 nm Digital CMOS J. Borremans, A. Bevilacqua, S. Bronckers, M. Dehan, M. Kuijk, P. Wambacq, and J. Craninckx	2693
The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta	2706
Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise A. Mazzanti and P. Andreani	2716
Terahertz CMOS Frequency Generator Using Linear Superposition Technique D. Huang, T. R. LaRocca, M.-C. F. Chang, L. Samoska, A. Fung, R. Campbell, and M. Andrews	2730
A 56-65 GHz Injection-Locked Frequency Tripler With Quadrature Outputs in 90-nm CMOS W. L. Chan and J. R. Long	2739
A Fully-Integrated Quad-Band GSM/GPRS CMOS Power Amplifier I. Aoki, S. Kee, R. Magoon, R. Aparicio, F. Bohn, J. Zuchan, G. Hatcher, D. McClymont, and A. Hajimiri	2747
ANALOG AND WIRELESS COMMUNICATION PAPERS		
A Field-Programmable Analog Array of 55 Digitally Tunable OTAs in a Hexagonal Lattice J. Becker, F. Henrici, S. Trendelenburg, M. Ortmanns, and Y. Manoli	2759
A Current-Feedback Instrumentation Amplifier With 5 μ V Offset for Bidirectional High-Side Current-Sensing J. F. Witte, J. H. Huijsing, and K. A. A. Makinwa	2769

A Low-Noise Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation	<i>C.-H. Hsu, M. Z. Straayer, and M. H. Perrott</i>	2776
Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional-N PLL	<i>K. J. Wang, A. Swaminathan, and I. Galton</i>	2787
Load-Independent Control of Switching DC-DC Converters With Freewheeling Current Feedback	<i>Y.-J. Woo, H.-P. Le, G.-H. Cho, G.-H. Cho, and S.-I. Kim</i>	2798
A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters	<i>W.-Y. Chu, B. Bakkaloglu, and S. Kiaei</i>	2809
A Pulse-Based Ultra-Wideband Transmitter in 90-nm CMOS for WPANs	<i>M. Demirkan and R. R. Spencer</i>	2820
A Fully Integrated 14 Band, 3.1 to 10.6 GHz 0.13 μm SiGe BiCMOS UWB RF Transceiver	<i>O. Werther, M. Cavin, A. Schneider, R. Renninger, B. Liang, L. Bu, Y. Jin, J. Rogers, and J. Marcincavage</i>	2829
UWB Fast-Hopping Frequency Generation Based on Sub-Harmonic Injection Locking	<i>S. Dal Toso, A. Bevilacqua, M. Tiebout, S. Marsili, C. Sandner, A. Gerosa, and A. Neviani</i>	2844
Equalization of Third-Order Intermodulation Products in Wideband Direct Conversion Receivers	<i>E. A. Keehr and A. Hajimiri</i>	2853
A Low-Power WCDMA Transmitter With an Integrated Notch Filter	<i>A. Mirzaei and H. Darabi</i>	2868
A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN	<i>M. Zargari, L. Y. Nathawad, H. Samavati, S. S. Mehta, A. Kheirkhahi, P. Chen, K. Gong, B. Vakili-Amini, J. A. Hwang, S. Chen, M. Terrovitis, B. Kaczynski, S. Limotyakis, M. P. Mack, H. Gan, M. Lee, R. Chang, H. Dogan, S. Abdollahi-Alibeik, B. Baytekin, K. Onodera, S. Mendis, A. Chang, Y. Rajavi, S. H. Jen, D. K. Su, and B. A. Wooley</i>	2882
A Single-Chip CMOS Bluetooth v2.1 Radio SoC	<i>W. W. Si, D. Weber, S. Abdollahi-Alibeik, M. Lee, R. Chang, H. Dogan, H. Gan, Y. Rajavi, S. Luschas, S. Ozgur, P. Husted, and M. Zargari</i>	2896
WIRELINE COMMUNICATION PAPERS		
A T-Coil-Enhanced 8.5 Gb/s High-Swing SST Transmitter in 65 nm Bulk CMOS With < -16 dB Return Loss Over 10 GHz Bandwidth	<i>M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Toift, and M. Schmatz</i>	2905
A 10.3 Gb/s Burst-Mode CDR Using a $\Delta\Sigma$ DAC ...	<i>J. Terada, K. Nishimura, S. Kimura, H. Katsurai, N. Yoshimoto, and Y. Ohtomo</i>	2921
A 40-Gb/s CDR Circuit With Adaptive Decision-Point Control Based on Eye-Opening Monitor Feedback	<i>H. Noguchi, N. Yoshida, H. Uchida, M. Ozaki, S. Kanemitsu, and S. Wada</i>	2929
A 90 nm CMOS DSP MLSD Transceiver With Integrated AFE for Electronic Dispersion Compensation of Multimode Optical Fibers at 10 Gb/s	<i>O. E. Agazzi, M. R. Hueda, D. E. Crivelli, H. S. Carrer, A. Nazemi, G. Luna, F. Ramos, R. López, C. Grace, B. Kobeissy, C. Abidin, M. Kazemi, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo, V. Posse, S. Wang, G. Asmanis, G. Eaton, N. Swenson, T. Lindsay, and P. Voois</i>	2939
Fast Power Transient Management for OC-192 WDM Add/Drop Networks	<i>H.-M. Bae, J. Ashbrook, N. Shanbhag, and A. Singer</i>	2958
Low-Spur, Low-Phase-Noise Clock Multiplier Based on a Combination of PLL and Recirculating DLL With Dual-Pulse Ring Oscillator and Self-Correcting Charge Pump	<i>S. L. J. Gierkink</i>	2967
IMAGERS, MEMS, MEDICAL, AND DISPLAYS PAPERS		
A 128 \times 128 Single-Photon Image Sensor With Column-Level 10-Bit Time-to-Digital Converter Array	<i>C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon</i>	2977
A Multi-Aperture Image Sensor With 0.7 μm Pixels in 0.11 μm CMOS Technology	<i>K. Fife, A. El Gamal, and H.-S. P. Wong</i>	2990
A 5 μW /Channel Spectral Analysis IC for Chronic Bidirectional Brain-Machine Interfaces	<i>A.-T. Avestruz, W. Santa, D. Carlson, R. Jensen, S. Stanslaski, A. Helfenstine, and T. Denison</i>	3006
A 200 μW Eight-Channel EEG Acquisition ASIC for Ambulatory EEG Systems	<i>R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof</i>	3025
A Mode-Matching $\Sigma\Delta$ Closed-Loop Vibratory Gyroscope Readout Interface With a 0.004 $^\circ$ /s/ $\sqrt{\text{Hz}}$ Noise Floor Over a 50 Hz Band ...	<i>C. D. Ezekwe and B. E. Boser</i>	3039
2008 INDEX		3049

A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters

Wing-Yee Chu, Bertan Bakkaloglu, *Senior Member, IEEE*, and Sayfe Kiaei, *Fellow, IEEE*

Abstract—A combined class-AB and switch-mode regulator based supply modulator with a master–slave architecture achieving wide bandwidth and low ripple is presented. Low frequency content of the envelope waveform is provided by a synchronous-rectifier based switch-mode power supply while high frequency content is provided by a rail-to-rail class-AB amplifier. A wide range, low loss output current sensing circuit is used at the class-AB amplifier output, canceling the ripple due to switch-mode power supply and extending overall modulator bandwidth. The proposed regulator is designed and fabricated on a 0.35 μm CMOS process. The combined regulator achieves a maximum efficiency of 82% and an IMD3 of 65 dBc at 10 MHz for 16 dBm output power. The regulator achieves a frequency range up to 10 MHz with less than 0.2% envelope tracking error, making this PA regulator suitable for CDMA applications.

Index Terms—Envelope tracking, supply modulator, PA regulator, CDMA, power amplifier.

I. INTRODUCTION

POWER AMPLIFIERS (PAs) consume a significant portion of the total power budget of battery operated wireless transceivers; therefore, they are the key components for power reduction in mobile systems. Although efficient class D, E, F, and S amplifiers offer power saving solutions for mobile transmission, their inherent non-linear nature creates out-of-band spurious emissions. As shown in Fig. 1, the typical variable envelope linear modulation scheme utilizes a PA at a lower power level compared to its maximum operating power. The backed-off levels can be anywhere between 6 dB to 20 dB, and at these levels more and more power is wasted at the PA, reducing overall PA efficiency. It is highly desirable to track the envelope variations of a modulated waveform at the PA power supply. This variable supply operation ensures close to peak efficiency at various signal envelope levels. Polar modulated transmitters try to address this efficiency loss by closely tracking the envelope of an RF band-pass signal and applying it onto the drain of a high efficiency, non-linear PA. An envelope detector extracts the envelope waveform and this is applied as input to a wideband supply regulator, as shown in Fig. 2 [1],

Manuscript received April 07, 2008; revised July 21, 2008. Current version published December 10, 2008. This work was supported by the National Science Foundation under NSF Award 0533151 and by Texas Instruments Inc. Wireless Terminals Business Unit.

W.-Y. Chu is with the Platform Components Group, Intel Corporation, Chandler, AZ 85224 USA (e-mail: wing-yee.chu@intel.com).

B. Bakkaloglu and S. Kiaei are with the Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287-8406 USA (e-mail: bertan@asu.edu; sayfe@asu.edu).

Digital Object Identifier 10.1109/JSSC.2008.2005743

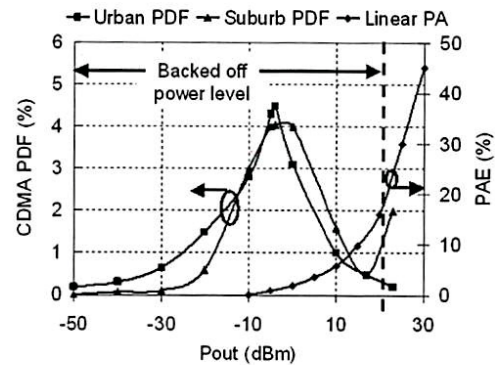


Fig. 1. Typical power density function (PDF) of CDMA handset power levels with respect to the PA efficiency [10], [11].

[2]. By applying the amplitude and phase components of RF signals separately to the power supply and input of non-linear PAs, the efficiency of PAs at backed-off power levels improve significantly. A known drawback of this technique is spectral expansion of envelope and phase bandwidths after envelope extraction. An example of this spectral expansion phenomenon in CDMA signals is shown in Fig. 3. As shown in this figure, -35 dB bandwidth of a composite IS-95 CDMA waveform envelope is approximately three times wider than the same waveform's occupied RF bandwidth. The envelope waveform also has a much higher DC content due to full wave rectification during envelope extraction. System level simulations show that at least 5 MHz bandwidth from the supply modulator for IS-95 CDMA applications is needed in order to minimize its impact on output ACPR. A bandwidth target of 10 MHz is selected to ensure margin across load variations. Another drawback of polar modulation is amplitude and phase path misalignment, which results in spectral regrowth of the transmitted signal [3]. In a similar fashion, fast response wide bandwidth supply modulators with small group delay can minimize this misalignment.

Previously, switch-mode regulators and low dropout (LDO) regulators were proposed for supply modulation [4], [5]. Although switch-mode supply regulators boost efficiency of the PA, their operating bandwidth is limited by the switching frequency. Alternatively, LDO regulators provide wide bandwidth while enhancing the linearity of the PA, but they are inefficient at backed-off power levels. Recently, combined linear and switch-mode supply modulation techniques are gaining attention for RF PA supply implementations [6], [7], [1].

In this paper, a master–slave linear and switch-mode supply modulator with fast dynamic transient response is presented. By

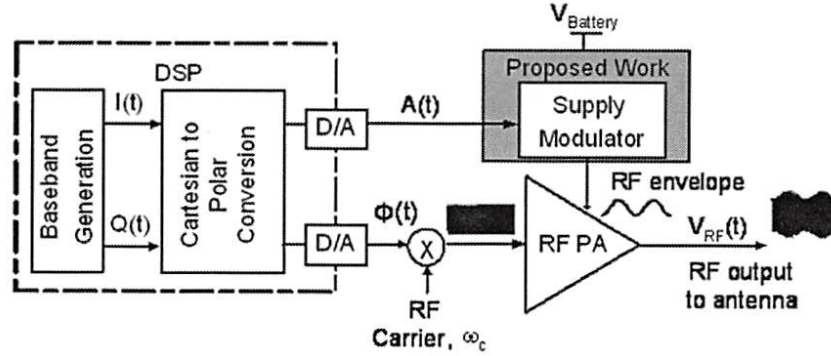


Fig. 2. Typical polar modulation based transmitter block diagram.

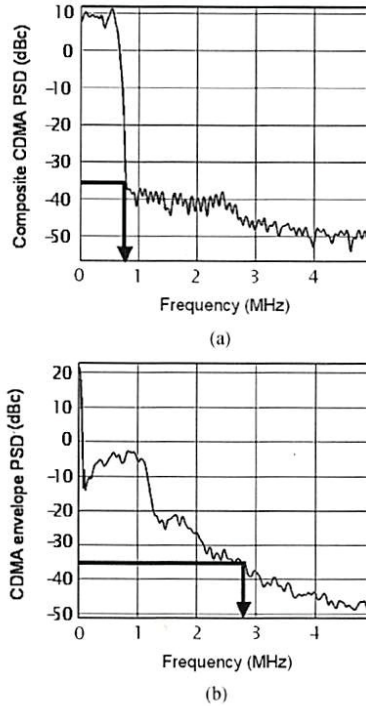


Fig. 3. Power spectral density (PSD) of (a) composite CDMA signal and (b) its extracted envelope.

using an accurate current sensing technique, efficiency and linearity of the supply modulator is further optimized. The organization of this paper is as follows: Section II describes the operation of the PA supply modulator and techniques for performance optimization. Section III details the circuit level implementations of the linear amplifier, switch-mode regulator and current sensing circuit. The measurement setup and results are presented in Section IV, followed by a conclusion in Section V.

II. DESIGN OF MASTER-SLAVE PA REGULATOR

A. Operation

Fig. 4 shows the block diagram of the proposed master-slave linear and switch-mode combined supply modulator loaded

with a PA. A high GBW linear amplifier in voltage follower configuration ensures that output node $V_o(t)$ tracks the reference envelope voltage $A(t)$. A current sensing circuit, high gain transimpedance amplifier and switch-mode regulator forms a global feedback control loop that suppresses the current output from the linear amplifier within the switch-mode regulator bandwidth. Consequently, a large portion of the load current is provided by the switch-mode regulator. The lower efficiency linear amplifier sources small amounts of output current $I_{lin}(t)$ to cancel out switch-mode regulator ripple and high frequency signal content. The transient response of currents at the output of the switch-mode regulator $I_{sm}(t)$, the linear amplifier $I_{lin}(t)$ and combined master-slave supply modulator $I_o(t)$ is shown in Fig. 5. Assuming an infinite GBW linear amplifier, this architecture will generate a ripple free output current $I_o(t)$ to the load. However, due to finite GBW of the linear amplifier, only the ripple energy within the linear amplifier is cancelled. This tradeoff between GBW of linear amplifier and ripple size will be discussed later.

To gain further insight on the operation of master-slave supply modulators, the current-mode frequency response of the linear amplifier, switch-mode regulator, and their combined response are analyzed. The steady state output current of switch-mode regulator I_{sm} can be defined by the linear regulator current I_{lin} as follows:

$$I_{sm} = \frac{I_{lin}}{n} \cdot A_{tia} \cdot \frac{1}{S_r} \cdot \frac{1}{1 + s^2 \cdot L \cdot C} \cdot \frac{1}{R_L} \quad (1)$$

where n is the current sense ratio, A_{tia} is the transimpedance gain, S_r is the slope of the ramp in the switch-mode regulator and R_L is the equivalent PA load resistance. The sensed current is amplified by the transimpedance amplifier, comparator and the voltage divider formed by equivalent series resistance (ESR) of the loading inductor and resistive component R_L of the PA load. The second-order LC filter and the ESR set the dominant pole location of the frequency response.

From (1), we can derive the transfer function of the combined output current I_o as follows:

$$\frac{I_o}{A} = \frac{1}{R_L} \cdot \frac{1}{1 + \frac{1}{A_{tia}}} \quad (2)$$

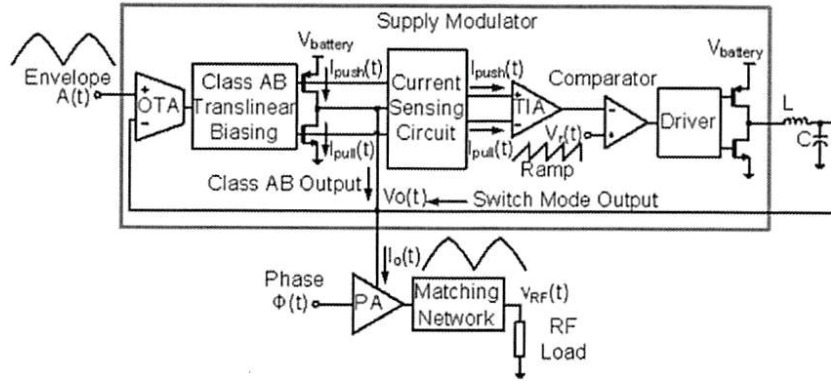


Fig. 4. The proposed master-slave linear and switch-mode PA regulator block diagram.

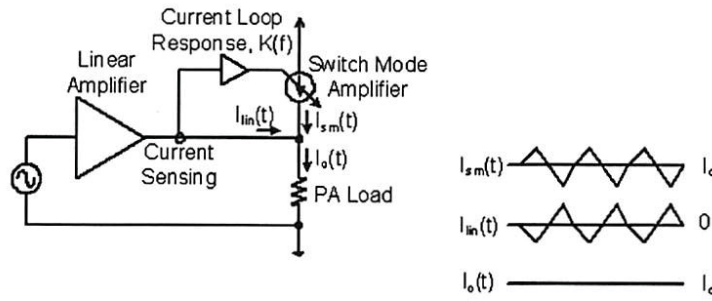


Fig. 5. Simplified block diagram of the proposed regulator showing ripple cancellation.

where A represents the input envelope signal and A_{lin} is the open loop gain of the linear amplifier. The switch-mode regulator output current I_{sm} can be shown as

$$\frac{I_{sm}}{A} = \frac{1}{1 + \frac{n \cdot S_r \cdot (1 + s^2 \cdot L \cdot C) \cdot R_L}{A_{tia}}} \cdot \frac{1}{R_L} \cdot \frac{1}{1 + \frac{1}{A_{lin}}} \quad (3)$$

and finally the linear amplifier output current I_{lin} is represented by

$$\frac{I_{lin}}{A} = \frac{n \cdot S_r \cdot (1 + s^2 \cdot L \cdot C)}{A_{tia}} \cdot \frac{1}{1 + \frac{1}{A_{lin}}} \quad (4)$$

As shown in (3) and (4), the output current response of the switch-mode amplifier has a two-pole transfer function forming a second-order low-pass characteristic, while the output current response of the linear amplifier has a two-zero transfer function that contains a second-order high-pass characteristic. At low frequencies, the linear amplifier current output is suppressed and the switch-mode regulator dominates the output current. Conversely, at high frequencies, the switch-mode regulator current response starts rolling off and the linear amplifier takes over the output current. The switch-mode regulator and linear amplifier current response combine and form a flat frequency response for the master-slave regulator. The frequency where switch-mode regulator current response rolls off and linear amplifier current response takes over is called transition frequency, f_T . This frequency plays an important role on efficiency optimization and will be discussed in the next section.

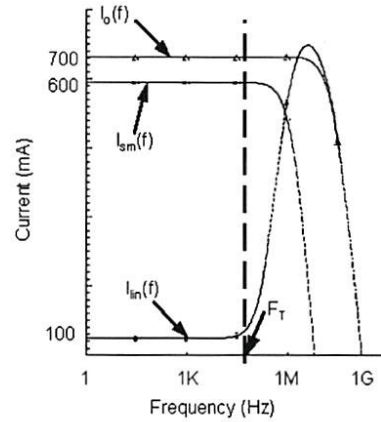


Fig. 6. Current-mode frequency response of the linear amplifier, the switch-mode regulator and the master-slave combined regulator.

Fig. 6 plots the current-mode frequency response of the linear amplifier, switch-mode regulator and master-slave regulator. As predicted in the mathematical analysis, second-order low-pass and high-pass characteristics were obtained. The resulted flat output current response is suitable for high linearity implementation. In addition, the overall bandwidth extended by the linear amplifier makes the supply modulator suitable for wide bandwidth signal transmission.

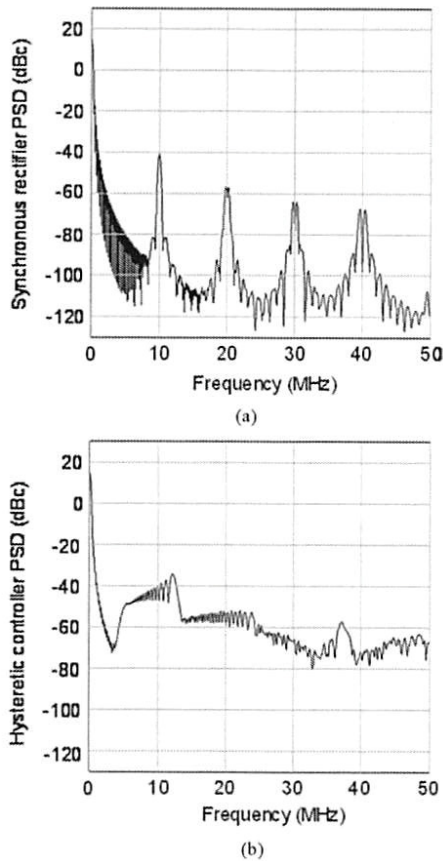


Fig. 7. Ripple energy for a 10 dBm, 100 kHz SSB suppressed carrier modulation waveform for (a) a synchronous rectifier versus (b) a hysteretic controller.

B. Performance Optimization

Master-slave regulator configuration is commonly used for audio amplifiers, and for these applications a switch-mode regulator is typically configured in hysteretic control mode. Hysteretic controllers do not need a clocked comparator; instead they use a window comparator, and frequency of operation depends on the load conditions. The loop response of hysteretic controllers is quite fast during load transients. However, this variable frequency operation generates wideband spurious emissions at the regulator output. This in turn increases the AC power from the linear amplifier since more ripple energy falls within class-AB amplifier bandwidth. The two power spectral density plots in Fig. 7 represent the ripple energy for a 10 dBm, 100 kHz single sideband (SSB) suppressed carrier modulation waveform for a synchronous rectifier versus a hysteretic controller. As shown in this figure, the integrated ripple energy within the class-AB bandwidth is much higher for a hysteretic controller. For wideband modulation schemes, this analysis shows that synchronous rectifiers are a better choice for low power, low spurious emissions design.

To optimize the efficiency of a PA supply modulator, two properties of the envelope signals should be considered: the power level probability density function (PDF) discussed in Fig. 1 and power spectral density (PSD). As shown in Fig. 3,

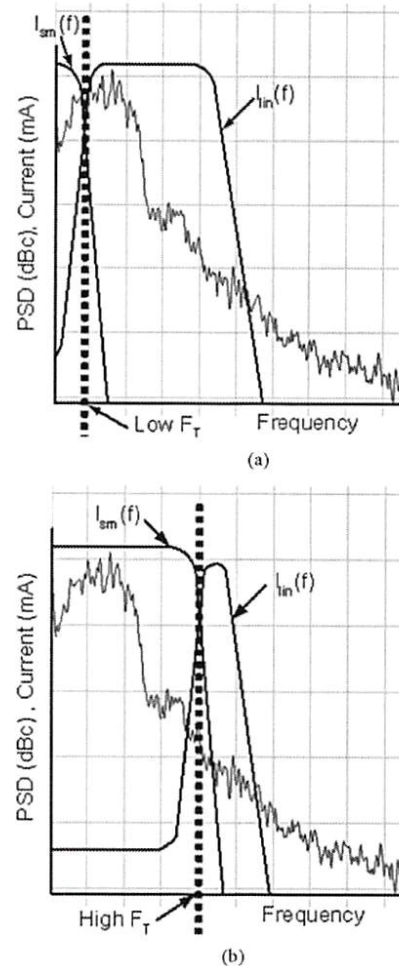


Fig. 8. Portion of CDMA spectrum amplified by linear amplifier and switch-mode regulator at (a) low f_T and (b) high f_T .

the envelope PSD contains high DC content and most of the envelope energy is accumulated at frequencies less than 2 MHz with a small portion of the envelope energy rolling off at higher frequencies. The bandwidth specifications of the switch-mode regulator can be relaxed further reduce the switching losses and use the linear amplifier to amplify the high frequency portion of the signal. However, as the bandwidth of the high efficiency linear amplifier becomes too low, the low efficiency linear amplifier dominates the output current, reducing overall efficiency. Fig. 8 shows the portions of the envelope spectrum amplified by the linear amplifier and switch-mode regulator with different transition frequencies f_T . Fig. 9 shows that peak efficiency of the supply modulator with a 20 dBm, 400 kHz SSB suppressed carrier modulated input waveform is achieved at 100 kHz f_T .

As discussed earlier, output ripple is another critical specification requirement for PA supply modulator design due to stringent ACPR and spurious emission requirements. [8]. In the proposed master-slave linear and switch-mode regulator, a significant portion of current ripple from the switch-mode

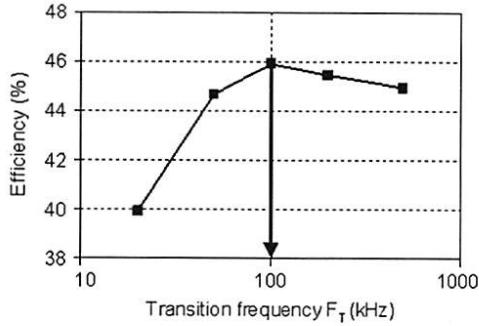


Fig. 9. Efficiency optimization of a 20 dBm, 400 kHz SSB suppressed carrier modulation envelope waveform by varying transition frequency f_T .

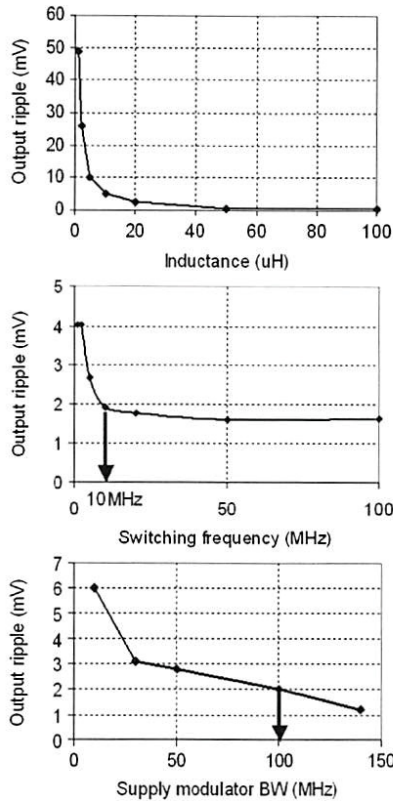


Fig. 10. Peak-to-peak output voltage ripple versus (a) load inductor, (b) switching frequency, and (c) linear amplifier GBW.

regulator is cancelled by the linear amplifier. This results in a much smaller residue voltage and current ripple at the PA drain. Output inductor and switching frequency also play an important role on output ripple value. Fig. 10(a) and (b) shows output ripple versus load inductor and switching frequency for the proposed composite regulator. Since both ripple frequency and output filter corner is determined by the transition frequency, these parameters cannot be used for ripple optimization. Therefore, the effectiveness of current ripple cancellation depends on the GBW of the linear amplifier. For the ripple specification, we have assumed a worst case PA power supply rejection (PSR) of

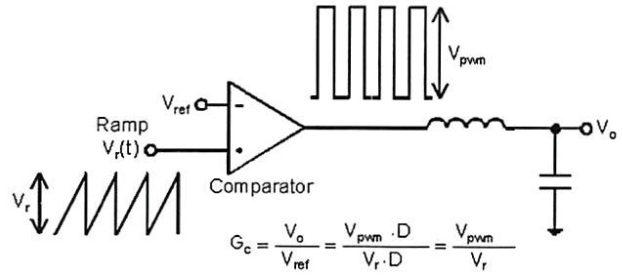


Fig. 11. Gain calculation in comparator. D is the duty cycle of $V_{pwm}(t)$.

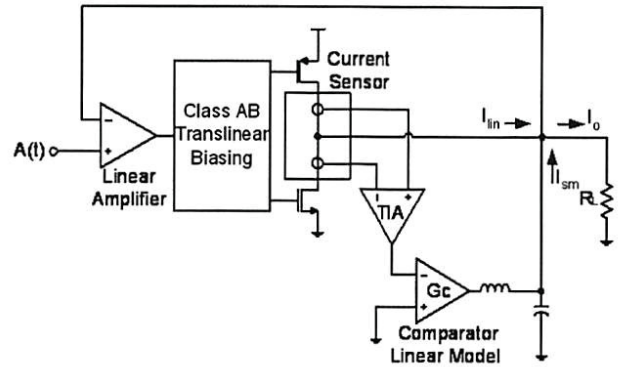


Fig. 12. Linear model for master-slave linear and switch-mode regulator.

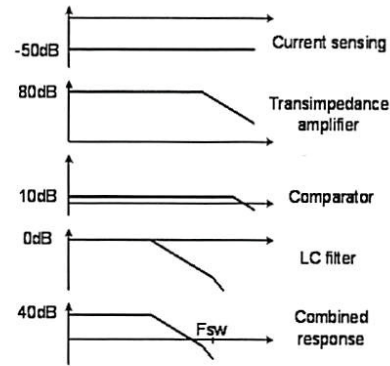


Fig. 13. Individual block and the combined frequency responses in switch-mode regulator feedback loop.

0 dB and used -55 dBc per 30 kHz bandwidth ACPR requirements to extract a maximum ripple specification of 2 mV_{pp} at the overall regulator output [8]. As shown in Fig. 10(c), as the linear regulator unity gain-bandwidth increases, the voltage ripple at the output reduces, with the expense of reduced efficiency and increased linear regulator power consumption. For a given 2 mV_{pp} ripple specification at a typical 16 dBm output power level, a linear regulator unity gain-bandwidth of 100 MHz is selected.

C. Switch-Mode Regulator Feedback Loop

The switch-mode regulator feedback loop includes a current sensing circuit, an error amplifier, a comparator, power stage and a low-pass filter and is designed with maximum loop gain for

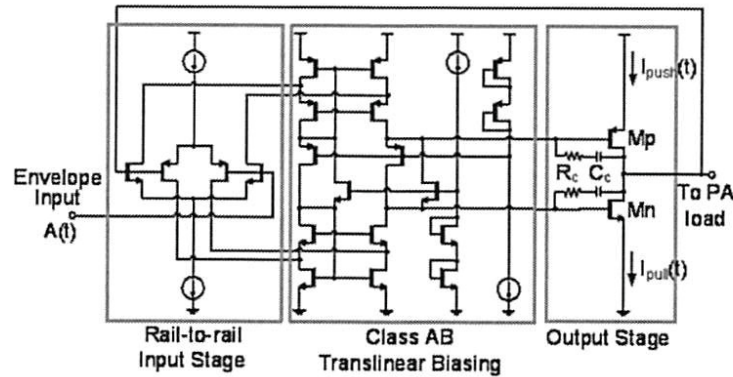


Fig. 14. Rail-to-rail input linear class-AB amplifier with common-source output stage in voltage follower configuration for ripple cancellation and master-slave supply modulator bandwidth extension.

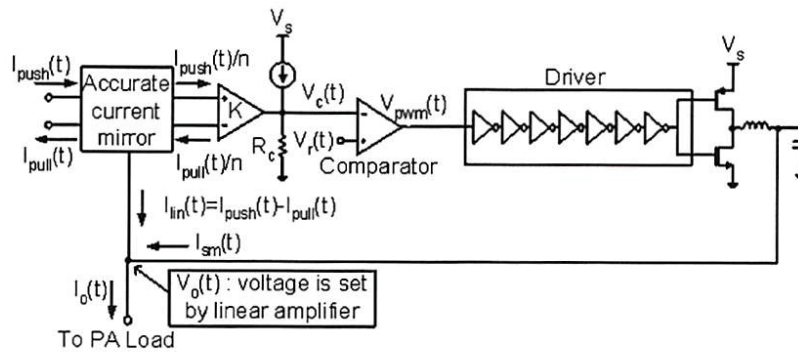


Fig. 15. Switch-mode regulator in master-slave supply modulator for high efficiency amplification.

accurate envelope tracking and highest linear amplifier output current suppression. For AC analysis, a linear model is utilized. As shown in Fig. 11, linearized gain of the comparator is defined by the ratio of its output voltage swing to the amplitude of its ramp input. $V_{pwm}(t)$ is the switching version of $V_o(t)$ that has equal magnitude but contains stronger and more high-frequency harmonics. A linear model is obtained and Fig. 12 shows the linearized model of the system.

In the comparator design a ramp voltage swing of 0.3 V is used, yielding an equivalent gain of 10. This gain is optimized in such a way that there is minimum penalty to the loop bandwidth and phase margin. The disadvantage of using a smaller ramp voltage is the increased comparator response time. This delay results in degradation in envelope tracking accuracy of the switch mode output current and consumes more linear amplifier output current to correct the time delay errors. Furthermore, excess comparator delays degrade the phase margin of the feedback loop around the combined regulator. In this design, with the switching frequency of the supply modulator at 10 MHz and a comparator BW of 96 MHz, the comparator achieves a response time of less than 6 ns. The delay introduces a phase shift of less than 1° and requires almost no extra current from the linear amplifier.

To ensure the stability of the feedback loop in the switch-mode regulator, the bandwidth of the switch-mode regulating

loop should be at least ten times less than the switching frequency. The limited operating bandwidth filters the high frequency contents of the output current ripple and prevents instability. To minimize current use from the linear amplifier, close loop gain should be high. There is also a gain-attenuation at the output of the switch-mode regulator: the ESR and resistive load form a voltage divider that degrades the loop gain. Small ESR is preferred to minimize attenuation and power losses.

Fig. 13 plots the frequency response of each block inside the switch-mode regulating loop. It shows that the total current to voltage conversion gain of current sensing and transimpedance stage is approximately 30 dB, followed by a comparator gain of 10 dB yielding an in-band gain of 40 dB. The transimpedance error amplifier and comparator are designed to have wide BW. Their poles should place beyond the GBW of the switch-mode regulator. The loading inductor sets the GBW of the close loop below switching frequency.

III. CIRCUIT IMPLEMENTATION

A. Linear Amplifier

A two-stage class-AB amplifier with a common-source output stage, as shown in Fig. 14, is used for the linear amplifier. The input stage is designed rail-to-rail in order to enable arbitrary feedback configurations, including unity gain

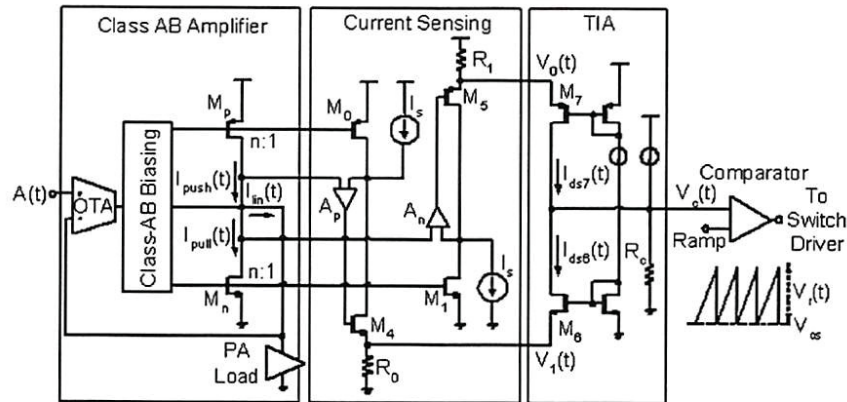


Fig. 16. Accurate current sensing circuit sensing the load current in class-AB amplifier and transimpedance amplifier driving the comparator load.

follower. System level simulations show that voltage follower configuration provides the highest efficiency with minimum group delay without the need for driving the passive feedback network. System level models also show that input *gm*-control circuitry is not required for the envelope tracking application due to asymmetric nature of the envelope waveform. Because the load resistance ranges from 3.33 Ω to 8.4 Ω, the output pole is nominally set at 200 MHz for a 100 pF load capacitor to ensure stability. The rail-to-rail input stage achieves 100 MHz GBW with a load capacitance of 100 pF.

B. Switch-Mode Regulator

In the master–slave regulator configuration, the switch-mode regulator serves as the slave stage, as shown in Fig. 15, and is driven by the class-AB amplifier sensed output currents. The transresistance gain of 10 k Ω in the current-to-voltage conversion stage enhances the switch-mode loop gain, increasing the accuracy of the current-mode amplifier. The synchronous rectifier utilizes a single-stage asynchronous latched comparator with worst case settling time of 6 ns. The gate driver uses seven cascaded tapered inverter stages, which is optimized for minimum delay. The size of the external *LC* filter and power stage is designed for optimum efficiency. The GBW of the switch-mode regulator is designed to be 100 kHz, and the switching frequency is set at 10 MHz. The power stage is sized to obtain minimum gate drive and on-resistance loss. In order to ensure the stability of the linear amplifier, the load capacitance needs to be limited to 100 pF, yielding an inductor value of 20 μH for minimum output current ripple and ESR.

C. Accurate Current Sensing and Switch-Mode Regulator Input Referred Offset Reduction

In order for the current feedback mechanism to track the input envelope accurately, the input referred system offset must be minimized. Typical current sensing techniques utilize a small series resistor and measure the voltage drop across it [9]. Although this approach can sense load current accurately, it is not suitable for CDMA supply modulator applications where output currents can be up to 380 mA. In the proposed accurate current sensing circuit shown in Fig. 16, transistors $M_p - M_0 - A_p$ and $M_n - M_1 - A_n$ together form two low-loss accurate cur-

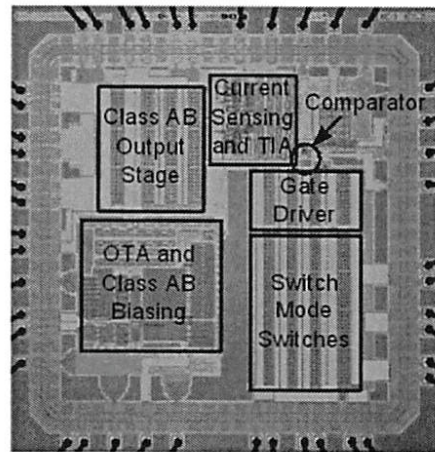


Fig. 17. Chip micrograph of master–slave linear and switch-mode supply modulator.

rent mirrors sensing output push and pull currents $I_{push}(t)$ and $I_{pull}(t)$ from the class-AB amplifier. The load currents in the class-AB output stage formed by M_p and M_n is mirrored with 250:1 ratio to M_0, M_1 and passed through the sense resistances R_0 and R_1 . To increase the operating voltage range of the current mirrors and achieve a high current sensing accuracy, a DC pedestal current source I_s is added to guarantee transistors M_4 and M_5 always stay in saturation. The BW of the current sensing circuit was limited by the GBW of the gain-enhancing amplifiers A_p and A_n at the current mirrors. With the use of moderate gain, rail-to-rail input swing, folded cascode amplifiers A_p and A_n , the current sensing circuit achieves less than 0.2% error and 10 MHz bandwidth.

In the sensing circuit inside switch-mode feedback loop, matched resistor pairs R_0 and R_1 convert the sensed currents, copied accurately by the current sensing circuit, to voltages separately. The converted voltages $V_0(t)$ and $V_1(t)$ modulate gate-source voltages of M_6 and M_7 and generate a replica current across transistors M_6 and M_7 with some gain. Drain currents of M_6 and M_7 are summed and converted back to control voltage $V_c(t)$ by R_c for the PWM controller. To minimize

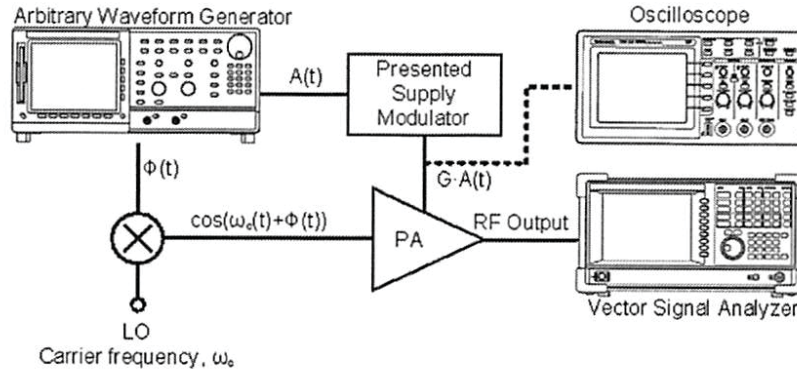


Fig. 18. Typical measurement setup for transient and spectral density analysis.

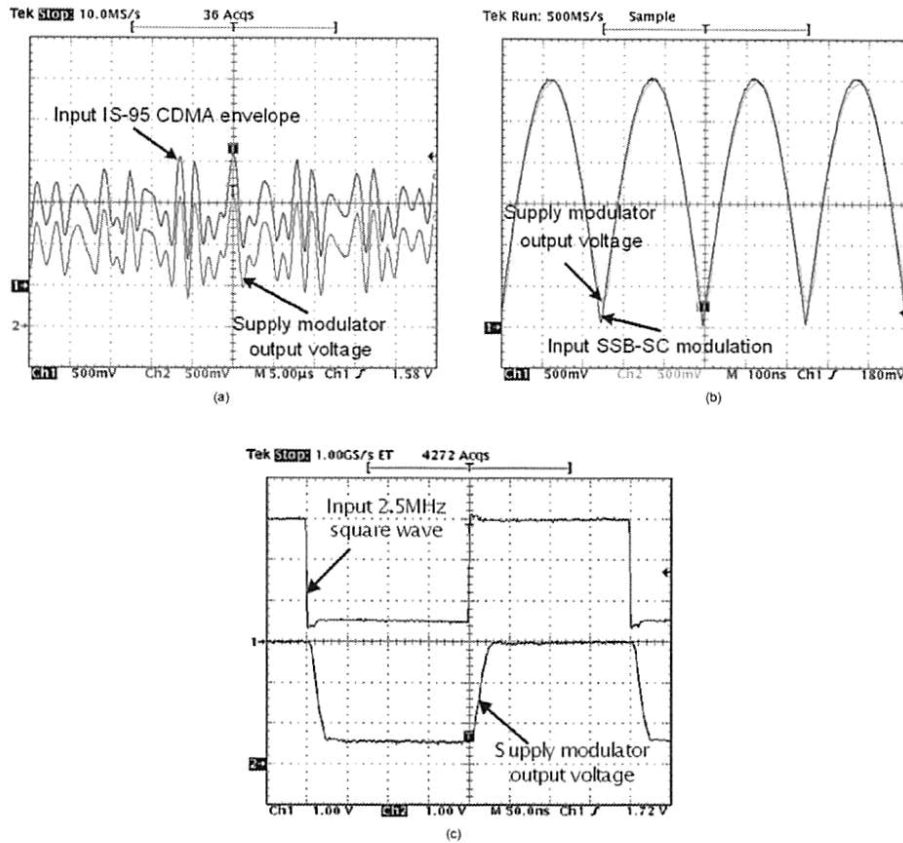


Fig. 19. Transient response of (a) CDMA envelope waveform with commercial PA load (CDMA signal baseline shifted for clarity), (b) 30 dBm, 400 kHz SSB suppressed carrier envelope waveform and (c) $2.5 V_{pp}$, 2.5 MHz square waveform with 4.4Ω resistive load.

input referred offset, the DC level of the input ramp is adjusted to cancel any system mismatches inside the current sensing circuit and transimpedance amplifier.

IV. TEST RESULTS

The master-slave, class-AB and switch-mode supply modulator is fabricated in a $0.35 \mu\text{m}$, 4-level metal CMOS process and occupies a total core area of 4.6 mm^2 excluding the bondpads. A die micrograph of the IC with the pad ring is shown

in Fig. 17. The fabricated chip was packaged in a 44-pin LCC package and mounted to a double-sided FR4 PCB for characterization.

A typical lab setup for the transient and spectral density characterization is shown in Fig. 18. Mathematical modeling software is used to generate amplitude and phase information of an arbitrary waveform, and these vectors are uploaded to an arbitrary waveform generator. An external mixer module is installed for narrowband modulation of the phase to 835 MHz center frequency for the PA characterization. The supply modulator has

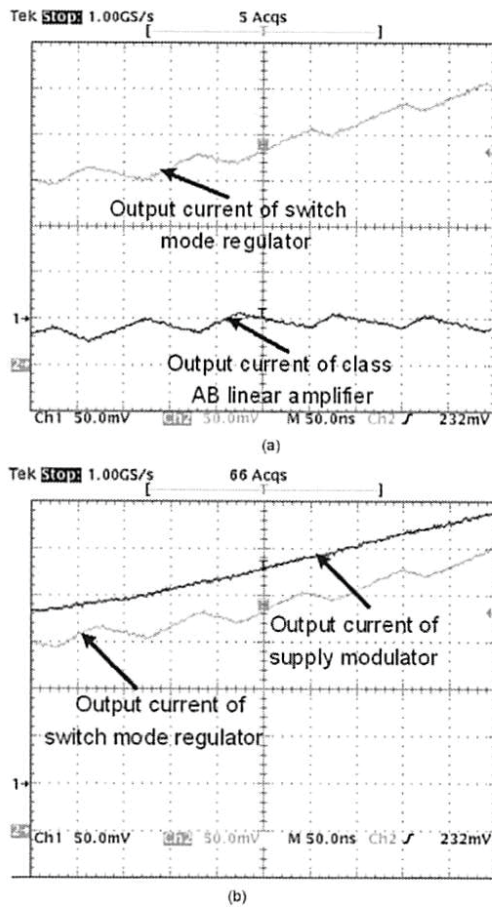


Fig. 20. Details transient response showing switching current ripple cancellation taken place at the output-summing node with 4.4 Ω resistive load.

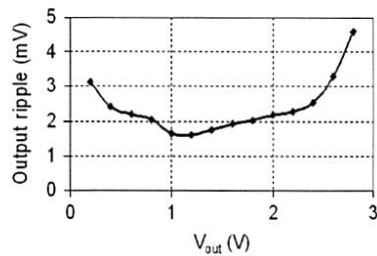


Fig. 21. Peak-to-peak output voltage ripple versus output voltage.

been tested with a 4.4 Ω resistive load with a 100 pF capacitive load and a commercial saturated PA load.

Fig. 19(a) and (b) represents a typical transient response of a CDMA envelope waveform and a 30 dBm, 400 kHz SSB suppressed carrier envelope waveform in a master–slave supply modulator with 4.4 Ω load. Fast transients at the envelope edges represent a challenge to the wideband regulator. Fig. 19(c) indicates the output transient signal settle within 60 ns with a 4.4 Ω resistive load. Fig. 20 details the current ripple cancellation take place at the output-summing node of the master–slave supply modulator. Typical output current ripple and its opposite

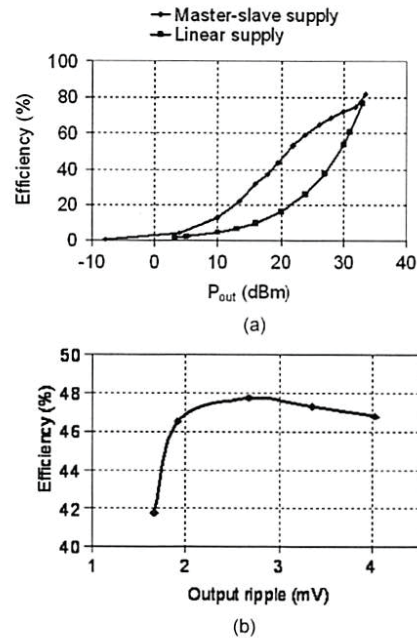


Fig. 22. (a) Efficiency comparison between linear modulator and master–slave supply modulator at different load levels. (b) Peak-to-peak ripple versus efficiency trade-off in supply modulator.

phase cancellation current from the class-AB amplifier are characterized with external 1 Ω sense resistors. As shown in the plot close to 25 mA, ripple is being cancelled by the linear regulator. Fig. 21 plots the peak-to-peak output ripple voltage at different dc levels. Fig. 22(a) compares the efficiency of the standalone class-AB supply modulator with the master–slave supply modulator at different dc levels. Maximum efficiency of the master–slave modulator is 82% and its dynamic range is 65 dBc. The efficiency of the master–slave supply modulator is three times higher than the efficiency of the linear amplifier at 16 dBm output power and indicates a significant efficiency improvement over the linear supply modulator at backed-off power levels. Based on lab characterizations shown in Fig. 22(b) modulator efficiency is found to be optimum at 2.7 mV ripple. In this characterization, the switching regulator bandwidth is modified to sweep different ripple levels. A commercial PA is used to characterize the ACPR performance of the proposed regulator system with a composite IS-95 CDMA waveform. The ACPR measurement is found in Fig. 23(a). At worst-case in-band power levels, the ACPR1 and ACPR2, 885 kHz and 1.98 MHz offset from the center frequency, are more than 46.6 and 57.4 dB, which meet the spectral mask density requirement for IS-95 CDMA transmission. A far-out plot of spectral density of the composite CDMA waveform is shown in Fig. 23(b). At 10 MHz offset from the center frequency, switching ripple adds less than –65 dB tonal content to the output spectrum. Table I summarizes the linearity and efficiency performance of the master–slave supply modulator. With 3.3 V power supply, the regulator can provide 750 mA peak current with a quiescent power consumption of 24 mA. The 2-tone SFDR at 10 MHz with commercial PA load achieves –65 dBc.

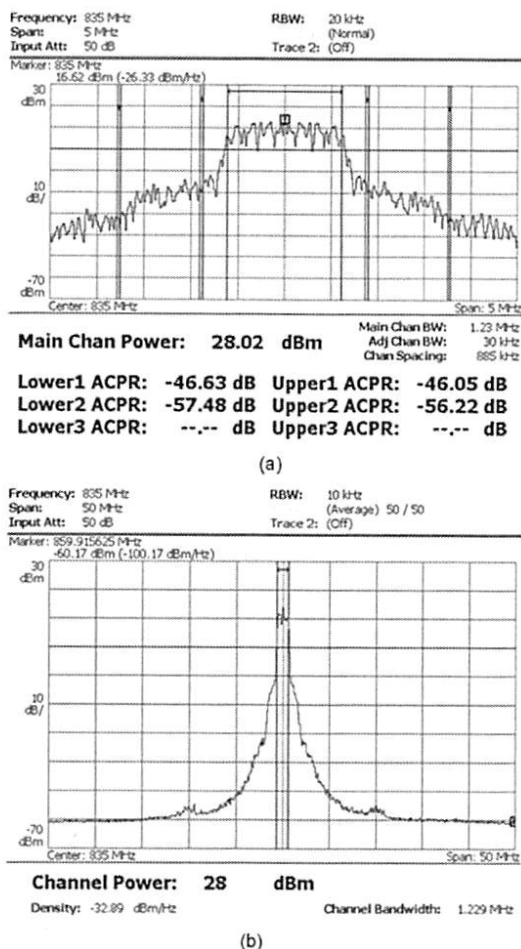


Fig. 23. (a) ACPR of IS-95 CDMA waveform with 5 MHz span (b) PSD with 50 MHz span with less than -65 dBc switching noise.

TABLE I
PERFORMANCE SUMMARY OF MASTER-SLAVE CLASS-AB AND SWITCH-MODE SUPPLY MODULATOR WITH COMMERCIAL PA LOAD

Parameters	Values
Technology	0.35 μ m CMOS
Die area	2.1mm x 2.2mm
Supply voltage	3.3V
Output voltage range	0.3 – 3V
Output RMS current	0 – 750mA
Bandwidth	DC – 10MHz
Linear amplifier quiescent current	24mA
2-tone SFDR at 10MHz	-65dBc
Modulator peak efficiency	82%
Switching frequency	10MHz

V. CONCLUSION

A wideband master–slave class-AB and switch-mode combined supply modulator fabricated on a 0.35 μ m CMOS technology is presented. A master class-AB regulator cancels distortion, supply noise and ripple associated with a switch-mode regulator, while providing high frequency signal content. A high linearity, high efficiency current sensing circuit

is used to sense the class-AB amplifier output. This signal is fed-forward to a current-controlled synchronous rectifier based regulator providing the output envelope content within its bandwidth. The measurement results demonstrate that the combined regulator has less than 2 mV_{pp} ripple at its output with 65 dBc SFDR and peak efficiency of 82% achieving 10 MHz bandwidth. The master–slave supply modulator regulated PA satisfies the CDMA spectral mask requirements.

REFERENCES

- [1] W. Y. Chu, B. Bakaloglu, and S. Kiaei, "A 10 MHz bandwidth 2 mV ripple PA regulator for CDMA transmitters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2008, vol. 51, pp. 448–449, 626.
- [2] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microw. Theory Tech.*, vol. 46, pp. 2220–2225, 1998.
- [3] F. H. Raab, "Intermodulation distortion in Kahn-technique transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 44, pp. 2273–2278, 1996.
- [4] G. Hanington, C. Pin-Fan, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, pp. 1471–1476, 1999.
- [5] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2598–2608, 2005.
- [6] J. Kitchen, W. Y. Chu, I. Deligoz, S. Kiaei, and B. Bakaloglu, "Combined linear and Δ -modulated switched-mode PA supply modulator for polar transmitters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2007, vol. 50, pp. 82–83, 885.
- [7] T. W. Kwak, M. C. Lee, and G. H. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2666–2676, 2007.
- [8] *Recommended Minimum Performance Standards for CDMA 2000 Spread Spectrum Mobile Stations Release C*, 3 GPP2, 2004.
- [9] R. A. R. van der Zee and E. A. J. M. van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, pp. 985–991, 1999.
- [10] MAX2264 PA Datasheet, Maxim IC.
- [11] S. Egoif, "Intelligent power management: A method to improve 2 G/3 G handset talk time," *Microwave J.*, Jul. 2007.



Wing-Yee Chu received the B.S. and M.S. degrees in electrical engineering from Iowa State University, Ames, in 1999 and 2002. She received the Ph.D. in electrical engineering from Arizona State University, Tempe, in 2008.

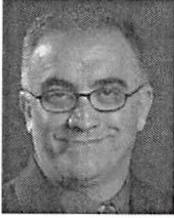
She worked as an intern at the Power Management Group at Texas Instruments Inc., Merrimack, NH, in 2000 and the Communications Circuits Laboratory at Intel Corp., Hillsboro, OR, in 2007. She joined the Platform Components Group at Intel Corp., Chandler, AZ, in 2008. Her research interests include supply modulators for power amplifiers and power management circuits.



Bertan Bakaloglu (M'95–SM'07) received the Ph.D. degree from Oregon State University in 1995.

He joined Texas Instruments Inc. Mixed Signal Wireless Design Group, Dallas, TX, working on analog, RF and mixed-signal front-ends for wireless and wireline communication ICs. He worked on system-on-chip designs with integrated battery management and analog baseband functionality as a design leader. In 2001, he joined the Broadband Communications group, working on cable modem analog front-end designs and Gigabit Ethernet front-ends. In 2004, he joined the Electrical Engineering Department, Arizona State University, Tempe, as an Associate Professor. His research interests include RF and PA supply regulators, RF synthesizers, high-speed RF data converters and RF built-in-self-test circuits for communication ICs.

Dr. Bakaloglu has been a technical program chair for ISCAS and MTT/RFIC conferences. He holds three patents.



Sayfe Kiaei (M'87–SM'93–F'02) was a Senior Member of Technical Staff with the Wireless Technology Center and Broadband Operations at Motorola from 1993 to 2001, where he was responsible for the development of wireless transceiver ICs, and digital subscriber lines (DSL) transceivers. Before joining Motorola, he was an Associate Professor at Oregon State University from 1987 to 1993, where he taught courses and performed research in digital communications, VLSI system design, advanced CMOS IC design, and wireless systems. He is currently a Professor and the Director of the Connection One Center (NSF I/UCRC Center) at Arizona State University, Tempe. He assisted

in the establishment of the Industry-University Center for the Design of Analog/Digital ICs (CDADIC) and served as a Co-Director of CDADIC for 10 years.

Dr. Kiaei is an IEEE Fellow and a member of the IEEE Circuits and Systems Society, IEEE Solid State Circuits Society, and IEEE Communication Society. He has been on the technical program committee and/or chair of many conferences, including: RFIC, MTT, ISCAS, and other international conferences. He has published over 100 journal and conference papers and holds several patents and his research interests are in wireless transceiver design, RF and Mixed-Signal IC's in CMOS and SiGe. He is a recipient of the Carter Best Teacher Award, Oregon State College of Engineering, the IEEE Darlington Award, and the Motorola 10X Design Award.