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A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters

Tae-Woo Kwak, *Student Member, IEEE*, Min-Chul Lee, *Student Member, IEEE*, and Gyu-Hyeong Cho, *Member, IEEE*

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***Abstract*—This paper presents a hybrid switching amplitude modulator for class-E2 EDGE polar transmitters. To achieve both high efficiency and high speed, it consists of a wideband buffered linear amplifier as a voltage source and a PWM switching amplifier with a 2 MHz switching frequency as a dependent current source. The linear amplifier with a novel class-AB topology has a high current-driving capability of approximately 300 mA with a bandwidth wider than 10 MHz. It can also operate on four quadrants with very low output impedance of about 200 mΩ at the switching frequency attenuating the output ripple voltage to less than 12 mV_{pp}. A feedforward path, a PWM control, and a third-order ripple filter are used to reduce the current burden of the linear amplifier. The output voltage of the hybrid modulator ranges from 0.4 to 3 V for a 3.5 V supply. It can drive an RF power amplifier with an equivalent impedance of 4 Ω up to a maximum output power of 2.25 W with a maximum efficiency of 88.3%. The chip has been fabricated in a 0.35 μm CMOS process and occupies an area of 4.7 mm^2.**

***Index Terms*—Buffer, class AB, dc–dc converter, EDGE, low dropout (LDO), low output impedance, operational amplifier, polar transmitter, power amplifier (PA), pulsewidth modulation (PWM), switching amplifier.**

I. Introduction

EVEN THOUGH amplitude variations of a phase-modulated carrier require inefficient linear RF power amplifiers, recent wireless systems tend to use amplitude modulation as well as phase modulation to achieve a high data rate. Polar transmitters as shown in Fig. 1 are known as good candidates for such high-data-rate systems because they can obtain high efficiency by using efficient switched-mode RF power amplifiers. However, when a complex signal is being split into its amplitude and phase components, the bandwidth of each component becomes wider than that of the original signal [1], [2]. This is why wideband low-dropout (LDO) linear amplifiers are still used in the amplitude path of most polar transmitters in spite of their low efficiencies. Recently, many efforts have been made to replace LDO amplifiers with switching ones to obtain better efficiency. Nevertheless, a switching amplifier has difficulty in efficiently following a high-frequency amplitude signal because a high switching frequency is required, and switching loss increases with switching frequency. Moreover, it has been implemented with many external components or expensive high-speed processes such as GaAs or SiGe. Although a CMOS amplitude modulator based on the concept of interleaving delta modulation has been suggested in [3], it still consumes considerable power and requires many external components—especially binary-weighted inductors. However, our proposed CMOS hybrid switching amplifier achieves both high speed and high efficiency through the combination of a wideband linear amplifier with a very efficient switching amplifier.

The organization of this paper is as follows. In Section II, we review the concept of the hybrid switching amplifier and present the auxiliary circuits, such as a feedforward path and a third-order ripple filter. In Section III, we present the proposed low-output-impedance buffer amplifier. In Section IV, we discuss the experimental results. Finally, in Section V, we present our conclusions.

II. Hybrid Switching Amplifier

A. *Concept of a Conventional Hybrid Switching Amplifier*

As shown in Fig. 2(a), the hybrid switching amplifier has a master–slave structure consisting of a wideband linear amplifier as a voltage source and a switching amplifier as a current-controlled current source. The wideband linear amplifier accurately controls the output voltage with good linearity, and the switching amplifier efficiently supplies most of the output current by sensing and amplifying the output current of the former.

Assuming that the current loop $\beta(\equiv i_d/i_a)$ has a large loop gain and a wide bandwidth, the linear amplifier only delivers the switching ripple current of the switching amplifier because the switching amplifier supplies most of the output current through the relation of $i_o = i_a + i_d = (1+\beta)\cdot i_a$. In reality, however, as shown in Fig. 2(b), the output current of the switching amplifier (i_d) is slower and less than the output current (i_o) because of the finite loop gain β. Thus, the linear amplifier must provide some amount of signal current in addition to the ripple current to compensate for the distortion that results from the phase lag of the switching stage in the high-frequency region. With the magnitude of loop gain $|\beta|$, the phase of loop gain θ, and the output current i_o at a specific frequency, the required output current of the linear amplifier i_a and the phase delay of the switching stage α are given by

$$|\beta| = \frac{\sin(\theta-\alpha)}{\sin\alpha}$$
$$i_a = i_o \cdot \frac{\sin\alpha}{\sin\theta}. \quad (1)$$

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