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SPECIAL ISSUE ON THE 2007 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC)

Introduction to the Special Issue on the 2007 IEEE International Solid-State Circuits Conference	2635
..... <i>J. Sevenhans, J. T. Stonick, M. Miller, and J. E. D. Hurwitz</i>	

ANALOG CIRCUITS AND CONVERTERS

A Wide-Bandwidth 2.4 GHz ISM Band Fractional- N PLL With Adaptive Phase Noise Cancellation	2639
..... <i>A. Swaminathan, K. J. Wang, and J. Galton</i>	
A Micropower Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer	2651
..... <i>M. Puavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen</i>	
A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters	2666
..... <i>T.-W. Kwak, M.-C. Lee, and G.-H. Cho</i>	
A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC	2677
..... <i>L. Brooks and H.-S. Lee</i>	
A 10-bit 205-MS/s 1.0-mm ² 90-nm CMOS Pipeline ADC for Flat Panel Display Applications	2688
..... <i>S.-C. Lee, Y.-D. Jeon, J.-K. Kwon, and J. Kim</i>	
A 56 mW Continuous-Time Quadrature Cascaded $\Sigma\Delta$ Modulator With 77 dB DR in a Near Zero-IF 20 MHz Band	2696
..... <i>L. J. Breems, R. Ruten, R. H. M. van Veldhoven, and G. van der Weide</i>	
A Single-Inductor Switching DC-DC Converter With Five Outputs and Ordered Power-Distributive Control	2706
..... <i>H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, and G.-H. Cho</i>	

WIRELINE

40-Gb/s High-Gain Distributed Amplifiers With Cascaded Gain Stages in 0.18- μm CMOS	2715
..... <i>J.-C. Chien and L.-H. Lu</i>	
A 40-44 Gb/s 3 \times Oversampling CMOS CDR/1:16 DEMUX	2726
..... <i>N. Nedovic, N. Tzartzanis, H. Tamura, F. M. Rotella, M. Wiklund, Y. Mizutani, Y. Okaniwa, T. Kuroda, J. Ogawa, and W. W. Walker</i>	
A Fully Integrated 4 \times 10-Gb/s DWDM Optoelectronic Transceiver Implemented in a Standard 0.13 μm CMOS SOI Technology	2736
..... <i>A. Narasimha, B. Analui, Y. Liang, T. J. Sleboda, S. Abdalla, E. Balmater, S. Gloeckner, D. Guckenberger, M. Harrison, R. G. M. P. Koumans, D. Kucharski, A. Mekis, S. Mirsaidi, D. Song, and T. Pinguet</i>	

(Contents Continued on Back Cover)

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ANALOG CIRCUITS AND CONVERTERS

A Wide-Bandwidth 2.4 GHz ISM Band Fractional- N PLL With Adaptive Phase Noise Cancellation	<i>A. Swaminathan, K. J. Wang, and I. Galton</i>	2639
A Micropower Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer	<i>M. Paavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen</i>	2651
A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters	<i>T.-W. Kwak, M.-C. Lee, and G.-H. Cho</i>	2666
A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC	<i>L. Brooks and H.-S. Lee</i>	2677
A 10-bit 205-MS/s 1.0-mm ² 90-nm CMOS Pipeline ADC for Flat Panel Display Applications	<i>S.-C. Lee, Y.-D. Jeon, J.-K. Kwon, and J. Kim</i>	2688
A 56 mW Continuous-Time Quadrature Cascaded $\Sigma\Delta$ Modulator With 77 dB DR in a Near Zero-IF 20 MHz Band	<i>L. J. Breems, R. Rutten, R. H. M. van Veldhoven, and G. van der Weide</i>	2696
A Single-Inductor Switching DC-DC Converter With Five Outputs and Ordered Power-Distributive Control	<i>H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, and G.-H. Cho</i>	2706

WIRELINE

40-Gb/s High-Gain Distributed Amplifiers With Cascaded Gain Stages in 0.18- μ m CMOS	<i>J.-C. Chien and L.-H. Lu</i>	2715
A 40-44 Gb/s 3 \times Oversampling CMOS CDR/1:16 DEMUX	<i>N. Nedovic, N. Tzartzanis, H. Tamura, F. M. Rotella, M. Wiklund, Y. Mizutani, Y. Okaniwa, T. Kuroda, J. Ogawa, and W. W. Walker</i>	2726
A Fully Integrated 4 \times 10-Gb/s DWDM Optoelectronic Transceiver Implemented in a Standard 0.13 μ m CMOS SOI Technology	<i>A. Narasimha, B. Analui, Y. Liang, T. J. Sleboda, S. Abdalla, E. Balmater, S. Gloeckner, D. Guckenberger, M. Harrison, R. G. M. P. Koumans, D. Kucharski, A. Mekis, S. Mirsaidi, D. Song, and T. Pinguet</i>	2736

A 14-mW 6.25-Gb/s Transceiver in 90-nm CMOS		
..... J. Poulton, R. Palmer, A. M. Fuller, T. Greer, J. Eyles, W. J. Dally, and M. Horowitz		2745
A Self-Calibrated On-Chip Phase-Noise Measurement Circuit With -75 dBc Single-Tone Sensitivity at 100 kHz Offset ...		
..... W. Khalil, B. Bakkaloglu, and S. Kiaei		2758
<hr/>		
WIRELESS AND RF		
A Blocker Filtering Technique for SAW-Less Wireless Receivers	H. Darabi	2766
A Multimode Transmitter in 0.13 μ m CMOS Using Direct-Digital RF Modulator		
..... P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Pärssinen		2774
A Single-Chip Dual-Band CDMA2000 Transceiver in 0.13 μ m CMOS		
..... J. Zipper, C. Stöger, G. Hueber, R. Vazny, W. Schelmbauer, B. Adler, and R. Hagelauer		2785
A Fully Integrated MIMO Multiband Direct Conversion CMOS Transceiver for WLAN Applications (802.11n)		
..... A. Behzad, K. A. Carter, H.-M. Chien, S. Wu, M.-A. Pan, C. P. Lee, Q. Li, J. C. Leete, S. Au, M. S. Kappes, Z. Zhou, D. Ojo, L. Zhang, A. Zolfaghari, J. Castanada, H. Darabi, B. Yeung, A. Rofougaran, M. Rofougaran, J. Trachewsky, T. Moorti, R. Gaikwad, A. Bagchi, J. S. Hammerschmidt, J. Pattin, J. J. Rael, and B. Marholev		2795
SiP Tuner With Integrated LC Tracking Filter for Both Cable and Terrestrial TV Reception		
..... J. R. Tourret, S. Amiot, M. Bernard, M. Bouhamame, C. Caron, O. Crand, G. Denise, V. Fillâtre, T. Kervaon, M. Kristen, L. Lo Coco, F. Mercier, J. M. Paris, F. Pichon, S. Prouet, V. Rambeau, S. Robert, J. van Sinderen, and O. Susplugas		2809
A 900 MHz UHF RFID Reader Transceiver IC		
..... S. Chiu, I. Kipnis, M. Loyer, J. Rapp, D. Westberg, J. Johansson, and P. Johansson		2822
An Integrated Ultra-Wideband Timed Array Receiver in 0.13 μ m CMOS Using a Path-Sharing True Time Delay Architecture	T.-S. Chu, J. Roderick, and H. Hashemi	2834
A 2.5 nJ/bit 0.65 V Pulsed UWB Receiver in 90 nm CMOS	F. S. Lee and A. P. Chandrakasan	2851
A 0.65-to-1.4 nJ/Burst 3-to-10 GHz UWB All-Digital TX in 90 nm CMOS for IEEE 802.15.4a		
..... J. Ryckaert, G. Van der Plas, V. De Heyn, C. Desset, B. Van Poucke, and J. Craninckx		2860
A Magnetically Tuned Quadrature Oscillator	G. Cusmai, M. Repossi, G. Albasini, A. Mazzanti, and F. Svelto	2870
A 23-to-29 GHz Transconductor-Tuned VCO MMIC in 0.13 μ m CMOS	K. Kwok and J. R. Long	2878
Heterodyne Phase Locking: A Technique for High-Speed Frequency Division	B. Razavi	2887
Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS		
..... B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad		2893
<hr/>		
IMAGING, MEMS, MEDICAL, AND DISPLAYS		
A Continuous-Grain Silicon-System LCD With Optical Input Function		
..... C. J. Brown, H. Kato, K. Maeda, and B. Hadwen		2904
10-bit Driver IC Using 3-bit DAC Embedded Operational Amplifier for Spatial Optical Modulators (SOMs)		
..... J.-S. Kang, J.-H. Kim, S.-Y. Kim, J.-Y. Song, O.-K. Kwon, Y.-J. Lee, B.-H. Kim, C.-W. Park, K.-S. Kwon, W.-T. Choi, S.-K. Yun, I.-J. Yeo, K.-B. Han, T.-S. Kim, and S.-I. Park		2913
CMOS Single-Chip Electronic Compass With Microcontroller	C. Schott, R. Racz, A. Manco, and N. Simonne	2923
A 2 μ W 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials	T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly	2934
A 232-Channel Epiretinal Stimulator ASIC	M. Ortmanns, A. Rocke, M. Gehrke, and H.-J. Tiedtke	2946
A 1/2.7-in 2.96 MPixel CMOS Image Sensor With Double CDS Architecture for Full High-Definition Camcorders		
..... H. Takahashi, T. Noda, T. Matsuda, T. Watanabe, M. Shinohara, T. Endo, S. Takimoto, R. Mishima, S. Nishimura, K. Sakurai, H. Yuzurihara, and S. Inoue		2960
Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors		
..... M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing		2968
A Spatial-Temporal Multiresolution CMOS Image Sensor With Adaptive Frame Rates for Tracking the Moving Objects in Region-of-Interest and Suppressing Motion Blur	J. Choi, S.-W. Han, S.-J. Kim, S.-I. Chang, and E. Yoon	2978
<hr/>		
2007 INDEX		2990

A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters

Tae-Woo Kwak, *Student Member, IEEE*, Min-Chul Lee, *Student Member, IEEE*, and Gyu-Hyeong Cho, *Member, IEEE*

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Abstract—This paper presents a hybrid switching amplitude modulator for class-E2 EDGE polar transmitters. To achieve both high efficiency and high speed, it consists of a wideband buffered linear amplifier as a voltage source and a PWM switching amplifier with a 2 MHz switching frequency as a dependent current source. The linear amplifier with a novel class-AB topology has a high current-driving capability of approximately 300 mA with a bandwidth wider than 10 MHz. It can also operate on four quadrants with very low output impedance of about 200 m Ω at the switching frequency attenuating the output ripple voltage to less than 12 mV_{pp}. A feedforward path, a PWM control, and a third-order ripple filter are used to reduce the current burden of the linear amplifier. The output voltage of the hybrid modulator ranges from 0.4 to 3 V for a 3.5 V supply. It can drive an RF power amplifier with an equivalent impedance of 4 Ω up to a maximum output power of 2.25 W with a maximum efficiency of 88.3%. The chip has been fabricated in a 0.35 μm CMOS process and occupies an area of 4.7 mm².

Index Terms—Buffer, class AB, dc–dc converter, EDGE, low dropout (LDO), low output impedance, operational amplifier, polar transmitter, power amplifier (PA), pulsewidth modulation (PWM), switching amplifier.

I. INTRODUCTION

EVEN THOUGH amplitude variations of a phase-modulated carrier require inefficient linear RF power amplifiers, recent wireless systems tend to use amplitude modulation as well as phase modulation to achieve a high data rate. Polar transmitters as shown in Fig. 1 are known as good candidates for such high-data-rate systems because they can obtain high efficiency by using efficient switched-mode RF power amplifiers. However, when a complex signal is being split into its amplitude and phase components, the bandwidth of each component becomes wider than that of the original signal [1], [2]. This is why wideband low-dropout (LDO) linear amplifiers are still used in the amplitude path of most polar transmitters in spite of their low efficiencies. Recently, many efforts have been made to replace LDO amplifiers with switching ones to obtain better efficiency. Nevertheless, a switching amplifier has difficulty in efficiently following a high-frequency amplitude signal because a high switching frequency is required, and switching loss increases with switching frequency. Moreover, it has been implemented with many external components or expensive high-

speed processes such as GaAs or SiGe. Although a CMOS amplitude modulator based on the concept of interleaving delta modulation has been suggested in [3], it still consumes considerable power and requires many external components—especially binary-weighted inductors. However, our proposed CMOS hybrid switching amplifier achieves both high speed and high efficiency through the combination of a wideband linear amplifier with a very efficient switching amplifier.

The organization of this paper is as follows. In Section II, we review the concept of the hybrid switching amplifier and present the auxiliary circuits, such as a feedforward path and a third-order ripple filter. In Section III, we present the proposed low-output-impedance buffer amplifier. In Section IV, we discuss the experimental results. Finally, in Section V, we present our conclusions.

II. HYBRID SWITCHING AMPLIFIER

A. Concept of a Conventional Hybrid Switching Amplifier

As shown in Fig. 2(a), the hybrid switching amplifier has a master–slave structure consisting of a wideband linear amplifier as a voltage source and a switching amplifier as a current-controlled current source. The wideband linear amplifier accurately controls the output voltage with good linearity, and the switching amplifier efficiently supplies most of the output current by sensing and amplifying the output current of the former.

Assuming that the current loop β ($\equiv i_d/i_a$) has a large loop gain and a wide bandwidth, the linear amplifier only delivers the switching ripple current of the switching amplifier because the switching amplifier supplies most of the output current through the relation of $i_o = i_a + i_d = (1 + \beta) \cdot i_a$. In reality, however, as shown in Fig. 2(b), the output current of the switching amplifier (i_d) is slower and less than the output current (i_o) because of the finite loop gain β . Thus, the linear amplifier must provide some amount of signal current in addition to the ripple current to compensate for the distortion that results from the phase lag of the switching stage in the high-frequency region. With the magnitude of loop gain $|\beta|$, the phase of loop gain θ , and the output current i_o at a specific frequency, the required output current of the linear amplifier i_a and the phase delay of the switching stage α are given by

$$|\beta| = \frac{\sin(\theta - \alpha)}{\sin \alpha}$$

$$i_a = i_o \cdot \frac{\sin \alpha}{\sin \theta} \quad (1)$$

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