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WIRELINE COMMUNICATION PAPERS

IMAGERS, MEMS, MEDICAL, AND DISPLAYS PAPERS

A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters

Wing-Yee Chu, Bertan Bakkaloglu, *Senior Member, IEEE*, and Sayfe Kiaei, *Fellow, IEEE*

***Abstract*—A combined class-AB and switch-mode regulator based supply modulator with a master–slave architecture achieving wide bandwidth and low ripple is presented. Low frequency content of the envelope waveform is provided by a synchronous-rectifier based switch-mode power supply while high frequency content is provided by a rail-to-rail class-AB amplifier. A wide range, low loss output current sensing circuit is used at the class-AB amplifier output, canceling the ripple due to switch-mode power supply and extending overall modulator bandwidth. The proposed regulator is designed and fabricated on a 0.35 μm CMOS process. The combined regulator achieves a maximum efficiency of 82% and an IMD3 of 65 dBc at 10 MHz for 16 dBm output power. The regulator achieves a frequency range up to 10 MHz with less than 0.2% envelope tracking error, making this PA regulator suitable for CDMA applications.**

***Index Terms*—Envelope tracking, supply modulator, PA regulator, CDMA, power amplifier.**

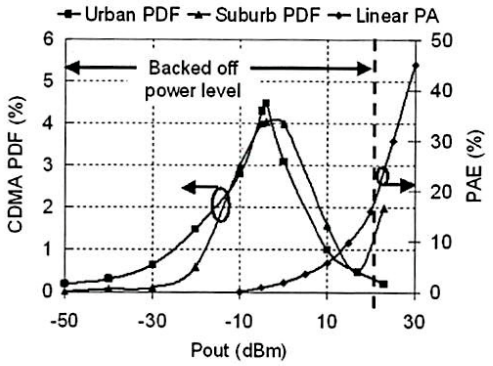

Fig. 1. Typical power density function (PDF) of CDMA handset power levels with respect to the PA efficiency [10], [11].

I. Introduction

POWER AMPLIFIERS (PAs) consume a significant portion of the total power budget of battery operated wireless transceivers; therefore, they are the key components for power reduction in mobile systems. Although efficient class D, E, F, and S amplifiers offer power saving solutions for mobile transmission, their inherent non-linear nature creates out-of-band spurious emissions. As shown in Fig. 1, the typical variable envelope linear modulation scheme utilizes a PA at a lower power level compared to its maximum operating power. The backed-off levels can be anywhere between 6 dB to 20 dB, and at these levels more and more power is wasted at the PA, reducing overall PA efficiency. It is highly desirable to track the envelope variations of a modulated waveform at the PA power supply. This variable supply operation ensures close to peak efficiency at various signal envelope levels Polar modulated transmitters try to address this efficiency loss by closely tracking the envelope of an RF band-pass signal and applying it onto the drain of a high efficiency, non-linear PA. An envelope detector extracts the envelope waveform and this is applied as input to a wideband supply regulator, as shown in Fig. 2 [1], [2]. By applying the amplitude and phase components of RF signals separately to the power supply and input of non-linear PAs, the efficiency of PAs at backed-off power levels improve significantly. A known drawback of this technique is spectral expansion of envelope and phase bandwidths after envelope extraction. An example of this spectral expansion phenomenon in CDMA signals is shown in Fig. 3. As shown in this figure, −35 dB bandwidth of a composite IS-95 CDMA waveform envelope is approximately three times wider than the same waveform's occupied RF bandwidth. The envelope waveform also has a much higher DC content due to full wave rectification during envelope extraction. System level simulations show that at least 5 MHz bandwidth from the supply modulator for IS-95 CDMA applications is needed in order to minimize its impact on output ACPR. A bandwidth target of 10 MHz is selected to ensure margin across load variations. Another drawback of polar modulation is amplitude and phase path misalignment, which results in spectral regrowth of the transmitted signal [3]. In a similar fashion, fast response wide bandwidth supply modulators with small group delay can minimize this misalignment.

Previously, switch-mode regulators and low dropout (LDO) regulators were proposed for supply modulation [4], [5]. Although switch-mode supply regulators boost efficiency of the PA, their operating bandwidth is limited by the switching frequency. Alternatively, LDO regulators provide wide bandwidth while enhancing the linearity of the PA, but they are inefficient at backed-off power levels. Recently, combined linear and switch-mode supply modulation techniques are gaining attention for RF PA supply implementations [6], [7], [1].

In this paper, a master–slave linear and switch-mode supply modulator with fast dynamic transient response is presented. By

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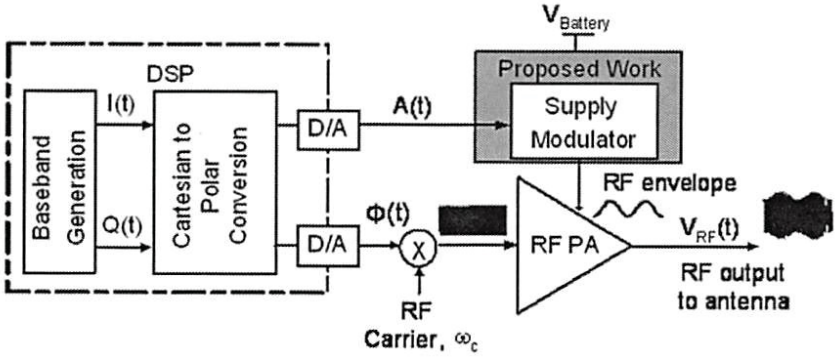

Fig. 2. Typical polar modulation based transmitter block diagram.

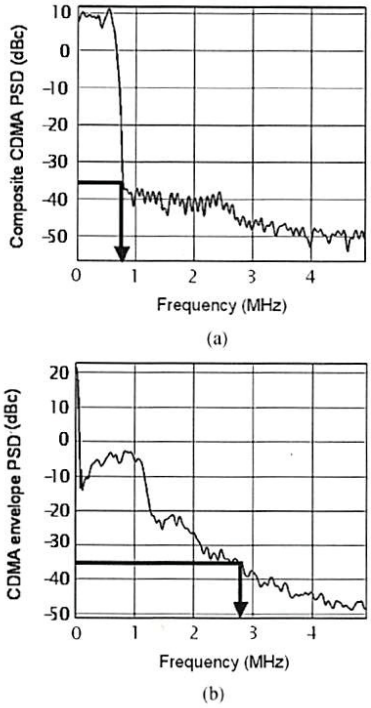

Fig. 3. Power spectral density (PSD) of (a) composite CDMA signal and (b) its extracted envelope.

using an accurate current sensing technique, efficiency and linearity of the supply modulator is further optimized. The organization of this paper is as follows: Section II describes the operation of the PA supply modulator and techniques for performance optimization. Section III details the circuit level implementations of the linear amplifier, switch-mode regulator and current sensing circuit. The measurement setup and results are presented in Section IV, followed by a conclusion in Section V.

II. Design of Master–Slave PA Regulator

A. Operation

Fig. 4 shows the block diagram of the proposed master–slave linear and switch-mode combined supply modulator loaded with a PA. A high GBW linear amplifier in voltage follower configuration ensures that output node $V_o(t)$ tracks the reference envelope voltage $A(t)$. A current sensing circuit, high gain transimpedance amplifier and switch-mode regulator forms a global feedback control loop that suppresses the current output from the linear amplifier within the switch-mode regulator bandwidth. Consequently, a large portion of the load current is provided by the switch-mode regulator. The lower efficiency linear amplifier sources small amounts of output current $I_{\rm lin}(t)$ to cancel out switch-mode regulator ripple and high frequency signal content. The transient response of currents at the output of the switch-mode regulator $I_{\rm sm}(t)$, the linear amplifier $I_{\rm lin}(t)$ and combined master–slave supply modulator $I_o(t)$ is shown in Fig. 5. Assuming an infinite GBW linear amplifier, this architecture will generate a ripple free output current $I_o(t)$ to the load. However, due to finite GBW of the linear amplifier, only the ripple energy within the linear amplifier is cancelled. This tradeoff between GBW of linear amplifier and ripple size will be discussed later.

To gain further insight on the operation of master–slave supply modulators, the current-mode frequency response of the linear amplifier, switch-mode regulator, and their combined response are analyzed. The steady state output current of switch-mode regulator $I_{\rm sm}$ can be defined by the linear regulator current $I_{\rm lin}$ as follows:

$$I_{\rm sm} = \frac{I_{\rm lin}}{n} \cdot A_{\rm tia} \cdot \frac{1}{S_r} \cdot \frac{1}{1 + s^2 \cdot L \cdot C} \cdot \frac{1}{R_L} \tag{1}$$

where n is the current sense ratio, $A_{\rm tia}$ is the transimpedance gain, S_r is the slope of the ramp in the switch-mode regulator and R_L is the equivalent PA load resistance. The sensed current is amplified by the transimpedance amplifier, comparator and the voltage divider formed by equivalent series resistance (ESR) of the loading inductor and resistive component R_L of the PA load. The second-order LC filter and the ESR set the dominant pole location of the frequency response.

From (1), we can derive the transfer function of the combined output current I_o as follows:

$$\frac{I_o}{A} = \frac{1}{R_L} \cdot \frac{1}{1 + \frac{1}{A_{\rm lin}}} \tag{2}$$

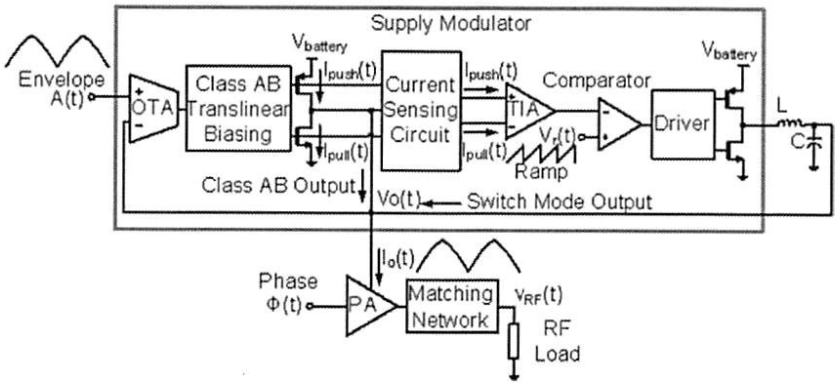

Fig. 4. The proposed master–slave linear and switch-mode PA regulator block diagram.

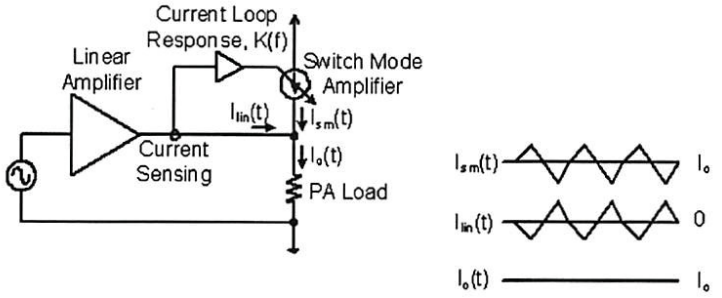

Fig. 5. Simplified block diagram of the proposed regulator showing ripple cancellation.

where A represents the input envelope signal and A_{lin} is the open loop gain of the linear amplifier. The switch-mode regulator output current I_{sm} can be shown as

$$\frac{I_{\text{sm}}}{A} = \frac{1}{1+\frac{n\cdot S_r\cdot(1+s^2\cdot L\cdot C)\cdot R_L}{A_{\text{tia}}}}\cdot\frac{1}{R_L}\cdot\frac{1}{1+\frac{1}{A_{\text{lin}}}} \tag{3}$$

and finally the linear amplifier output current I_{lin} is represented by

$$\frac{I_{\text{lin}}}{A} = \frac{n\cdot S_r\cdot(1+s^2\cdot L\cdot C)}{A_{\text{tia}}}\cdot\frac{1}{1+\frac{1}{A_{\text{lin}}}}. \tag{4}$$

As shown in (3) and (4), the output current response of the switch-mode amplifier has a two-pole transfer function forming a second-order low-pass characteristic, while the output current response of the linear amplifier has a two-zero transfer function that contains a second-order high-pass characteristic. At low frequencies, the linear amplifier current output is suppressed and the switch-mode regulator dominates the output current. Conversely, at high frequencies, the switch-mode regulator current response starts rolling off and the linear amplifier takes over the output current. The switch-mode regulator and linear amplifier current response combine and form a flat frequency response for the master–slave regulator. The frequency where switch-mode regulator current response rolls off and linear amplifier current response takes over is called transition frequency, f_T. This frequency plays an important role on efficiency optimization and will be discussed in the next section.

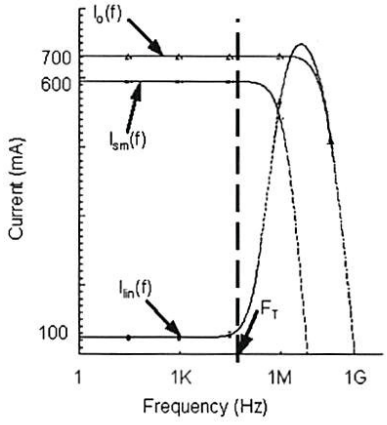

Fig. 6. Current-mode frequency response of the linear amplifier, the switch-mode regulator and the master–slave combined regulator.

Fig. 6 plots the current-mode frequency response of the linear amplifier, switch-mode regulator and master–slave regulator. As predicted in the mathematical analysis, second-order low-pass and high-pass characteristics were obtained. The resulted flat output current response is suitable for high linearity implementation. In addition, the overall bandwidth extended by the linear amplifier makes the supply modulator suitable for wide bandwidth signal transmission.

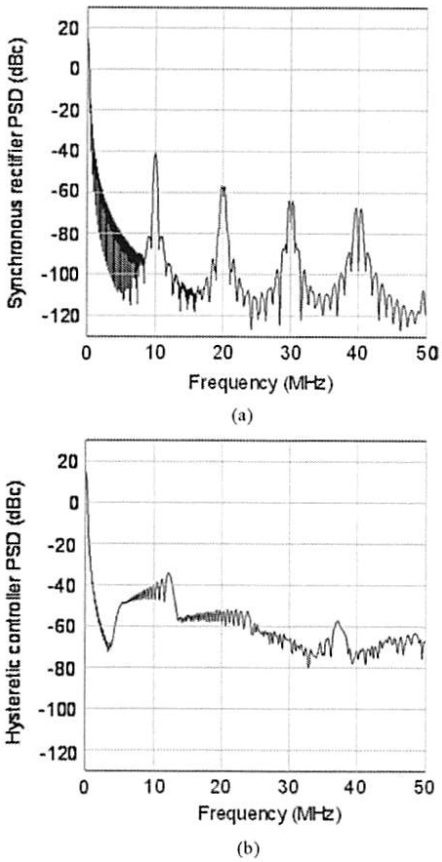

Fig. 7. Ripple energy for a 10 dBm, 100 kHz SSB suppressed carrier modulation waveform for (a) a synchronous rectifier versus (b) a hysteretic controller.

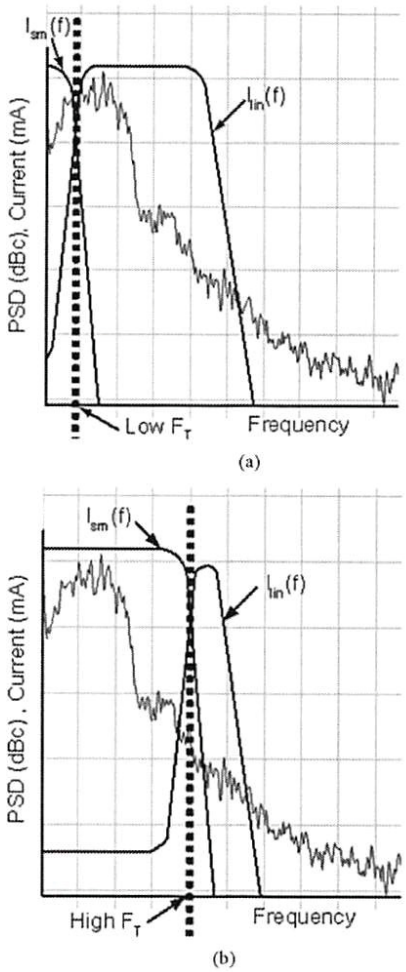

Fig. 8. Portion of CDMA spectrum amplified by linear amplifier and switch-mode regulator at (a) low f_T and (b) high f_T.

B. Performance Optimization

Master–slave regulator configuration is commonly used for audio amplifiers, and for these applications a switch-mode regulator is typically configured in hysteretic control mode. Hysteretic controllers do not need a clocked comparator; instead they use a window comparator, and frequency of operation depends on the load conditions. The loop response of hysteretic controllers is quite fast during load transients. However, this variable frequency operation generates wideband spurious emissions at the regulator output. This in turn increases the AC power from the linear amplifier since more ripple energy falls within class-AB amplifier bandwidth. The two power spectral density plots in Fig. 7 represent the ripple energy for a 10 dBm, 100 kHz single sideband (SSB) suppressed carrier modulation waveform for a synchronous rectifier versus a hysteretic controller. As shown in this figure, the integrated ripple energy within the class-AB bandwidth is much higher for a hysteretic controller. For wideband modulation schemes, this analysis shows that synchronous rectifiers are a better choice for low power, low spurious emissions design.

To optimize the efficiency of a PA supply modulator, two properties of the envelope signals should be considered: the power level probability density function (PDF) discussed in Fig. 1 and power spectral density (PSD). As shown in Fig. 3, the envelope PSD contains high DC content and most of the envelope energy is accumulated at frequencies less than 2 MHz with a small portion of the envelope energy rolling off at higher frequencies. The bandwidth specifications of the switch-mode regulator can be relaxed further reduce the switching losses and use the linear amplifier to amplify the high frequency portion of the signal. However, as the bandwidth of the high efficiency switch-mode regulator becomes too low, the low efficiency linear amplifier dominates the output current, reducing overall efficiency. Fig. 8 shows the portions of the envelope spectrum amplified by the linear amplifier and switch-mode regulator with different transition frequencies f_T. Fig. 9 shows that peak efficiency of the supply modulator with a 20 dBm, 400 kHz SSB suppressed carrier modulated input waveform is achieved at 100 kHz f_T.

As discussed earlier, output ripple is another critical specification requirement for PA supply modulator design due to stringent ACPR and spurious emission requirements. [8]. In the proposed master–slave linear and switch-mode regulator, a significant portion of current ripple from the switch-mode

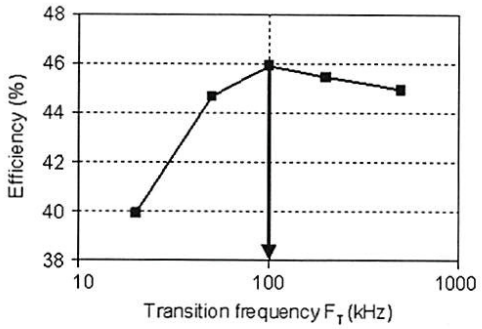

Fig. 9. Efficiency optimization of a 20 dBm, 400 kHz SSB suppressed carrier modulation envelope waveform by varying transition frequency f_T.

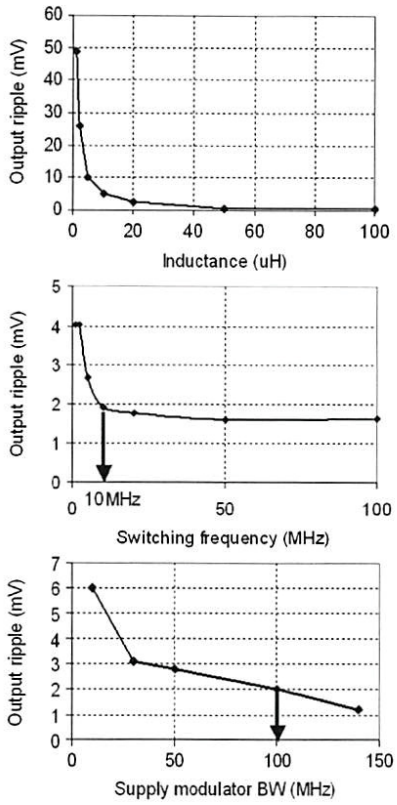

Fig. 10. Peak-to-peak output voltage ripple versus (a) load inductor, (b) switching frequency, and (c) linear amplifier GBW.

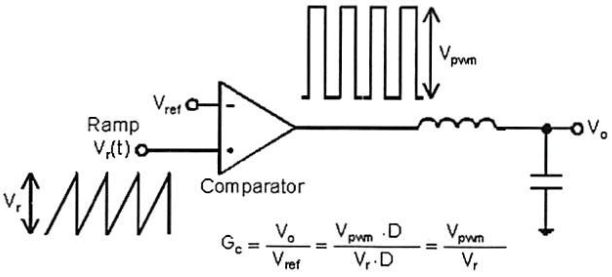

Fig. 11. Gain calculation in comparator. D is the duty cycle of $V_{\mathrm{pwm}}(t)$.

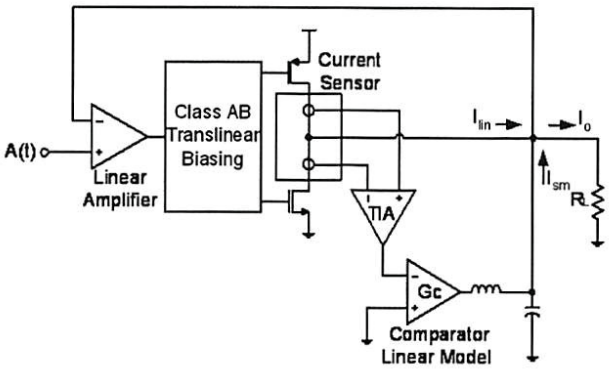

Fig. 12. Linear model for master–slave linear and switch-mode regulator.

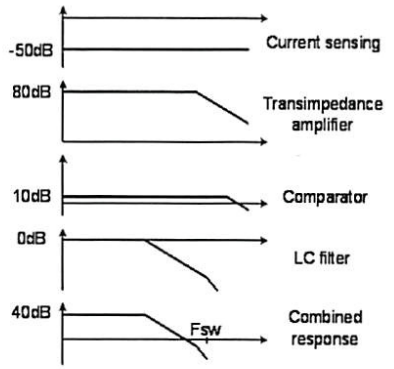

Fig. 13. Individual block and the combined frequency responses in switch-mode regulator feedback loop.

regulator is cancelled by the linear amplifier. This results in a much smaller residue voltage and current ripple at the PA drain. Output inductor and switching frequency also play an important role on output ripple value. Fig. 10(a) and (b) shows output ripple versus load inductor and switching frequency for the proposed composite regulator. Since both ripple frequency and output filter corner is determined by the transition frequency, these parameters cannot be used for ripple optimization. Therefore, the effectiveness of current ripple cancellation depends on the GBW of the linear amplifier. For the ripple specification, we have assumed a worst case PA power supply rejection (PSR) of 0 dB and used −55 dBc per 30 kHz bandwidth ACPR requirements to extract a maximum ripple specification of 2 $\mathrm{mV_{pp}}$ at the overall regulator output [8]. As shown in Fig. 10(c), as the linear regulator unity gain-bandwidth increases, the voltage ripple at the output reduces, with the expense of reduced efficiency and increased linear regulator power consumption. For a given 2 $\mathrm{mV_{pp}}$ ripple specification at a typical 16 dBm output power level, a linear regulator unity gain-bandwidth of 100 MHz is selected.

C. Switch-Mode Regulator Feedback Loop

The switch-mode regulator feedback loop includes a current sensing circuit, an error amplifier, a comparator, power stage and a low-pass filter and is designed with maximum loop gain for

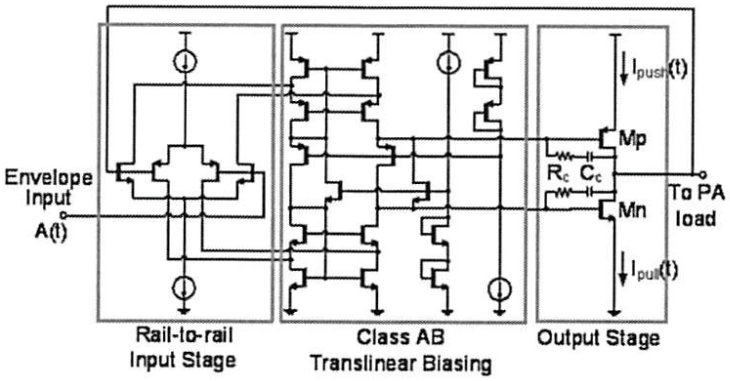

Fig. 14. Rail-to-rail input linear class-AB amplifier with common-source output stage in voltage follower configuration for ripple cancellation and master–slave supply modulator bandwidth extension.

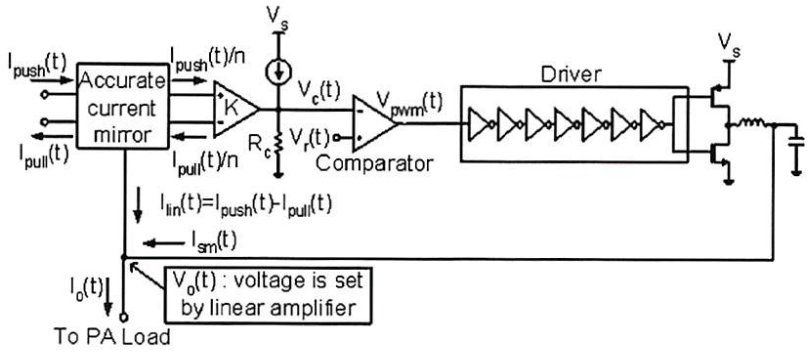

Fig. 15. Switch-mode regulator in master–slave supply modulator for high efficiency amplification.

accurate envelope tracking and highest linear amplifier output current suppression. For AC analysis, a linear model is utilized. As shown in Fig. 11, linearized gain of the comparator is defined by the ratio of its output voltage swing to the amplitude of its ramp input. $V_{\rm pwm}(t)$ is the switching version of $V_o\ (t)$ that has equal magnitude but contains stronger and more high-frequency harmonics. A linear model is obtained and Fig. 12 shows the linearized model of the system.

In the comparator design a ramp voltage swing of 0.3 V is used, yielding an equivalent gain of 10. This gain is optimized in such a way that there is minimum penalty to the loop bandwidth and phase margin. The disadvantage of using a smaller ramp voltage is the increased comparator response time. This delay results in degradation in envelope tracking accuracy of the switch mode output current and consumes more linear amplifier output current to correct the time delay errors. Furthermore, excess comparator delays degrade the phase margin of the feedback loop around the combined regulator. In this design, with the switching frequency of the supply modulator at 10 MHz and a comparator BW of 96 MHz, the comparator achieves a response time of less than 6 ns. The delay introduces a phase shift of less than 1° and requires almost no extra current from the linear amplifier.

To ensure the stability of the feedback loop in the switch-mode regulator, the bandwidth of the switch-mode regulating loop should be at least ten times less than the switching frequency. The limited operating bandwidth filters the high frequency contents of the output current ripple and prevents instability. To minimize current use from the linear amplifier, close loop gain should be high. There is also a gain-attenuation at the output of the switch-mode regulator: the ESR and resistive load form a voltage divider that degrades the loop gain. Small ESR is preferred to minimize attenuation and power losses.

Fig. 13 plots the frequency response of each block inside the switch-mode regulating loop. It shows that the total current to voltage conversion gain of current sensing and transimpedance stage is approximately 30 dB, followed by a comparator gain of 10 dB yielding an in-band gain of 40 dB. The transimpedance error amplifier and comparator are designed to have wide BW. Their poles should place beyond the GBW of the switch-mode regulator. The loading inductor sets the GBW of the close loop below switching frequency.

III. Circuit Implementation

A. Linear Amplifier

A two-stage class-AB amplifier with a common-source output stage, as shown in Fig. 14, is used for the linear amplifier. The input stage is designed rail-to-rail in order to enable arbitrary feedback configurations, including unity gain

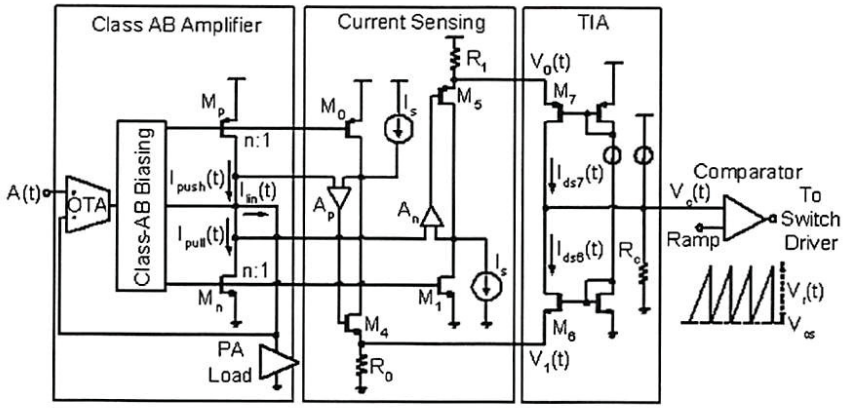

Fig. 16. Accurate current sensing circuit sensing the load current in class-AB amplifier and transimedance amplifier driving the comparator load.

follower. System level simulations show that voltage follower configuration provides the highest efficiency with minimum group delay without the need for driving the passive feedback network. System level models also show that input *gm*-control circuitry is not required for the envelope tracking application due to asymmetric nature of the envelope waveform. Because the load resistance ranges from 3.33 Ω to 8.4 Ω, the output pole is nominally set at 200 MHz for a 100 pF load capacitor to ensure stability. The rail-to-rail input stage achieves 100 MHz GBW with a load capacitance of 100 pF.

B. Switch-Mode Regulator

In the master–slave regulator configuration, the switch-mode regulator serves as the slave stage, as shown in Fig. 15, and is driven by the class-AB amplifier sensed output currents. The transresistance gain of 10 k Ω in the current-to-voltage conversion stage enhances the switch-mode loop gain, increasing the accuracy of the current-mode amplifier. The synchronous rectifier utilizes a single-stage asynchronous latched comparator with worst case settling time of 6 ns. The gate driver uses seven cascaded tapered inverter stages, which is optimized for minimum delay. The size of the external *LC* filter and power stage is designed for optimum efficiency. The GBW of the switch-mode regulator is designed to be 100 kHz, and the switching frequency is set at 10 MHz. The power stage is sized to obtain minimum gate drive and on-resistance loss. In order to ensure the stability of the linear amplifier, the load capacitance needs to be limited to 100 pF, yielding an inductor value of 20 μH for minimum output current ripple and ESR.

C. Accurate Current Sensing and Switch-Mode Regulator Input Referred Offset Reduction

In order for the current feedback mechanism to track the input envelope accurately, the input referred system offset must be minimized. Typical current sensing techniques utilize a small series resistor and measure the voltage drop across it [9]. Although this approach can sense load current accurately, it is not suitable for CDMA supply modulator applications where output currents can be up to 380 mA. In the proposed accurate current sensing circuit shown in Fig. 16, transistors $M_p - M_0 - A_p$ and $M_n - M_1 - A_n$ together form two low-loss accurate current mirrors sensing output push and pull currents $I_{\text{push}}(t)$ and $I_{\text{pull}}(t)$ from the class-AB amplifier. The load currents in the class-AB output stage formed by M_p and M_n is mirrored with 250:1 ratio to M_0, M_1 and passed through the sense resistances R_0 and R_1. To increase the operating voltage range of the current mirrors and achieve a high current sensing accuracy, a DC pedestal current source I_s is added to guarantee transistors M_4 and M_5 always stay in saturation. The BW of the current sensing circuit was limited by the GBW of the gain-enhancing amplifiers A_p and A_n at the current mirrors. With the use of moderate gain, rail-to-rail input swing, folded cascode amplifiers A_p and A_n, the current sensing circuit achieves less than 0.2% error and 10 MHz bandwidth.

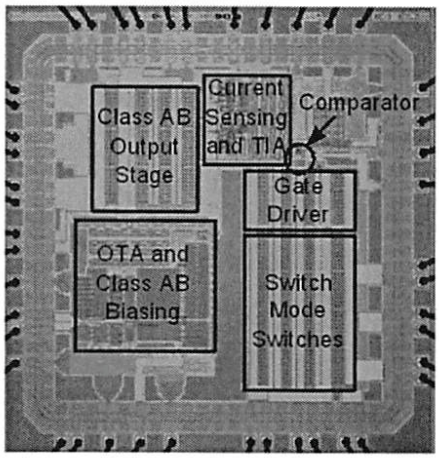

Fig. 17. Chip micrograph of master–slave linear and switch-mode supply modulator.

In the sensing circuit inside switch-mode feedback loop, matched resistor pairs R_0 and R_1 convert the sensed currents, copied accurately by the current sensing circuit, to voltages separately. The converted voltages $V_0(t)$ and $V_1(t)$ modulate gate-source voltages of M_6 and M_7 and generate a replica current across transistors M_6 and M_7 with some gain. Drain currents of M_6 and M_7 are summed and converted back to control voltage $V_c(t)$ by R_c for the PWM controller. To minimize

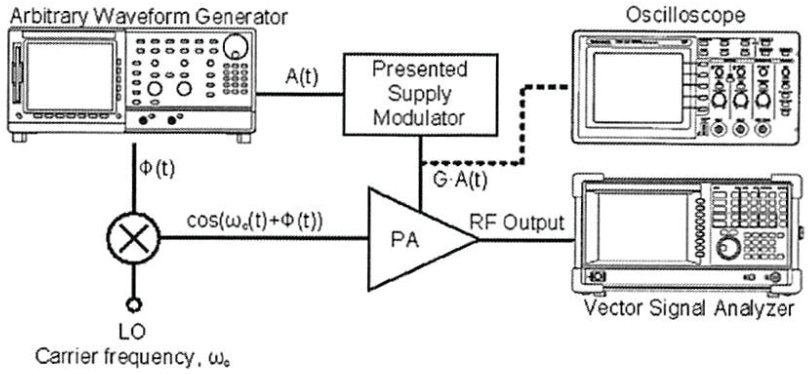

Fig. 18. Typical measurement setup for transient and spectral density analysis.

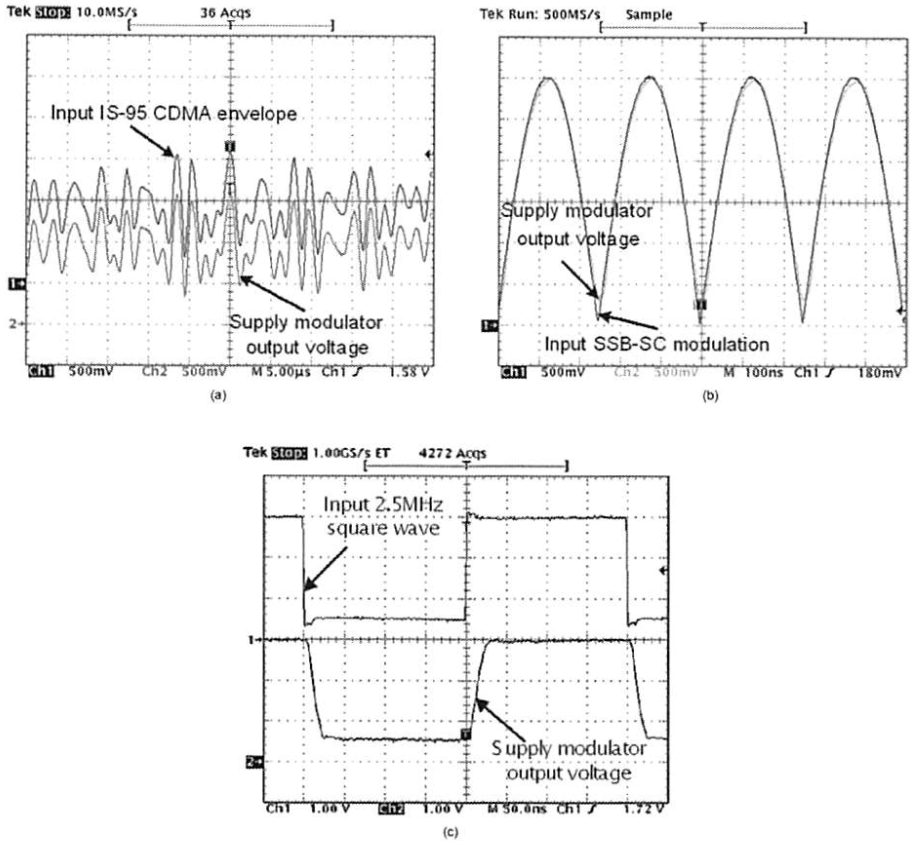

Fig. 19. Transient response of (a) CDMA envelope waveform with commercial PA load (CDMA signal baseline shifted for clarity), (b) 30 dBm, 400 kHz SSB suppressed carrier envelope waveform and (c) 2.5 V_{pp}, 2.5 MHz square waveform with 4.4 Ω resistive load.

input referred offset, the DC level of the input ramp is adjusted to cancel any system mismatches inside the current sensing circuit and transimpedance amplifier.

IV. Test Results

The master–slave, class-AB and switch-mode supply modulator is fabricated in a 0.35 μm, 4-level metal CMOS process and occupies a total core area of 4.6 mm^2 excluding the bondpads. A die micrograph of the IC with the pad ring is shown in Fig. 17. The fabricated chip was packaged in a 44-pin LCC package and mounted to a double-sided FR4 PCB for characterization.

A typical lab setup for the transient and spectral density characterization is shown in Fig. 18. Mathematical modeling software is used to generate amplitude and phase information of input waveform, and these vectors are uploaded to an arbitrary waveform generator. An external mixer module is installed for narrowband modulation of the phase to 835 MHz center frequency for the PA characterization. The supply modulator has

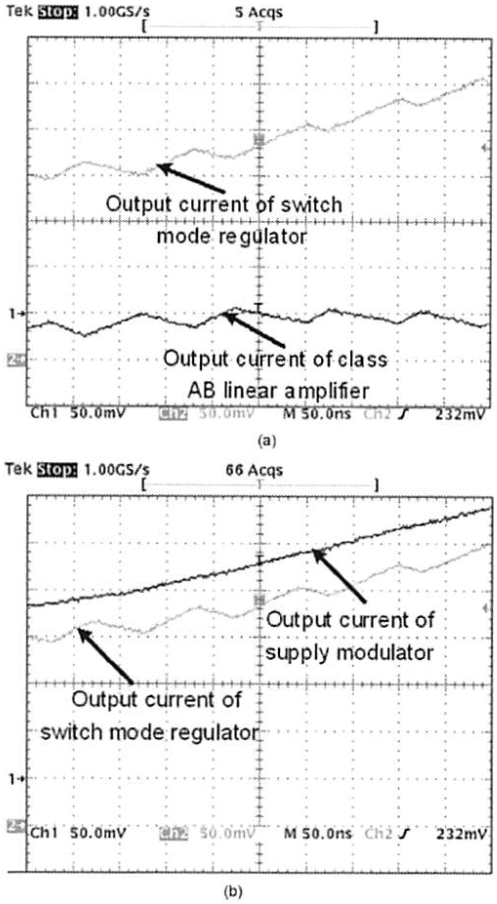

Fig. 20. Details transient response showing switching current ripple cancellation taken place at the output-summing node with 4.4 Ω resistive load.

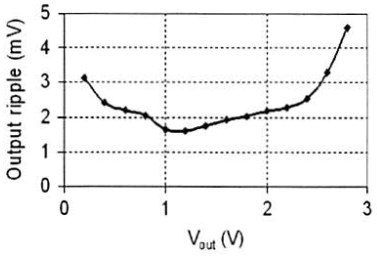

Fig. 21. Peak-to-peak output voltage ripple versus output voltage.

been tested with a 4.4 Ω resistive load with a 100 pF capacitive load and a commercial saturated PA load.

Fig. 19(a) and (b) represents a typical transient response of a CDMA envelope waveform and a 30 dBm, 400 kHz SSB suppressed carrier envelope waveform in a master–slave supply modulator with 4.4 Ω load. Fast transients at the envelope edges represent a challenge to the wideband regulator. Fig. 19(c) indicates the output transient signal settle within 60 ns with a 4.4 Ω resistive load. Fig. 20 details the current ripple cancellation take place at the output-summing node of the master–slave supply modulator. Typical output current ripple and its opposite

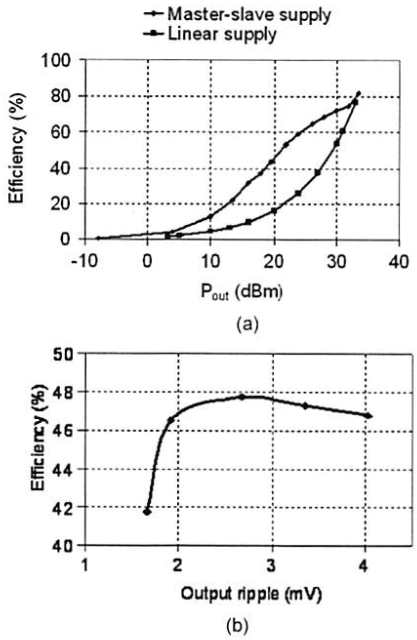

Fig. 22. (a) Efficiency comparison between linear modulator and master–slave supply modulator at different load levels. (b) Peak-to-peak ripple versus efficiency trade-off in supply modulator.

phase cancellation current from the class-AB amplifier are characterized with external 1 Ω sense resistors. As shown in the plot close to 25 mA, ripple is being cancelled by the linear regulator. Fig. 21 plots the peak-to-peak output ripple voltage at different dc levels. Fig. 22(a) compares the efficiency of the standalone class-AB supply modulator with the master–slave supply modulator at different dc levels. Maximum efficiency of the master–slave modulator is 82% and its dynamic range is 65 dBc. The efficiency of the master–slave supply modulator is three times higher than the efficiency of the linear amplifier at 16 dBm output power and indicates a significant efficiency improvement over the linear supply modulator at backed-off power levels. Based on lab characterizations shown in Fig. 22(b) modulator efficiency is found to be optimum at 2.7 mV ripple. In this characterization, the switching regulator bandwidth is modified to sweep different ripple levels. A commercial PA is used to characterize the ACPR performance of the proposed regulator system with a composite IS-95 CDMA waveform. The ACPR measurement is found in Fig. 23(a). At worst-case in-band power levels, the ACPR1 and ACPR2, 885 kHz and 1.98 MHz offset from the center frequency, are more than 46.6 and 57.4 dB, which meet the spectral mask density requirement for IS-95 CDMA transmission. A far-out plot of spectral density of the composite CDMA waveform is shown in Fig. 23(b). At 10 MHz offset from the center frequency, switching ripple adds less than −65 dB tonal content to the output spectrum. Table I summarizes the linearity and efficiency performance of the master–slave supply modulator. With 3.3 V power supply, the regulator can provide 750 mA peak current with a quiescent power consumption of 24 mA. The 2-tone SFDR at 10 MHz with commercial PA load achieves −65 dBc.

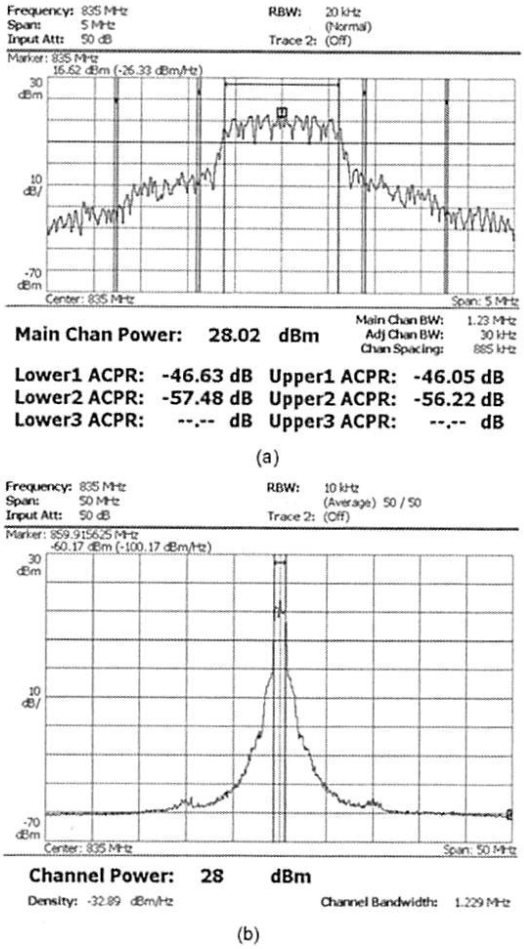

Fig. 23. (a) ACPR of IS-95 CDMA waveform with 5 MHz span (b) PSD with 50 MHz span with less than −65 dBc switching noise.

TABLE I
PERFORMANCE SUMMARY OF MASTER-SLAVE CLASS-AB AND SWITCH-MODE SUPPLY MODULATOR WITH COMMERCIAL PA LOAD

Parameters	Values
Technology	0.35um CMOS
Die area	2.1mm x 2.2mm
Supply voltage	3.3V
Output voltage range	0.3 – 3V
Output RMS current	0 – 750mA
Bandwidth	DC – 10MHz
Linear amplifier quiescent current	24mA
2-tone SFDR at 10MHz	-65dBc
Modulator peak efficiency	82%
Switching frequency	10MHz

V. CONCLUSION

A wideband master–slave class-AB and switch-mode combined supply modulator fabricated on a 0.35 μm CMOS technology is presented. A master class-AB regulator cancels distortion, supply noise and ripple associated with a switch-mode regulator, while providing high frequency signal content. A high linearity, high efficiency current sensing circuit is used to sense the class-AB amplifier output. This signal is fed-forward to a current-controlled synchronous rectifier based regulator providing the output envelope content within its bandwidth. The measurement results demonstrate that the combined regulator has less than 2 mV_{pp} ripple at its output with 65 dBc SFDR and peak efficiency of 82% achieving 10 MHz bandwidth. The master–slave supply modulator regulated PA satisfies the CDMA spectral mask requirements.

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