is either being designed or is in prototype form. Not all the test and repair equipment needed for manufacturing has be invented yet, and a continuous flow of new products is expected for the next decade. Multiple items of each category may be required for manufacturing, including optical or voltage imaging for defects.

Table 2-18 *In-Process Inspection and Repair Equipment List*

Equipment	Remarks
Electrical Parametric Test	Design based on IC test equipment
Substrate Flatness	Similar to IC equipment
Sheet Resistivity Monitor	ITO, metal line monitor, off-line and in-situ
Critical Dimension Measurement	Similar to IC equipment
Particle Monitors	Similar to IC equipment
Optical Microscope Inspection	Similar to IC equipment
Digital/Analog Optical Inspection	Based on mask/wafer inspection of ICs
Voltage Imaging or other TFT imaging	Specific design for TFT arrays
Laser Cutting	Cut shorted metal lines -combine operation with laser deposition
Laser Deposition	Metal deposition to repair opens

Table 2-19 is a list of assembly equipment with pricing for each item. The price includes semi-automatic cassette to cassette handlers, but does not include transport equipment from equipment item to equipment item. Equipment for assembly includes the actual joining and sealing of the substrates, separation and final testing, and die attach equipment for placing driver circuits on the completed panel or on flexible circuit boards which are attached to the panel.

2.5.2 MANUFACTURING COST AND YIELD

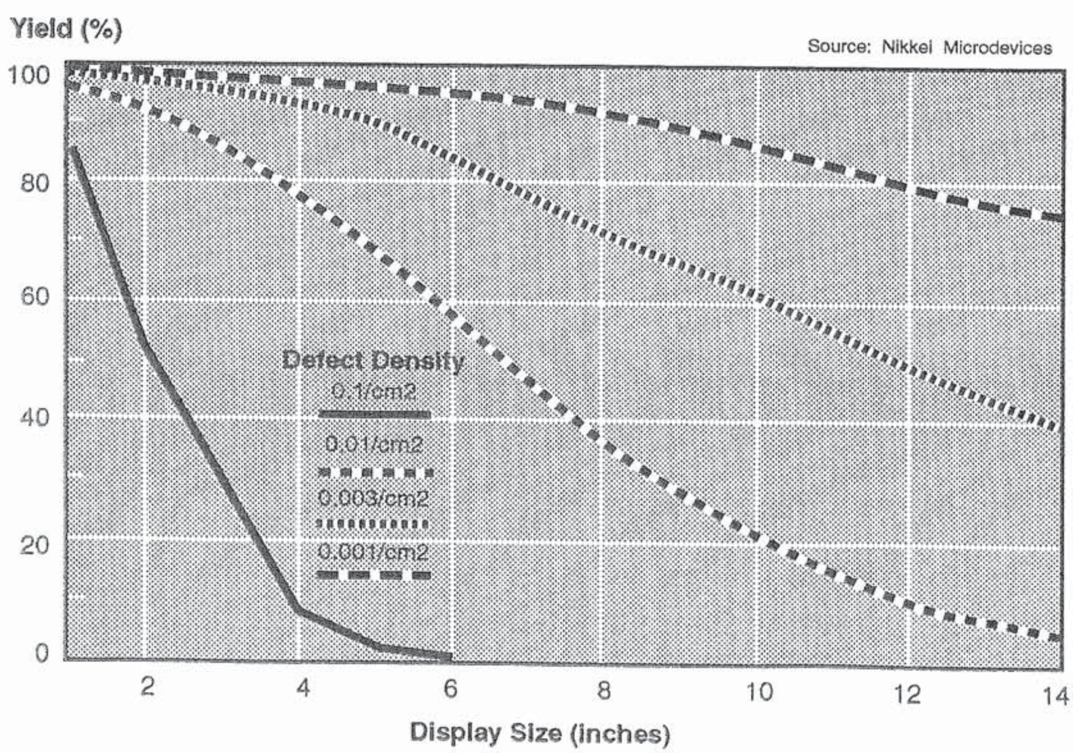
Yield vs ASP

Yield considerations will be even more important for AMLCD manufacturing than for integrated circuit production. Figure 2-21 shows a simulated yield chart based on differing levels of defect densities and display sizes. This chart, developed by the process consultant N. Yamamura and published in the August, 1990 issue of Nikkei Microdevices, shows the dramatic effect of defect density on yield and cost of color TFT displays.

Table 2-19 *Assembly and Die Attach Equipment*

Equipment	Price/Remarks
Orientation Film Printer	$180K
Orientation Film Rubbing	$80K
Substrate Cleaning	$120K
Spacer Spraying	$35
Seal Printing	$120K
Alignment/Sealing	$560K includes cassette/cassette handling
Liquid Crystal Injection	$40K
Scribe/Break	$65
Die Attach Equipment	$500K for both inner and outer lead TAB bonder

Figure 2-21 *Simulated yield curves for various defect densities in TFT display manufacturing*



On the left hand side of the illustration is the calculated yield vs display size line corresponding to 0.1 defects/cm^2. This solid line is about the defect density for small LCD displays, like those used for calculators and watches. It is impossible to build large TFT displays at all with this defect density. The next level of defects, 0.01 defects/cm^2, corresponds approximately with the current manufacturing practice in Japan. At this defect level, shown by the dashed line, a 10" display yield is about 20% at best, and corresponding display pricing is $2000 each. A much reduced defect level, 0.003 defects/cm^2, results in a higher yield curve shown by the dotted line. At this defect density, the next step for TFT manufacturing, a 60% yield can be obtained. This yield might be expected in the mid 1990s, and will result in an average selling price of $800.

A much lower defect density, 0.001 defects/cm^2, will lead to yields in the range of 80% for displays, and a corresponding selling price of $500 each or less. This level of defects, a total of 10 defects per square meter of substrate, is a lower level that is currently achieved in semiconductor manufacturing. Of course, the size of the critical dimension in TFT manufacturing is larger, but absolute defect levels are much more important for displays than for integrated circuits where many chips are manufactured at the same time on the silicon wafer.

Manufacturing Cost Model

A manufacturing cost analysis of a high definition TV factory based on AMLCD displays has been presented recently. According to this analysis, substantial differences exist between flat panel display and IC manufacturing. A written presentation by G. Resor, entitled "The Surprising Economics of Flat-Panel Production", was published in the Society for Information Display Technical Digest, p186, 1990. One of the principal differences between AMLCD and IC manufacturing is the optimum factory size, which is relatively small for displays at about 500,000 starts per year. Another difference concerns the relative importance of the cost of capital and materials. For integrated circuits, especially cost competitive products such as DRAMs, the initial investment dominates all other costs. For displays, the situation is quite different, and materials costs are dominant. Figure 2-22 shows the cost breakdown for a "minifab" with 500,000 display starts per year. The factory product in this case is a completed 14 inch high definition television. The cost analysis indicates that material costs account for more that 50% of the total, with depreciation and R&D costs at less than 10% each. The factory price of $862 per completed TV applies to the fifth year after the start of the project, and the factory is still ramping up production. After ten years of operation, production costs have declined to levels competitive with CRT-base TV sets, but materials costs continue to dominate.

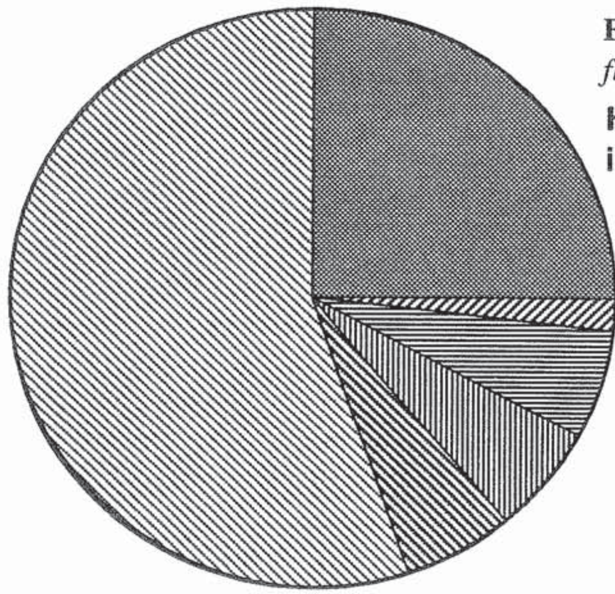


Figure 2-22 *Cost components of flat panel display production.*

Manufacturing Yield Model

A comparison of TFT-LCD manufacturing to DRAM manufacturing reveals significant differences. (See R. R. Troutman, "Forecasting Array Yields for Large-Area TFT-LCDs", Society for Information Display Technical Digest, 1990, p197) Partially good displays are not acceptable, and the probability of a fault must be small over a large area. A Poisson distribution is used to analyze and predict the yield in this situation.

The most common single cell fault is a pinhole short in a storage capacitor because of the large area of the capacitor. The resulting high leakage path produces a fixed ON or OFF condition, depending on voltage and polarizer settings. Another single cell fault is a source to drain short in the data metallization, which prevents charge transfer. A Poisson distribution of faults is constructed, and it is assumed that a few single cell faults are tolerable, as long as they are not clustered. If 10 single cell faults are allowed, then the yield is 100% at 10 faults, about 50% at 12 faults, and 20% at 15 faults. However, to ensure 99% yield at 10 allowable faults, the average number of faults has to be fewer than 5 per array.

Faults other than single cell faults are intolerable, and must be repaired. If a gate or data line is open, it is easily detected by an electrical continuity check. Repair consists of laser welding a spare line driver to the initially undriven end of the line. An interlevel short is repaired by laser cutting either the gate line or the data line and then treating the cut line as an open line. Two types of repairability are described.

Type 1 repairability is the case where gate line repairs are made only for open gate lines. In displays using the inverted staggered TFT structure, the gate is buried under several thin film layers, and laser scribing these lines might cause a yield loss by itself. Data lines are more accessible, and data line repair options cover both open lines and interlevel shorts.

Type 2 repairability assumes a high yielding technique for scribing gate lines in the array. Type 2 repairability is significantly better than Type 1 only when there are many spare gate lines available to repair interlevel shorts.

Total array yield is the product of single cell fault yield and repairable fault yield. $Y_{tot}=Y_{sc}Y_{rf}$. If the single cell fault yield can be raised to 99%, then the overall yield is determined by the repairable fault yield. Table 2-20 shows the relation between yield, defect size, and defect density without repairability. The calculation is performed for a 640x480x3 array, and assumes an average defect size of 1μm.

Table 2-20 *TFT Array Yield Summary (No Repair)*

Yield	Faults/Display	Faults/cm^2
10%	2.3	0.24
50%	0.68	0.072
90%	0.10	0.01

Consider a 1Mbit DRAM line operating at 50% yield. For a chip area of 0.5cm^2, the allowable fault density is 1.5/cm^2. Compare this to the value of 0.072 from the table, and one sees that without repair, the fault densities for a TFT array must be 21 times lower than for current DRAM manufacturing.

Repairability of the data lines and gate lines can significantly improve the yields. By providing 5-10 extra lines for repair, the major challenge to achieving high yields is interlevel (crossover) shorts. This fault type must then be maintained below 1 fault/cm^2.

AMLCD Factory

The NEC Kagoshima plant in Kyushu is manufacturing 10" flat panel TFT displays, and has achieved 50% manufacturing yields, according to an article in the August 1991 issue of Nikkei Microdevices. The yield might go as high as 70% in certain instances. The plant is inputting 5000-7500 substrates per month, which, on the 300x350mm substrate, comes to a potential 10,000-15,000 10" displays per month. Factoring in the yield, output is 6000-9000 displays per month.

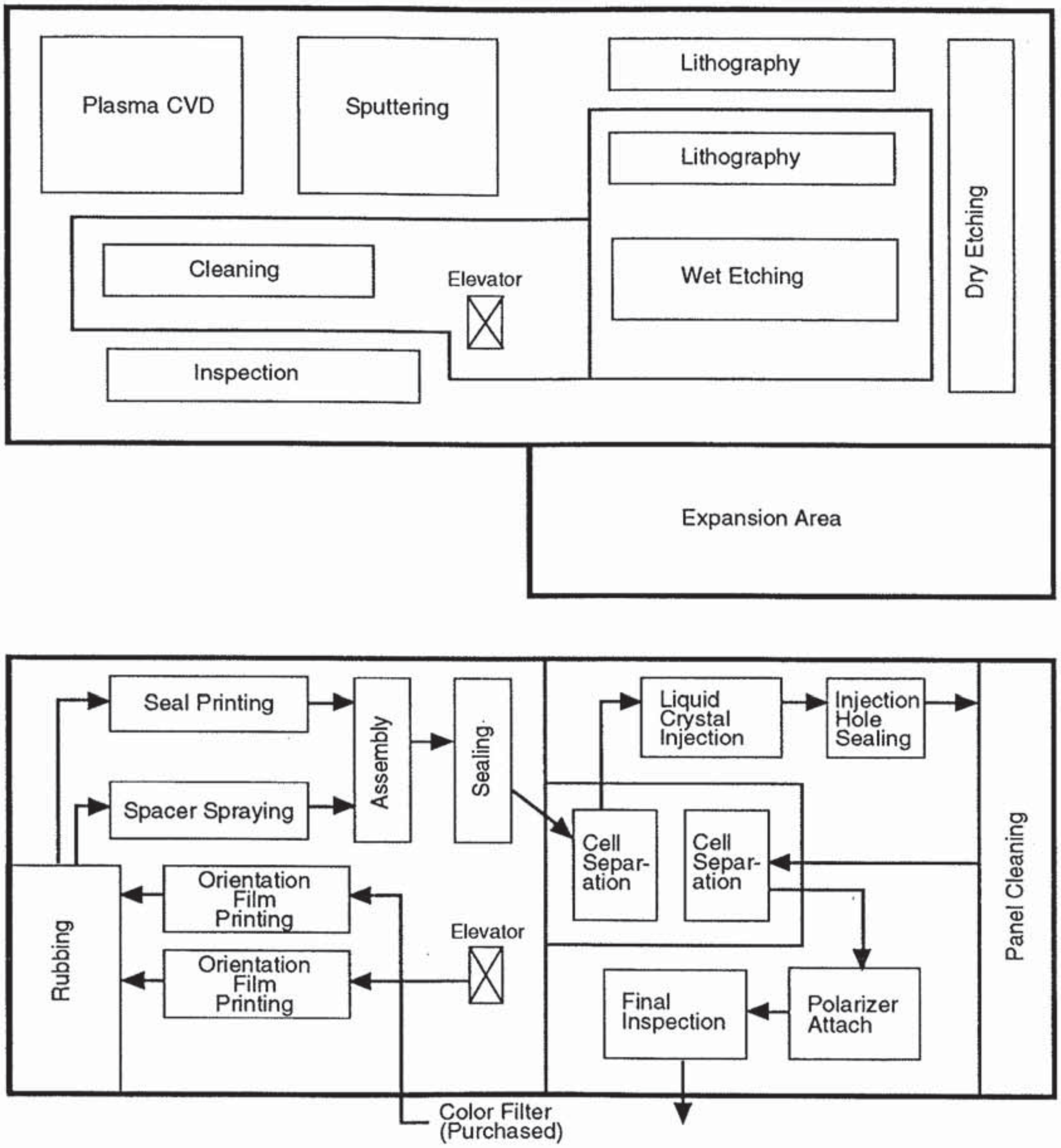
The manufacturing equipment is interconnected only where this is easy to do. Substrates are transported around the factory by automatic ground vehicles. These vehicles, which are provided with HEPA filters, are used to transport the heavy 20-substrate carriers, and to avoid particulate contamination which would occur if an operator performed the transport. Operators are used to load carriers onto the equipment, which may be an in-line series of individual processes. Equipment such as for photolithography is not fully interconnected. Computers are used to control the operation and collect information regarding machine performance.

NEC has made a high yield process using their LSI experience, and finds the process quite similar to LSI. They don't understand the cause of the yield problems in TFT fabrication reported at other companies. In NEC's opinion, the cell assembly process is a much stricter and more difficult to control process. The TFT manufacturing equipment is very like the LSI processing equipment already in use at most companies who are making TFT's, and the equipment is made by large, reliable companies. In contrast, the equipment for cell assembly is made by small and medium sized companies, and may not be available.

Figure 2-23 shows the floor plan of the factory. The upper floor contains the TFT panel fabrication area. This area is composed of lithography, cleaning, sputtering, CVD and so forth. An elevator connects this floor to the assembly area below. The floor space for the clean room is 40mx90m, and the total area is 4000 m^2 per floor. 20% of the clean room is class 100, 20% is class 1000, with the rest class 10,000. For the lithography area, class 10 is used. In the cell assembly area, the equipment and processes that generate particles, such as the rubbing equipment, are enclosed.

Right now, completed TFT panels are sent downstairs, and purchased color filter panels are started into the cell assembly process. Module assembly, with back-light occupies 2000 m^2 in another building.

Figure 2-23 *NEC two story AMLCD fabrication facility layout*



The factory is operated with 250 people on three shifts. In addition to the operators, there are 100 additional staff, and of these, 70 are technicians. 25-26 are LCD specialists, and the others are from the semiconductor process area. New technology transfer takes 3-6 months.

The TFT area has room for expansion to 10,000 substrates per month. It has been converted for 10 inch panel manufacturing. New equipment was installed and pilot manufacturing was initiated. The biggest problem was with the lithography and plasma CVD equipment. Then, Nikon stepper equipment was adopted. Each panel requires 4 exposures. Stitching accuracy is 0.2µm. Defect inspection equipment has not been chosen yet. The operation rate of the equipment has reached LSI levels. 4 stepper lines are in operation.

Anelva supplied the plasma CVD equipment for 3 lines. Due to particle buildup, thorough periodic maintenance is required. Uptime of 50% is achieved. There are 3 sputtering lines and 5 dry etching lines, also from Anelva. Resist coating lines come from Dainippon Screen. Particle inspection equipment is from Hitachi Engineering.

The 4096 color display produced at this factory has a diagonal measurement of 9.8", with 640xRGBx400 lines. Each color pixel measures $0.11 \times 0.33 mm^2$. Contrast is 80:1. A 20:1 contrast ratio or greater is maintained for a viewing angle of ±20° vertical, ±35° horizontal. Response speed is 20ms. Brightness is $80 cd/m^2$. Backlight power consumption is 12 W. TFT design employs a bottom gate construction, with a 2-layer, ITO/Cr construction. Gate insulator is SiO_2 plus Si_3N_4 deposited by plasma CVD. Gate line and data line metal is chromium, and transparent electrode is ITO. The gate electrode, channel, dielectrics and so forth are dry etched. Defective pixels number 10 or less in completed displays. Defective blue pixels are most easily detected, and two defective blue pixels can reject the entire display. As the level of cleanliness of the clean room improves, the defect level is expected to decrease.

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Materials for Flat Panel Displays

The particulars of materials for flat panel displays are presented in this part of the book, emphasizing the unique requirements for active matrix displays. In many cases, the ultimate combination of materials performance, quality and price has not yet been achieved. Particularly for color filters, significant cost reduction is essential for high volume manufacturing. For other materials, cost effectiveness is determined primarily by beneficial effects on transistor manufacturing yield.

Glass Substrates

3.1

Glass substrates of various types are used for liquid crystal displays. Substrate types were discussed in Part 2, with emphasis on fusion glass as an active matrix substrate. This section describes float glass manufacturing and ITO deposition.

Advantages of float glass material were pointed out in a recent article by Pilkington Micronics [1]. Flat glass was made by drawing processes until the advent of the float process, in which molten glass is allowed to settle onto a bath of molten tin. The glass achieves a uniform thickness with smooth surfaces on both sides. Stringent glass specifications are required for LCD applications in spite of the fact that this constitutes less than 1% of the world-wide flat glass market.

Some difficulty in obtaining the tolerances on glass properties, especially surface smoothness, arose from processing float glass for LCDs in the same furnaces used for architectural and other purposes. These furnaces might have a production capacity of 5000 tons per week, enough to satisfy the world market for LCD applications in a few days. By moving the float glass manufacturing for LCDs to a small dedicated float line, materials specifications were improved.

Float lines can produce 3 meter wide continuous ribbons with thickness variations of ±0.1μm, negligible warp, and microcorrugation controlled to averages of less than 0.1μm. On-line CVD processes are also used by this glass manufacturer to provide SiO_2 coated surfaces. Characterization of microroughness will allow classification of substrates, and reduced polishing of selected classes of glass can be achieved for STN applications. Eventually, float glass suppliers hope to eliminate the polishing process completely.

Processing the base glass substrate into a form useful to the display manufacturer is a multi-step process, with several Japanese firms offering services at each step. Table 3-1 shows the types of operations for LCD glass and suppliers at each step. Processes for SiO_2 and ITO coating are indicated. Various glass fabricators supply material to several firms for cutting and polishing. SiO_2 coating may be done be another firm, and ITO by a fourth.

Table 3-1 *LCD Glass Supplier Matrix in Japan*

Bare Glass	Cutting/Polishing	SiO_2 Coating	ITO Coating
Asahi Glass	Kuramoto	Matsuzaki (dipping)	Matsuzaki (sputter & evap.)
NSG	Fujimi	Tokyo Ohka (dipping)	Asahi Glass (sputter & evap.)
Central Glass	Mitsuru	Kuramoto	Sanyo Shinku* (sputter)
N.E.G.	N.E.G. (BLC & OAZ types)	Asahi	NSG
			CVD Central
			Seiko Epson
			Sharp
			Optrex
			Sputter
Corning			

* 100% Sharp subsidiary

3.2 ITO Sputtering

ITO sputtering is a crucial and ubiquitous part of the flat panel display industry. The material is deposited from a sintered powder source to a thickness of 1500-3500Å. Important deposited film properties are transparency, resistivity, and ease of patterning. Transmittance of 90% and resistivity of 1-3μohm-cm are normal values for these properties. These are a sensitive function of the oxygen content of the film, and oxygen is often added in the gas stream during sputtering, to make up for any loss of oxygen during transport from the ITO target to the glass substrate. Deposition temperature is a critical parameter of the process.

The higher the deposition temperature, the lower the resistivity of the film. Previously, a glass substrate temperature of 300°C was common for ITO deposition, but 200°C is necessary for color LCD displays, where the polymer color filters cannot withstand the higher temperature. Lower temperature deposition has been made possible by the new, higher density targets, which can provide uniform deposition at higher magnetic fields than the previous model, which allows for lower deposition temperatures. Table 3-2 shows film properties of deposited films. Ulvac has described a process for low temperature sputter deposition which provides resistivities as low as 5 Ω/square.

Table 3-2 *ITO Film Properties*

Deposition Conditions	Resistivity/Resistance	Application
350°C, 1000Å, e-beam or sputtering	$1.5x10^{-4}$ ohm/cm	B/W STN ~20 ohm/ square
200°C, 1000Å, e-beam sputter	$2x10^{-4}$ ohm/cm	Color Filter (requires or 2000Å for 10 ohm/ square)
Ulvac - new system 200°C sputter	$1.2x^{-4}$ ohm/cm	As low as 5 ohm/square is possible at low temp-erature for color filter

ITO targets are usually prepared in the form of rectangles about 15"x5" in size, about 6 mm thick. The material is usually cold-pressed, then sintered after isostatic pressing. Usual composition of the target is 10 wgt% SnO_2. After machining to the correct final size and shape, the ITO material is bonded to a backing plate using some form of indium or indium alloy bonding preform. Table 3-3 shows the currently available target densities available from suppliers. The higher density material is more difficult to prepare, but provides longer target life and fewer deposited InO black particles.

Table 3-3 *Characteristics of ITO Targets*

Density	InO black particles	Target Life (using high density life as ~100%)
Low (70%)	most	70%
Medium (80%)	some	80%
High (95%)	fewest	~100%

Sputtering processes consist of bombarding a material such as ITO with energetic argon ions. These ions dislodge atoms from the target, and these atoms travel to the substrate under the influence of electric and magnetic fields. If the composition of the target is non-uniform, less desirable results can occur. These include non-uniform sputtering across the target, which shortens its useful life. In addition, non-uniform density or composition can lead to absorbing particle formation.

The rectangular target is used in large batch or in-line sputtering equipment made by a variety of suppliers in Japan, including Ulvac, the largest commercial supplier, Anelva, Asahi Glass (makes equipment for their own use), and Shinku Kikai. For very large systems, the targets can be used two at a time, forming a one meter long sputtering source. Glass panels have a wide range of sizes, both because many products may be prepared in a single factory, and also because no standard sizes have been developed by the manufacturers.

Erosion of the target by the sputtering process is not uniform, and an elliptical cavity is etched out more or less in the center of the rectangle. Because a lot of ITO is left in an unusable form at the end of life of the target, and because the material is somewhat expensive, there is some interest in reclaiming the targets.

Film properties may be enhanced by annealing in air after deposition. Subsequent patterning and etching forms the transparent electrodes whose function was discussed in the previous section.

ITO sputtering is mostly done by glass coaters, primarily Matsuzaki Shinku and Asahi Glass. Glass can be supplied in coated form, except for the panels used for the active matrix TFT backplane. These are ITO coated after transistor fabrication, and this will be done internally at the display manufacturer.

Requirements for glass type, ITO thickness and other parameters vary according to the type of display being produced. Table 3-4 is a summary of the types of displays, ITO resistivity, deposition methods, and type of substrate.

3.2.1 ITO POWDER AND THIN FILM PROPERTIES

ITO targets depend on powder formulations of consistent particle size and shape, as well as adequate purity. Powder sources are Nippon Mining and Mitsui Metal Mining, with some material produced by Dowa Mining and Osaka Asahi Metals, and perhaps Sumitomo Metal Mining for internal use. Nippon Mining and

Table 3-4 *Glass Substrates for Liquid Crystal Displays*

Application	Resistivity (ohm-cm)	ITO Deposition Method	Substrate Type
TN (twisted nematic)	100-200	Electron Beam (200°C)	Soda-lime, SiO_2 coated
STN (supertwist)	15-100	Electron Beam (300°C)	Soda-lime, SiO_2 coated
STN (newer type)	10	Sputter (300°C)	Soda-lime, SiO_2 coated
Active Matrix	10	Sputter (300°C)	Low-expansion
Color filter	10	Sputter (<200°C)	Low-expansion

MitsuiMining may sell a portion of their powder production for outside use, and Tosoh is currently buying powder from one of them. But each of these is concentrating on the target market.

Typical properties of ITO target material are shown in Table 3-5.

Matsuzaki Shinku is the primary glass coater in Japan, and uses equipment made by Shinku Kikai. Asahi Glass makes their own equipment. Neither Shinku Kikai nor Asahi attempts to make the target material. This is in contrast to the older technology of sputtering ITO from indium-tin metal alloy targets, using an oxygen ambient as the source of oxygen in the film. In that case, the user could make his own target in a crucible by melting the proper amounts of metal. The other supplier of equipment of note is Ulvac, with a captive target supplier, VMC. VMC is the largest supplier of targets for the semiconductor industry in Japan, but is just beginning ITO target development.

Other Sputtering Materials 3.3

Metals used for TFT fabrication are deposited by sputtering, using similar or identical equipment as for ITO. Chromium is used for black matrix formation on the color filter portion of the display in most current processes. For TFT

Table 3-5 *Specifications for High Density ITO Target*

Property	Value
Composition	10 Wgt% SnO_2
Actual Density	6.07 gm/cm^3
Percent Theoretical Density	95%
Bulk Resistivity	0.22 mohm-cm
Thermal Conductivity	19.55 mcal/cm-sec°C
Tensile Strength	12.8 kg/mm^2
Bonding Material	In, In/Sn, In/Bi
Bond Void Ratio	<2.0%
Deposited Film Properties	
Thickness	1500-3000Å
Resistivity	<20 ohm/square
Optical Transmission	>85%

manufacturing, the materials choices are aluminum, tantalum, molybdenum, tungsten or other refractory metals for the gate lines. Source and drain metallization is primarily aluminum, with underlayers of molybdenum or other refractory for diffusion barriers. The metallurgy of thin film transistors was described in Part 2. Other than the form factor of the sputtering target, requirements for these metals appear to be identical to those for semiconductor applications. Also mentioned in Part 2 is research to develop sputter-deposition of silicon for the thin film transistor material itself.

3.4 Color Filters

Color filter applications began with manufacture of pocket sized TV which appeared on the market in the mid-1980's. The filter was made by the dye method, and its spectral properties equalled those of the CRT [2]. This method and its companion, pigment dispersion, were scaled to meet the size requirements of notebook computers. Required properties of color filter material include those shown in Table 3-6. Color filter materials such as dyes and pigments are supplied by companies such as Dainippon Paint, Dainippon Ink and so forth. Specialized formulations of polyimide with dissolved colorants are available from Toray and Brewer Science.

Table 3-6 *Properties of Color Filters*

Property	Comment
Spectral property	Colors of red, blue and green filters should be close to CIE chromaticity of CRT
Contrast ratio	Loss of light should be minimal
Uniformity	Spectral properties should be uniform across the surface of the array
Flatness	No foreign objects or projections. (most severe restriction on STN filters, ±0.1μm)
Defects	No foreign object, pin-hole, crack or dirt
Dimensional accuracy	Sufficient to align substrates easily
Thermal stability	Resistant to cell sealing and polarizer application process (250°C, 1hr target)
Chemical resistance	No discoloration, swelling, separation or creasing during cleaning or ITO etching processes.
Reliability	Temperature extremes and thermal shock (80°C to -30°C), and temperature/humidity resis tance (40°C + 95% RH)
Light stability	Resistant to bleaching in ambient light

Test conditions for color filters are summarized in Table 3-7.

3.4.1 DYE METHOD

Presently the dyeing method is the most widely used technique. Its materials and processes are both well established, with reproducible spectral properties. However, the use of dyes and water soluble polymers as binders pose some problems, resulting in poor resistance to heat, light, and chemicals. The way around this results in increased process complexity. Patterning and dyeing of each color plus other steps such as substrate cleaning and drying result in a process with a total of 40-50 steps of various types. For example, the water soluble polymer such as gelatin is made photosensitive, exposed with UV light, and then the pattern is developed. This sequence is accomplished using equipment similar to the photolithography equipment in the semiconductor industry. Next, the relief pattern is dyed by acid or reactive dyes. Because the optical density of the dye is influenced by the degree of polymerization of the resin, and because the film thickness varies depending on the dyeing process, control is necessary for each

Table 3-7 *Test Conditions for Color Filters*

Test	Equipment	Treatment Condition	
Thermal stability	Oven	180-200°C, 1hr	
Thermal stability (long term)		80°C, 500hr	
Thermal Shock	Environmental Testing Machine	-30°C, 50hr 40°C, 95%RH, 420hr. -30-80°C, .5hr 20 cycles	
Light stability	Xe-Fademeter	200-500 hr	
Chemical resistance		Dipping 10-30min	IPA
			Xylene
			Butyl Acetate
			NMP
			Butyl Lactate
			NaOH (5%)
			H_2SO_4 (5%)
		60°C, 30min	H_2O
		Supersonic Wave 5min	IPA
			H_2O
		Vapor 5min	IPA
			Fluorocarbon

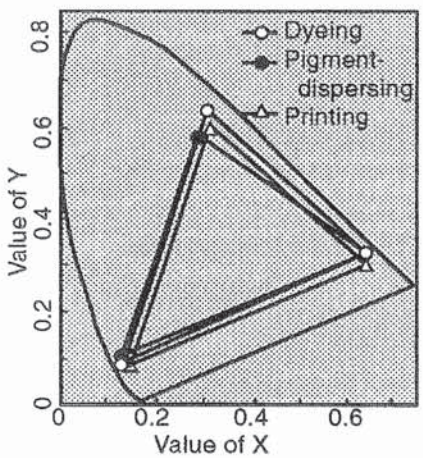
dye lot, its stability over time, and its optical density. Some investigation is being made to replace the water soluble resin with acrylic resin. In order to prevent the mixing of colors, it is possible to use an intermediate hardening step after each filter is formed, and also an intermediate transparent passivation layer is sometimes deposited separately over each color element.

Toppan is investigating offset printing as a low cost replacement method of production color filters arrays, and has presented comparison of properties of filters produced by different methods. Figure 3-1 shows the CIE chromaticity diagram for color filter arrays made by dyeing, pigment dispersion, and printing. The chromaticity coordinates are close for each of the methods, and indicate that good color balance can be achieved with these methods.

Transmittance of each filter element as well as resistance to fading is shown in

Figure 3-2, comparing dyed and printed filter elements. Printed filters show increased resistance to fading.

Figure 3-1 (Below Left) *CIE Chromaticity Diagram for color filters made by dyeing, pigment dispersion, and printing*



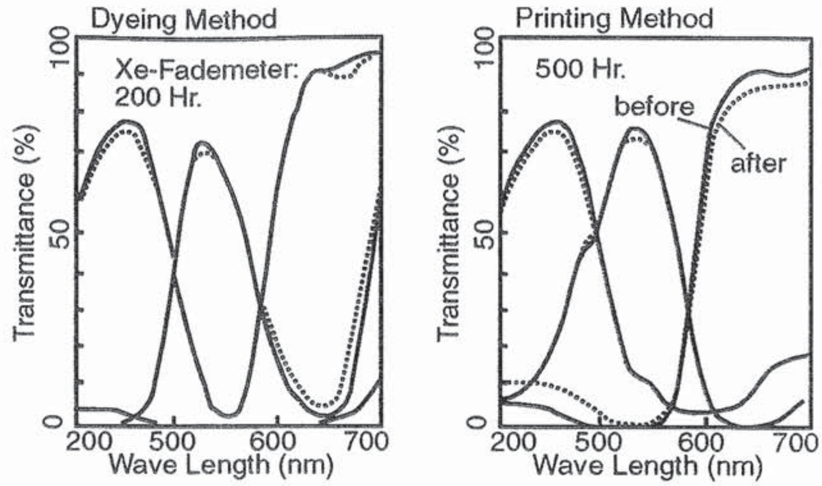


Figure 3-2 (Above center and right) *Resistance to fading of dyed and printed color filters*

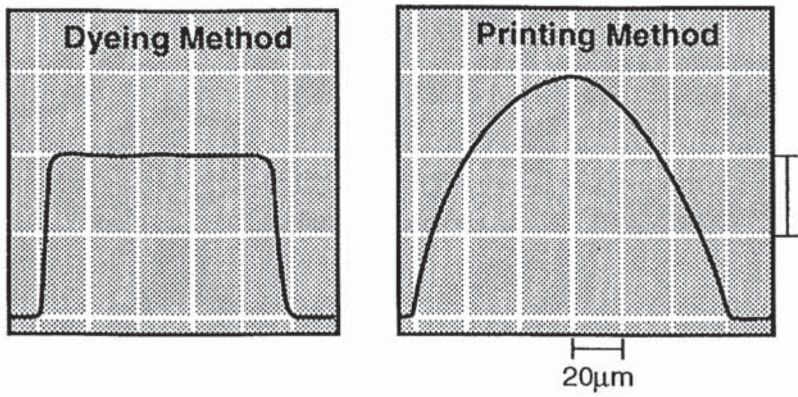
Certain problems have to be solved in order to make printing the practical production process for color filters. These include the registration of the filter array in the direction in which the print head rolls. Registration along the axis of the ink roller is easy to do. The surface tension of the ink causes it to tend to form a spherical shape when printing the 100x300μm rectangles. Figure 3-3 compares the cross-section of a spin-coated filter element with a printed one. Some of the non-uniformity which results from this droplet shape can be accommodated by the black matrix around each pixel.

In the end, even relatively high volume production will be accompanied by retouching of panels. Automation of the inspection and retouching process will be of paramount importance to improve manufacturing yield.

3.4.2 PIGMENT DISPERSION

There are various methods for dispersing a colorant in resin, and one method uses PVA steel stilbazolium negative type photosensitive resin [3]. It is a clear, water

Figure 3-3 *Comparison of spin-coated and printed filter element*



soluble resin. Under UV exposure, the double bond of the steel stilbazolium base forms a cyclobutane ring which cures by crosslinking. High sensitivity is retained after dispersion of the colorant. Pigment is used as the colorant, but generally available pigments are in large, coagulated particle form, and transparency is inadequate in this form. Therefore, the coagulated resin is refined and a dispersing agent is added to prevent coagulation. The viscosity is then adjusted and any large particles are removed by filtration. This mixture is added to the steel stilbazonium photosensitive resin. Viscosity adjustment and filtration are then performed on this final mixture.

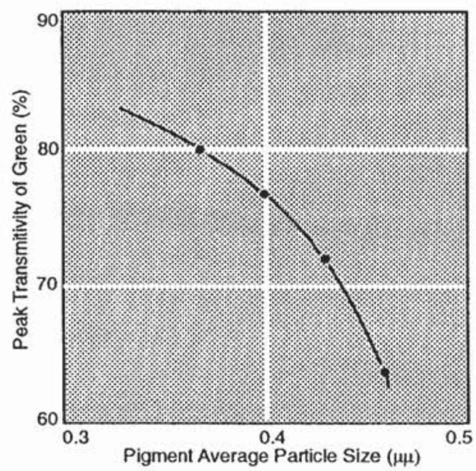
Pigment particle size averages 0.04μm, with a maximum of 0.2μm. Non-ionic dispersing agents are employed. Figure 3-4 shows the transmittance of green pigment material as a function of pigment particle size. The small average particle size of 0.04μm assures high transmittance.

The repetitive process for color filter formation using photolithography is employed, and each color element is resistant to subsequent processing. For this reason, a neutral passivation layer is not required between each color. After the color filter array is formed, a transparent overcoat is applied, followed by ITO deposition. Good stability of color arrays has been achieved.

Other types of resin materials can be used for pigment dispersion color array formation. These include an acrylic photosensitive resin, developed with alkali developer, and thermally polymerized. The polymerization reaction is suppressed when carried out in the presence of oxygen. Exposure is made in a nitrogen environment from which the oxygen has been removed.

It is also possible to disperse pigment in non-photosensitive materials such as a polyimide. Positive photoresist is used for patterning.

Figure 3-4 *Transmittance of green pigment material as a function of pigment particle size*



Electrodeposition is another method for color filter formation. In this case, an ITO pattern is covered by a colorant such as polymer dispersed pigment. Electrophoresis, which has been used for automobile body painting, can be used. Normally, anionic deposition is performed in aqueous solution, but solvent media can also be employed. A highly crystallized ITO layer with resistivity of 20 Ω/square or less is required. The ITO electrode is patterned, and colors are electrodeposited one at a time. In this case, the black matrix cannot be formed from Cr thin film deposition that is used in dyeing or pigment dispersion processes. Alternatively RGB filters can be formed without patterning the ITO, using photoresist to mask each color.

Other kinds of color filter formation methods have been suggested, including multilayer interference films. This method has been used for image pick-up tubes, but because of a lengthy production process, the cost will probably be too high. It may have applications in projection type displays [4]. Alternative methods are listed in Table 3-8.The color filter pattern can be mosaic, triangular or striped, with pixels of 80-100μm size.

Table 3-8 *Alternative Methods of Color Filter Formation*

Multilayer interference film
Color Evaporation
Alumite coloring
Sublimation transfer
Photographic coloration
Lenticular
Electromist

The color filter spectral characteristics must be matched to the particular backlight being used so that the overall chromaticity matches that of the CRT as closely as possible. The color filter material must not elude ionic contaminants into the liquid crystal cell or otherwise adversely affect the liquid crystal material.

3.4.3 ELECTRODEPOSITION

Nippon Paint has developed an electrodeposition process for color filter manufacturing on unpatterned ITO [5]. The process makes use of a single positive photoresist application at its beginning. The photoresist is sequentially developed to allow the red, green, blue filter elements to be deposited. Finally, the photoresist is removed and a black border material composed of a mixture of the three colors is electrodeposited.

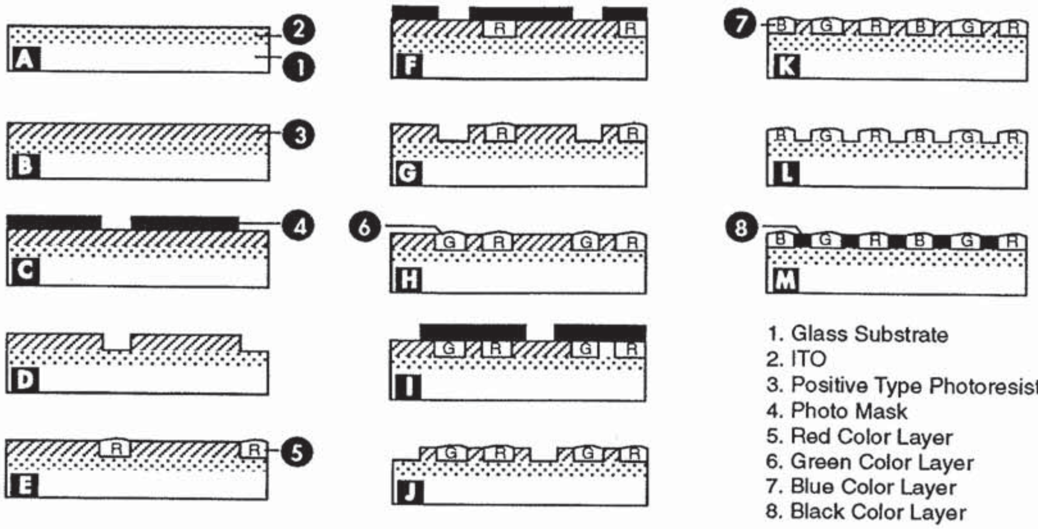
The process is shown schematically in Figure 3-5. The glass substrate is coated with ITO and photoresist, then patterned with UV light for the first color filter layer. After heating, the first area is developed with alkaline developer such as NaOH. The, the next two color filter patterns are formed in the same way, one at a time. Finally, the photoresist is removed, and the "black" material is plated in the areas between filters, a shown in the figure.

A new type of photoresist was developed for this process. The standard quinonediazide material lost its sensitivity after the process sequence of electrodeposition, alkaline development, and heating. This required the application of a new photoresist coating after each electrodeposition step. On the other hand, the new positive material, coated to a uniform thickness of 2μm, was exposed with 254nm UV light, 30mJ/cm^2, and developed with 0.5% sodium hydroxide solution.

Color filter materials are water dispersed resins. Initially, anionic resins were used, but when a second color was developed, the one that preceded it dissolved in the alkaline developer. Cationic resins were evaluated, but initially these caused the ITO film to turn yellow. New cationic materials solved this problem, and allow heating of the electrodeposited film at 100°C for 10 min in alkaline solution without dissolution. An emulsion of red, blue or green pigment is dispersed, and average particle size is less than 400nm.

The ability to strip the photoresist, leaving the color filters cleanly exposed at the edges, allows the final electroplating step of the black matrix, a composite mixture of red, blue, green pigments. Carbon black dispersions were also evaluated.

Figure 3-5 *Schematic of electrodeposition process for color filters*



Color filter production by electrodeposition is reported to be very slow, requiring many hours for each color. On the other hand, plating equipment is rather simple and inexpensive, and the process shouldn't need constant monitoring by production personnel. The process requires that ITO be deposited on the glass substrate prior to the color filters. This may preclude its use for AMLCD displays. When the cell is assembled, there is an added voltage drop compared to cells where the ITO is over the color filter material, caused by the high resistivity of the color filter material itself. This extra voltage drop is hard to accommodate in the active matrix scheme.

3.4.4 ELECTROMIST

Color filter material is deposited from a mist whose droplets have been charged to a few volts potential [6]. The color material is deposited directly onto the TFT pixel by addressing the TFT with up to 10-20V potential. Up to 30V can be placed across the TFT without damaging it. The color pigment deposits on the ITO layer over each pixel. No masks are required and three colors can be sequentially deposited in one step. A wide variety of color filter materials can be used, including inks, polyimides and sublimable dyes. The resolution of 160μm is better than currently required pixel pitch.

The apparatus consists of an ultrasonic mist generator, a drop size separator which produces 3μm nominal size drops, and a chamber in which the droplets are charged with an AC voltage. This method allows up to 0.008 coulombs/kg charge to mass ratio, much larger than achieved with DC charging. Positive air ions are formed at a DC corona wire and the droplets are swept out of the chamber in the air stream, which passes over the ITO coated substrate. The pixels are charged and drops deposit only on the pixels with negative charge. The deposition is self-limiting, reaching a thickness of 2μm.

3.4.5 OVERCOAT

Clear plastic material used over color filter material to protect color filter array, and to planarize the surface for ITO deposition. The ITO layer is relatively thin and cannot conform to feature thickness variations.

3.4.6 TWO COLOR APPROACH

Based on the work of Edmund Land, full color perception is possible using only two colors instead of three [7]. For example, a red/white pixel arrangement might produce the perception of full color with only 2/3rds the number of individual pixels and associated connections and driver circuits. The observations are especially relevant to automotive displays in terms of simplicity and cost.

3.5 Process Chemicals & Gases

Process chemical and gas requirements are very similar to those for integrated circuit manufacturing. Since tremendous strides in liquid and gas purity have been achieved for semiconductor applications, these can be adopted directly for flat panel display manufacturing.

In general, organic solvents are more widely used in processing liquid crystal displays, since the many organic polymer layers are soluble only in organic solvents. In addition, cleaning solutions often must be organic as well. Table 3-9 shows the properties of common organic solvents used in this application. This table and others in this section are taken from a recent handbook of LCD processing [8].

Improved purity in terms of lower particle levels has been the subject of active development at suppliers of semiconductor chemicals. Table 3-10 shows typical particle counts as a function of size for common process chemicals. The most important process chemical is the rinse water, supplied by an in-house system. Semiconductor grade water supply systems show performance like those of the firms in Table 3-11.

Table 3-9 *Solubility of Cleaning Chemicals*

Chemical	Formula	Boiling Pt. (°C)	Solubility in Water	Solubility in Alcohol
Acetone	CH_3COCH_3	56.5	Soluble	Soluble
Methanol	CH_3OH	64.56	Soluble	Soluble
Ethanol	C_2H_3OH	78.3	Soluble	Soluble
n-propanol	$CH_3CH_2CH_2OH$	97.2	Soluble	Soluble
i-propanol	$(CH_3)_2CHOH$	82.7	Soluble	Soluble
o-xylene	$C_6H_4(CH_3)_2$	144.0	Insoluble	Soluble
m-xylene		139.0	Insoluble	Soluble
p-xylene		138.0	Insoluble	Soluble
Trichloroethylene	$ClHC{=}CCl_2$	87.0	Insoluble	Soluble
Tetrachloroethylene	$CCl_2{=}CCl_2$	121.0	Insoluble	Soluble

Table 3-10 *Particles in Electronic Chemicals*

	Particle Size Range (μm)					Total
Chemical	2-5	5-15	15-25	25-50	>50	#/100cc
Trichloroethane	150	119	22	9	4	304
Acetone	172	90	8	8	0	278
Methanol	406	483	17	11	1	618
Xylene	203	43	12	4	1	263
Isopropanol	856	600	152	60	10	1678
Nitric Acid	3362	1627	204	38	3	5234
Hydrogen Peroxide	894	420	12	6	1	1333

Table 3-11 *DI Water Quality*

Property	Company A	Company B	Company C	Company D	Company E	Average
Resistivity (MΩ-cm)	>18	>15	>16	>15	>10	>16
Particles/liter	<150	<150	<100	<150	<100	<130
Particle size (μm)	<0.5	<0.5	<0.5	<0.5	<0.5	<0.5
Dissolved gas (ppm)	-	<200	-	<200	<200	<200
TOC (ppm)	<1.0	<1.0	<1.0	<1.0	<1.0	<1.0
Bacteria (colonies/liter)	-	<8	<10	-	<10	<9

Cleaning efficiency can be measured in a number of ways, including the contact angle measurement described in Part 2. Other ways of determining cleaning efficiency are shown in Table 3-12. These include static friction measurement. The higher the value of static friction, the cleaner the surface; contaminants such as organic films reduce friction. Another test is the LC chromatograph, for which the lower values indicate the highest cleanliness. Liquids such as hot water and acid provide the cleanest surface except for argon bombardment. Unfortunately, the material being cleaned will often react with these chemicals. In addition, acids tend to have a higher level of suspended particles, requiring careful rinsing and handling.

Table 3-12 *Measurement of Cleaning Efficiency*

	Measurement Method		
Method/Material	Wetting	Static Friction	LC Chromatograph
Methanol		0.41	0.7
Neutral Solution		0.39	0.41
Proprietary Chemical	Wetting	0.38	0.21
Hot Water	Wetting	0.53	0.17
Acid	Wetting	0.77	0.05
Argon Ion Bombardment	Wetting	0.63	0.03

Gases include deposition gases for chemical vapor deposition of amorphous silicon, silicon nitride, and silicon dioxide. Primary source gas is silane, with hydrogen as background gas in some cases for control of hydrogen content of deposited layer.

Photoresists 3.6

Positive and negative resist materials were recently evaluated for LCD applications using ITO coated glass substrates and an MRS panel printer for exposure [9]. The softbake condition was optimized for both kinds of resist, and is a critical parameter for good sensitivity and process latitude. However, the lower limit of 3.0μm resolution was achieved for all soft bake conditions. The mechanism for softbake conditions to influence ANR negative photoresist sensitivity depends on the effect of the solvent. Of course, increased softbake time and temperature leads to increased solvent removal. However, the solvent enhances the sensitivity of the resist, possibly by promoting increased diffusivity of photogenerated acid, the crosslinking agent. Similarly, post-exposure bake conditions strongly affected sensitivity while resolution limits remained the same. For post exposure process times of 110-130°C for 90-210 seconds, increasing the bake temperature by 10°C or bake time by 60 seconds increased the sensitivity by a factor of two.

For positive resists, the exposure latitude available can be used to ensure straight sidewalls even for small numerical aperture lenses. Both positive and negative resists will be needed for active matrix device manufacturing, and resists with adequate sensitivity and resolution, adapted from semiconductor photoresists, are available.

Etch resistance of photoresists parallels the requirements for IC processing, although for wet etching, less concentrated acids are used. Plasma etch requirements appear to be virtually the same.

Photoresist suppliers include Tokyo Ohka, JSR and Shipley. Standard negative and positive resists and associated developers and strippers are used in flat panel processing.

Photomasks 3.7

Steppers use standard photomask reticles made just like those for integrated circuit manufacturing. Typical reticles are 5" quartz plates, and steppers are configured to accept pellicles on both sides of the reticle. Reticle libraries allow storage and retrieval of needed masks. Design rules are typically 3-5μm for thin film transistor manufacturing. Suppliers include semiconductor reticle manufacturers, Toppan Printing, Dainippon Printing, and Sashin Kagaku.

Scanning projection or full projection exposure equipment requires a large mask, up to the same size as the glass substrate. For dimensional stability, the mask must be made of quartz. Very large quartz substrates are required, and specialized electron beam exposure equipment is needed. Quartz blanks are becoming available in Japan from mask substrate suppliers such as Hoya, SEH and Toshiba Ceramic. These blanks are very expensive, since cutting losses are very high. Diamond saws with very large saw kerf (cutting width) are required. Cutting is followed by laborious grinding and polishing to flat, optical finish on both sides. Standard sized blanks for use in integrated circuit mask making use well developed slicing and polishing equipment and processes not available for the large-sized substrates. In addition, the substantial investment needed for projection masks won't be made until the projection unit sales indicate that a large installed base of equipment will justify the demand. Until then, large quartz masks will remain very expensive items.

3.8 Orientation Films

Alignment of liquid crystals at the substrate surface refers to the orientation of the liquid crystal director at the surface, and can be either homeotropic or homogeneous. For homeotropic orientation, the liquid crystal director is perpendicular to the substrate. An organic surfactant can be applied to the substrate with long chains trailing off perpendicular to it, orienting the liquid crystal molecules in the same direction. New display materials based on homeotropic liquid crystals are being commercialized by Stanley.

Homogeneous orientation is more complicated. The liquid crystals are aligned with the director parallel to the surface. However, in addition to this orientation, the LC molecules must be oriented in a particular direction along the surface, which is more difficult than for homeotropic alignment. The orientation is accomplished by depositing and rubbing a thin organic film, usually polyimide. It is difficult to detect the change in the surface of the material after rubbing. In addition to determining the direction the liquid crystal molecules will follow on the surface of the substrate, the rubbing process controls the "pretilt angle" of the molecule, the slight angle the molecule makes with the substrate. This angle, ranging from 2°-8°, should be as high as possible for fast response STN displays. The mechanism by which a rubbed polyimide film of a certain composition achieves a given pretilt angle is not understood. Materials are developed and improved on an empirical basis.

3.8.1 POLYIMIDE ORIENTATION FILMS

During the 1970's, various kinds of material were investigated for the alignment of liquid crystals at the substrate surface, including inorganic compounds like silicon monoxide. Generally, liquid crystal alignment materials are heat resistant polymers with high T_g. Polyimides were selected based on properties such as mechanical strength, thermal strength, and low solubility in process solvents [10]. Normal aromatic polyimides must be baked at temperatures higher than 300°C, which is too high for color filters composed of organic polymer and dyes. Therefore, development of a film which could be cured at 180°C or below was undertaken. The material is an aliphatic cyclic polyimide which is soluble in solvents such as butyrolactone and NMP.

Generally, it is easy to align liquid crystal molecules, no matter what kind of material is used, if it is rubbed in a certain direction to align the material's molecules. However, liquid crystal stability after rubbing will be influenced by the materials used. Polyimides were found to be suitable in the early 1970's, and in the 1980's, flexographic printing was adopted as mass production machines for alignment film deposition. Generally speaking, a High T_g polymer will meet the requirement of alignment films, but producing a thin film is difficult. However, for polyimides, the precursor polyamic acid will dissolve in polar solvents. After thin film formation by the precursor, heating produces imidization and a satisfactory thin film. Table 3-13 shows the properties of alignment layer materials.

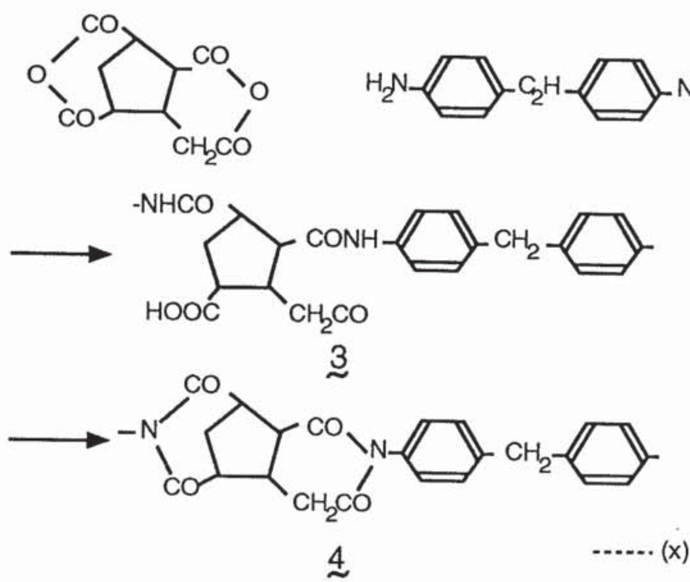
Table 3-13 *Alignment Film Material Requirements*

Required Property	Relevant Process
Thin film (<1000Å)	Film forming (flexo printing)
Adhesion to substrate	Film forming, rubbing
Chemical resistance	Cleaning
Adhesion to sealant	Sealing, Assembly
Thermal stability	Sealing, Assembly

For AMLCD's, standard polyimides cannot be used. Requirements for AMLCD include imidization at 200°C or lower, and good voltage holding ratio and RC time constant of liquid crystal cell. Standard polyimides required 300-350°C processing, and unstable polyamic acid radicals will remain in the film if cured at 200°C. NMP, used as solvent for standard polyimides, has a strong extractive power for the dyes used in color filters. Development work centered on eliminating the aromatic, conjugated molecular structure, since this was believed to affect the voltage holding ratio and RC time constant of the cell. In addition, the fully imidized material was targeted, which could be prepared as a thin film simply by evaporating the solvent.

Synthesis route and structural formula for a typical soluble polyimide are shown in Figure 3-6. No imidization was observed below 220°C, providing a very stable film. RC time constants of liquid crystal cells made using this alignment material are reported superior to conventional films. The imidization rate can be matched to device characteristics, and the alignment film optimized for each device.

Figure 3-6 *Synthesis and structure of aliphatic soluble polyimide*



Newer liquid crystal materials impact the alignment film in two ways. First, tilt angle is being added as a requirement, and improvement of afterimage is required. Tilt angle control is being pursued by modifying the STN alignment film materials. Control of afterimage is more difficult, since the relation between voltage holding ratio, afterimage and alignment film is not clear.

Further research is concentrating on developing alignment layers that require no rubbing.

A recent article by researchers at Nissan Kagaku Kogyo discussed the properties of polyimides used for orientation films [11]. An important ingredient in polyimide performance is to provide a high pretilt angle for the liquid crystal molecules. The higher the pretilt, the wider the viewing angle of the display. This is especially critical for STN displays, but is becoming important for TFT displays also. The Nissan researchers have investigated the effects of varying the molecular structure of the polyimide on the pretilt angle. Alkyl radicals were introduced into the polymer, providing a wide range of curing temperatures. Selecting the polyimide skeleton correctly allows maximum pretilt angle with minimum rubbing pressure.

Two factors influencing the pretilt angle of a polyimide are the polymer side chain groups and the presence of fluorine end groups. Pretilt angle is much higher when alkyl groups are present. The addition of fluorine reduces the surface tension, and further raises the pretilt angle. The higher the fluorine content, the higher the pretilt angle. At the same time, it is necessary to create polymers that are soluble in solvents such as NMP and EC. As a minimum the polyamic acid precursor must possess such solubility, but the cured polyimide is also evaluated.

The effect that long chain alkyls have on the polyimide depend on the stage at which the material is added. When reacted as a monomer, the effect is substantial. However, when mixed with polyamic acid, no effect is seen on pretilt angle.

The temperature dependence of pretilt angle is also important. Normally, pretilt angle increases with curing temperature in the range 150-300°C. This occurs even when fluorine is added, although the pretilt angle is higher with fluorine. However, an improvement or change in the alkyl bond can reverse the temperature dependence, resulting in higher pretilt angles at lower curing temperatures. This is obviously very important for orientation films over other polymers such as color filters, which are adversely affected by a high temperature cure.

Depending on the polyimide backbone, the pretilt angle varies with rubbing pressure. For all materials tested, *highest pretilt angle occurs with the lowest rubbing pressure.* A series of polyimides was measured, and measured surface tension for the polymers ranged in surface tension values from 22 to 47 dyne/cm. The pretilt angle was highest for the molecule with the lowest surface tension. If the rubbing pressure is increased by a factor of four, the pretilt angle declines almost a factor of two. Similar behavior is observed for the other molecules, but pretilt angles are lower than this. One result is to show the importance of the surface tension measurement and its role in selecting materials with high pretilt.

The final pretilt angle depend on curing conditions. It is essential to cure without overbaking the material. Overbaking leads to changes in threshold voltage of devices due to a residual voltage on the orientation film. Table 3-14 shows results from four polymer types.

Table 3-14 *Comparison of Polyimides for Orientation Film Applications*

Material	Pretilt Angle (degrees)	Resistivity (Ω-cm)	Residual Voltage (mV)	Overbaked
PI-A	5	$2x10^{16}$	340	Yes
PI-E	5	$1x10^{16}$	210	Yes
PI-F	4	$2x10^{16}$	20	No
PI-G	8	$2x10^{16}$	280	Yes

Different kinds of polyimide structures can generate different tilt angles in rubbed orientation films. Investigations by Spaulding and Estes compared polyimides' tilt angles using the magnetic-null method[11]. Experimental polyimides were deposited by spin coating on ITO covered glass and cured at 250°C. The 250Å films were rubbed using a NOMEX pile buffing wheel. Rubbing was verified for each cell by measuring the induced birefringence. Test cells were laminated with the rubbing directions antiparallel using DuPont WA-Acrylic adhesive, filled with Merck ZLI-2293, and cleared following data sheet information. The magnetic-null method employs an external magnetic field and measures the capacitance induced on the cell by the field. The angle of the magnetic field for which the capacitance is constant and equal to zero is obtained, and this angle is a function of the tilt angle. An extension of this method determined the slope of the reduced capacitance at the center of the cell. Tilt angles of 5.2-16° were measured for experimental polyimides. Such high tilt angles are needed for advanced STN and SBE (supertwisted birefringence) displays.

A recent report describes a process to stain and image the grooves formed in a polyimide film by the rubbing process [12]. Orientation films can be deposited by printing, with 1000Å-thick layers possible using flex-printing. Spin coating is also used. Orientation film suppliers include JSR, Hitachi Kasei, Toray, and Nissan Chemical.

Most STN and TN materials are aligned homogeneously, which means that the liquid crystal director lies in the plane of the glass substrate. If the liquid crystal director is aligned vertically with respect to the substrate, some display advantages are realized. These have been described by Clerc[13] of Stanley Electric, and include full color capability, wide viewing angle, and fast switching time. Development of vertically aligned displays has manufacturing benefits compared to STN displays, including less severe cell gap control (±0.2μm), ability to use standard sodalime glass substrates, and no need for a planarizing layer over color filters. Development work is underway on a 10" full color display for computer applications based on this new alignment scheme.

Vertical alignment of liquid crystals is possible using an orientation material that has alkyl (nonpolar) chains protruding at right angles to the substrate. These side chains have to be >200Å long, or about 12-14 carbon atoms in length. A lot of materials have this property, and the investigation by Stanley focused on choosing the most reliable and most easily manufactured material. Eventually, a material that could be offset printed was selected. This means that the same manufacturing equipment is still used when switching from STN to vertical alignment displays. A slight tilt of the liquid crystal molecules is necessary, or a special electrode design can compensate for 0° tilt.

Optical compensation was achieved using a ionomer single film compensator possessing an isotropic phase at high temperature. The film is pressed between two substrates, heated to the clearing point, then cooled to the birefringence phase under the external pressure. This locks in a vertical mechanical constraint, and orients the optical axis in the vertical direction as well. The extraordinary index of the film is lower than the ordinary, and the birefringent film has retardation zero, which is ideal for compensation of vertically aligned LCD.

Spacers 3.9

Spacers are used to control the cell gap of liquid crystal displays by maintaining a separation between the two glass plates. They are constructed of plastic or glass. Plastic spacers are spherical while glass spacers are often rod-shaped, and long fibers can also be used.

Sekisui Fine Chemical's Micropearl; SP is a spherical particle of cross-linked polymer, primarily consisting of divinyl-benzene. It has specific gravity and thermal expansion coefficient close to those of liquid crystal materials and is used for in-cell spacers. Requirements on spacers include no degradation of liquid crystal resistivity, sufficient compressive strength, high temperature capability, and flexibility at low temperature. Plastic spacer materials have an advantage in being able to match thermal coefficient of expansion and specific gravity (SG=1.19) of liquid crystal.

For STN displays, tone and color may be affected by the accuracy of cell spacing. The higher accuracy required on cell spacing, the more spacers that are required. Plastic spacers with a high coefficient of thermal expansion can help maintain the spacing even as the temperature changes. Therefore, plastic is mainly used in STN displays, for which cell spacing tolerance is very low, and for automotive displays which may be exposed to a wide temperature range.

Inorganic spacers have a higher compressive strength and can provide dimensional stability at high applied loads. On the other hand, plastic spacers are deformed by high loads, leading to a change in cell gap.

Spacer thickness is determined from the design parameter Δnd. Cell spacing, d is determined to an accuracy of 0.1μm, and tolerance is specified at ±1% for displays that operate over a wide range of conditions. Spacer size ranges from 3.0μm to more than 10.0μm with standard increment of 0.25μm. Some further fine adjustment of spacing can be achieved by controlling the dispersion density of the spacers. The cell gap is not necessarily equal to the spacer dimension, since some spacer deformation will occur. This means that the proper spacer size is determined empirically by selecting several sizes and determining the cell gap each one produces. Typical sizes and standard deviation of size are shown in Table 3-15.

Table 3-15 *Plastic Spacer Size Variation*

Nominal Size (μm)	Standard Deviation (μm)
3.00 ± 0.05	0.21 ± 0.03
5.00 ± 0.05	0.30 ± 0.03
7.00 ± 0.05	0.34 ± 0.04
9.00 ± 0.05	0.45 ± 0.05

Compressive strength of plastic spacers is temperature dependent, and is about 20% lower at 180°C than at room temperature. Thermal expansion coefficient is also temperature dependent, as shown in Table 3-16 below.

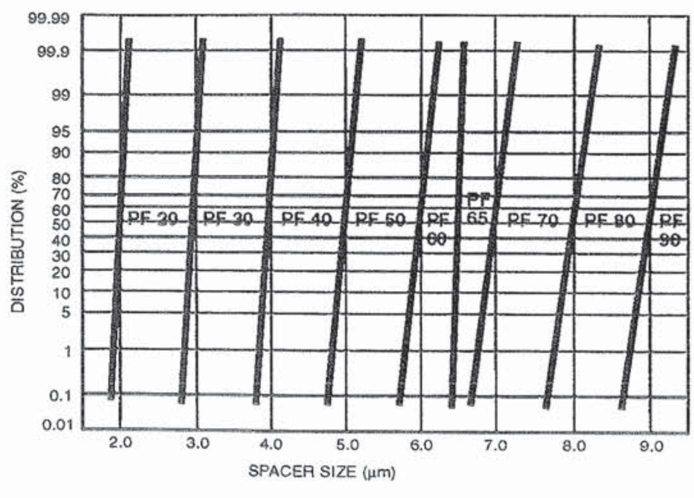
Table 3-16 *Plastic Spacer Thermal Expansion Coefficient*

Temperature range	30-60°C	60-200°C	200-280°C
Thermal expansion coefficient (x10^5/°C)	4.7	5.4	3.7

Several methods can be used to apply spacers to the glass substrate. Spacer spray equipment using specially designed nozzles is most common, with spacers contained in a dispersion agent such as alcohol, Freon, or water/alcohol mixtures.

Precision silica fiber spacers are available from Tokuyama Soda and others. These are manufactured from high purity SiO_2, and are available in diameter distributions similar to plastic spacers. Fiber length varies from 50μm to 200μm. Figure 3-7 shows diameter distribution graphically.

Figure 3-7 *Glass fiber spacer size distribution.*



Sealing Materials

3.10

Generally, thermosetting or UV curable epoxy resins are used as sealant materials. It is essential that the material be inert after curing, so as not to degrade the resistivity or other properties of the liquid crystal due to constant contact. By themselves, epoxy resins won't usually degrade the liquid crystal material, but the amines present in thermosetting material dissolve in the liquid crystal. Therefore, after screen printing the thermosetting resin, the hardening temperature is approached in stages, using prebaking to evolve these amine groups. An alloy of phenoxy and epoxy resins, joined to a silicone rubber has also been proposed as a substitute for amine chemistry.

Instead of thermosetting epoxies, UV hardening epoxies are also available. However, it is difficult to harden the glue in the UV resin by exposure to light alone, so after UV hardening, a postbake treatment is used. The seal strength of UV resin is low compared to thermosets, so thermosetting resins are commonly used.

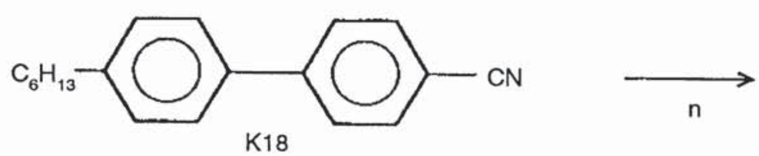
In case there is an orientation film covering the area where the seal is deposited, there will not be an intimate bond between seal, orientation film, and substrate, and the seal will not be hermetic. In order to avoid this, it is possible to mask the area to be sealed prior to orientation film deposition and rubbing. However, this results in a very complicated manufacturing process, and has not been implemented. More recently, where the orientation film covers the entire substrate, it is removed in the area where the seal material is to be deposited. Both hot etching and plasma etching have been employed for this step. For ease in removal of the orientation film in the seal area, photosensitive polyimide can be used as the orientation film material.

Seal materials are available from Hitachi, Nihon Kayaku, and Mitsui Toatsu.

3.11 Liquid Crystals

Liquid crystal materials are rod-like molecules typified by the cyanobiphenyl compound shown in Figure 3-8. The director, n, of a liquid crystal is a unit vector parallel with the long axis of the molecule.

Figure 3-8 *Typical liquid Crystal*



For the Nematic Phase, molecules are oriented at random in the liquid, but the directors of the molecules are parallel, as in Figure 3-9. Thermal motions of individual molecules perturb the alignment, but, on the average, the bulk director is invariant.

The Cholesteric Phase is also characterized by random molecular position, and parallel alignment of the director. However, in the cholesteric phase, the director rotates from layer to layer through the bulk, adopting a spiral structure as shown in Figure 3-10. The pitch, p, of a cholesteric liquid crystal is defined as the distance for which the director rotates through 360°, and is important especially for supertwist devices.

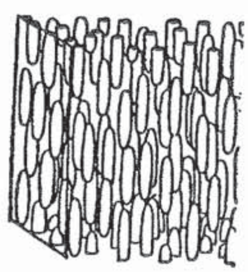


Figure 3-9 *Nematic phase*

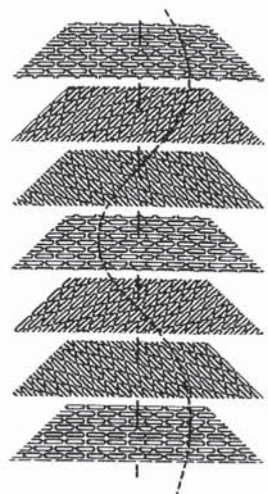


Figure 3-10 (Center)
Cholesteric phase

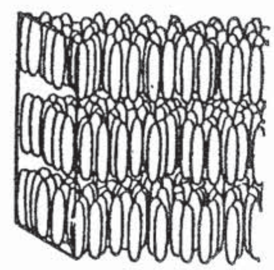


Figure 3-11
Smectic phase

Making a cholesteric phase requires the addition of chiral, or optically active molecules. The mixture of small amounts of chiral material with nematic liquid crystal material produces a cholesteric phase with a long pitch, the value of p depending on the amount of chiral mesogen added. In fact, the nematic phase can be considered as a special case of a cholesteric phase with infinite pitch.

Smectic A (S_A) material is characterized by parallel alignment of the molecular director. However, there is also positional order, and the molecules form layers with the director parallel to the layer normal, Figure 3-11.

Chiral Smectic C (S_C*) phase has a similar layered structure, except that the molecular directors are tilted at a constant angle (the tilt angle) to the layer normal. In a chiral smectic C phase, the presence of chiral or optically active molecules cause the director to rotate from layer to layer, the tilt angle remaining constant.

All liquid crystals used for display manufacture are thermotropic - they are formed by melting mesogenic solids. Liquid crystals for displays are typically mixtures of several compounds aimed to optimize several physical properties for specific applications. A mixture may exhibit a number of different liquid crystal phases; a typical phase sequence is shown below.

crystalline (K) -> smectic A (S_A) -> smectic (N) -> isotropic (I)

The properties of the liquid crystal materials are often anisotropic, specifically the dielectric permittivity (Σ), and the refractive index (n). Table 3-17 shows the physical properties specified in a liquid crystal formulation.

Table 3-17 *Parameters Specified in Liquid Crystal Formulations*

Designation	Property	
K -> N	Phase transition	Melting point, crystalline - nematic
K -> S_A	Phase transition A	Melting point, crystalline - smectic
S_A -> N	Phase transition	Transition point, smectic A - nematic
N -> I	Phase transition	clearing point, nematic - isotropic
$\Delta\Sigma$	Dielectric anisotropy	
Δn	Optical anisotropy	
n_{20}	Kinematic viscosity at 20°C	
V(90,0,20)	Threshold voltage	Voltage at 90% of maximum transmission at perpendicular viewing angle and 20°C, crossed polarizers
V(10,0,20)	Saturation Voltage	Voltage at 10% of maximum transmission at perpendicular viewing angle and 20°C, crossed polarizers
V(90,45,20)		Voltage at 90% of maximum transmission, 45° viewing angle, and 20°C, crossed polarizers
V(x,y,z)		Voltage at x% of maximum transmission, y° viewing angle, z°C
M_{20}	Margin	M_{20}=V(10,0,20)/V(90,45,20)
M'_{20}	Margin	M'_{20}=V(50,10,20)/V(90,45,20)
A_{11}, A_1	Absorbance	Absorbances in a dye solution parallel and perpendicular to the director
S	Order parameter (dye)	$S=(A_{11}-A_1)/(A_{11}+2A_1)$

Material resistivity is another important parameter not listed in the table. In general, resistivity must be high, and for active matrix devices, as high as possible.

Twisted Nematic (TN) liquid crystal displays are used for small displays, and homogeneous alignment is used in cells with a gap of about 10μm. The orientation film is rubbed so that the director lies parallel to the surface of the glass with a small tilt angle of 2° or so. The rubbing directions of the two glass plates of the display are mutually perpendicular, and the nematic liquid crystal forms a twisted structure with a 90° rotation of the director from one plate to the other. A small amount of chiral material is added as an anti-reverse twist additive, to prevent a defect known as reverse twist. The liquid crystal is actually a long pitch cholesteric, rather than a true nematic.

Specifications for a liquid crystal mixture depend on the application. For example, automobile dashboard displays require a mixture with a broad operating temperature range, capable of switching in 1 second at -30°C, indicating a low viscosity fluid. On the other hand, a high information content display, normally used indoors, requires a low value of M_{20}.

Although simple matrix displays can be addressed by direct drive, higher information content displays require multiplexing. A matrix of NxM segments can be multiplex driven N ways using N+M connections. The drive scheme results in a voltage of V(off) or V(on) applied to OFF or ON segments respectively, where

$$V(off) = \frac{V}{S}\sqrt{\left[\frac{N = (S-2)^2 - 1}{N}\right]} \qquad V(on) = \frac{V}{S}\sqrt{\left[\frac{N + S^2 - 1}{N}\right]}$$

V = Supply Voltage $\quad$ *1/S = Select Scheme* $\quad S = 1 + \left[\sqrt{N}\right]$ *(or nearest integer value)*

Both OFF and ON segments have a voltage applied, requiring that the electro-optic response of the liquid crystal should be as sharp as possible, indicated by a low value of M_{20}. Because of variations in V, N, and S, the threshold voltage of the liquid crystal is critical. Ranges of V(90,0,20) from 1.01V to 4.03V are available.

The liquid crystal manufacturer can supply 2-bottle or 3-bottle systems which consist of identical formulations with either 1 or 2 variable components. Mixtures can be continuously adjusted to vary a single property of the formulation, such as V(90,0,20), while holding the other properties constant. This is useful in display development.

Supertwist (STN) devices are used where the level of multiplexing is high (N>100) and adequate contrast is difficult to achieve with TN material. Twist angles >90° allow the electro-optic threshold to be improved. Addition of a chiral dopant to the nematic mixture is necessary to ensure the correct twist angle, and a high tilt alignment is usually required for twist angles >220°. Commonly, twist angles range from 180-270° for STN displays, and the liquid crystal formulation contains more than 20 components.

Devices built with supertwist material include supertwisted birefringence (SBE) devices, with a twist angle of 270°. This requires a high tilt alignment layer to avoid an undesirable scattering texture in the ON state. Optical mode interference (OMI) devices offer a positive contrast, black and white display, where the optical performance is less susceptible to variations in cell thickness than STN or SBE devices. The brightness is lower than STN or SBE displays, and may be inadequate for reflective displays. Low birefringence is required.

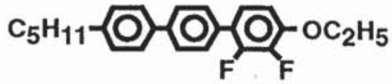
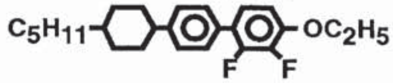
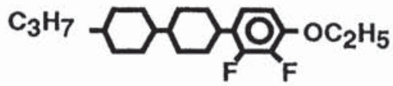
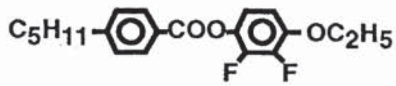
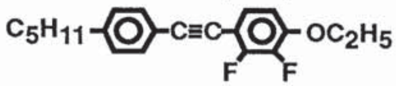
Recent improvements in liquid crystal materials focus on the addition of fluorine or other functional groups which terminate the polymers and provide added performance. The response time of STN materials can be improved with fluorine terminations. In addition, the twisted nematic molecules suitable for active matrix displays require extremely high resistivity, on the order of 10^{13} Ω-cm, and the resistivity of the polymers is increased with the addition of fluorine. Figure 3-12 shows examples of high performance STN materials, and Figure 3-13 molecules for active matrix displays [14].

3.11.1 OTHER LIQUID CRYSTAL MATERIALS

Guest-Host (GH) devices employ nematic mixtures containing a dichroic dye. A molecule of a positive dichroic dye will selectively absorb certain wavelengths of light, incident normal to its long axis. This absorption falls to a minimum for light incident parallel to the long axis. When the dye (guest) is mixed with a nematic liquid crystal (host), the dye molecules line up parallel to the bulk director of the liquid crystal, producing anisotropic absorption of light at certain wavelengths. The tendency of the dye molecules to align with the nematic director is measured by the dye order parameter, S. In general, S should be high, normally >0.7.

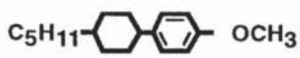
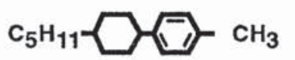
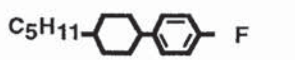
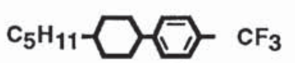
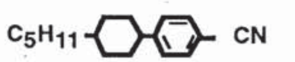
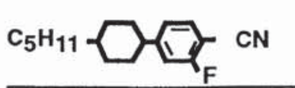
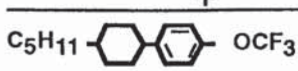
Certain chiral smectic liquid crystal phases exhibit ferroelectric properties, which can be used in electro-optic devices. The most commonly used ferroelectric phase is the chiral smectic C (S_c^*) phase. In the bulk, because the director spirals through the material, there is no net polarization. However, using suitable boundary conditions, the helical condition can be "unwound" and thin layers of S_c^* materials can show net electrical polarization.

Figure 3-12 *Molecular structure and physical properties of 1,4 - disubstituted - 2,3 - difluorobenzene derivatives.*

	t (°C)	ΔΣ	$V (mm^2 * s^{-1})$	Δn
	K 105 S_C 135 N 185 I	-4.2	49	0.27
	K 68 SA 87N 172 I	-4.1	46	0.18
	K 76 SB 79N 186 I	-4.4	39	0.13
	K 51 N 63 I	-4.6	18	0.09
	K 57 N 61 I	-4.4	17	0.25
	K 84 N 229 I	-4.1	27	0.29

ΔΣ, *V* and Δn extrapolated values

Figure 3-13 *Trans-4-n-pentylcyclohexyl (PCH-5) derivatives.*

	Mesophase (°C)	ΔΣ	$V (mm^2/s)$
	K 41 N (31) I	-0.5	8
	K 25 N (-4) I	+0.3	7
	K 34 I	+3	3
	K 10 I	+11	9
	K 37 N 51 I	+11	12
	K 31 N 55 I	+13	22
	K 13 N (5) I	+18	28
	K 14 I	+7	4

The surface stabilized ferroelectric liquid crystal (SSFLC) described by Clark and Lagerwall is similar to a TN device except that the cell is much thinner, typically about 2μm, and the rubbing directions on the alignment layers are parallel[15]. The S_c^* material fills the cell, with layer normals parallel to the rubbing directions, and with the molecular directors in planes parallel to the glass plates, and at an angle ±Ø (the tilt angle) to the layer normals. These states have opposite electrical polarity and the molecules can be switched between the +Ø and -Ø states by applying a DC voltage of the appropriate polarity. Crossed polarizers produce bright and dark states respectively, due to the birefringence of the liquid crystal.

The advantage of this type of display is that switching times of a few microseconds can be achieved, and high levels of multiplexing can be employed. Ferroelectric displays are being studied as an alternative to active matrix devices for high information content displays. Other, non-display applications for ferroelectric devices include printing heads and fast optical light valves and shutters.

3.11.2 POLYMER DISPERSED DISPLAYS

Polymer dispersed liquid crystal (PDLC) materials have been discussed for a variety of applications including shutters for window glass, projection screens, signboards, and even projection TV shutters. Typically, the difference between the Off and On state of the material is a transition from light scattering to clear. This might discourage its application to direct view displays. However, researchers at Hughes have discovered a way around some of the difficulties of PDLC display manufacturing. Specifically, they have created spatially separated regions where liquid crystal polymer droplet sizes differ, providing regions of high scattering where address lines can be hidden [16].

By varying the liquid crystal droplet size in designated regions, direct view polymer dispersed liquid crystal displays are constructed with simple addressing schemes. A multiple droplet size PDLC is used to hide addressing line voltage effects in a segmented display which requires a clear background. Edge-lighting improves the contrast of the displays.

The PDLC material consists of droplets of the liquid crystal BDH-E7 (British Drug House Ltd.), dispersed in a matrix of NOA65 (Norland Optical Adhesives), where the PDLC is formed by the polymerization-induced phase separation technique. When exposed to UV light, NOA65 polymerizes, phase separation occurs, and liquid crystal droplets form. The droplets coalesce and grow until the polymer matrix becomes rigid. The intensity of the UV light determines the time available for droplet growth. High intensity UV produces small droplets by causing polymerization to occur rapidly. Conversely, for low intensity light, larger droplets are obtained.

With sufficient voltage drop, V, across the substrates of a PDLC of thickness d, the liquid crystal in the droplets aligns and the PDLC switches from scattering to clear. Whether or not a voltage is large enough to switch the PDLC is determined by the relative values of the free energies of the droplet with and without the voltage. With no voltage present, the free energy of the droplet is proportional to K/r_d^2 where K is an effective elastic constant of the liquid crystal and r_d is the radius of the liquid crystal droplet. With a voltage applied to the substrates of the PDLC, the free energy of the droplet is proportional to $(V/d)^2$, where d is the polymer layer thickness. Relating these two proportionalities yields a droplet size dependent switching voltage for the PDLC, $V \sim (d/r_d)K^{-1/2}$. The relationship has been experimentally confirmed.

In order to create regions in the material with different droplet sizes, the UV exposure was conducted through a mask whose transparency varied from 8-39%. This created a droplet-size dependent turn on voltage as shown in Table 3-18.

Table 3-18 *Relation Between UV Exposure and Turn On Voltage*

UV Exposure Relative Intensity (%)	Turn On Voltage
8	5
11	10
17	20
27	39
39	50

Displays were made with a continuous ITO coating on one substrate, with a patterned substrate on the other surface. For a 20μm thick display and a voltage greater than 110V, the entire display is clear. If the voltage on one segment is between 45V and 110V, the segment scatters while the addressing line remains clear. Edge lighting of the display can enhance its contrast.

Other applications for PDLC materials have been discussed previously.

3.11.3 POLYMER NETWORK DISPLAYS

A polymer network liquid crystal (PNLC) display differs from a polymer dispersed liquid crystal ((PDLC) display in several important ways [16]. The PDLC is well known from Fergason's work, and consists of dispersion of droplets of liquid crystals in a polymer matrix. Polymer network materials, PNLC, disperse a nematic liquid crystal as a random network of molecules. The networks are prepared using acrylate oligomers and/or monomers, and light-induced polymerization.

The light-scattering type of polymer films such as PDLC and PNLC have advantages such as high brightness, wide viewing angle, and simplicity of fabrication. Disadvantages of PDLC include high driving voltage, requirement for matching index of refraction of liquid crystal and polymer matrix, and temperature dependence of transmission-voltage characteristics. The first few disadvantages can be overcome using PNLC, for which index matching is not a requirement, and for which greatly reduced turn-on voltages have been achieved. Drive voltage has been reduced to below 5V, probably because of the weaker surface interaction on a polymer network than for the droplet of a PDLC. The sharpness γ ($=V_{50}/V_{10}$) of the transmission-voltage characteristic is 1.3-2, and maximum number of multiplexible lines is therefore 2-15. This is much better than PDLC, but is inferior to TN displays. Other factors influencing the performance of the displays include viewing angle dependence and temperature dependence of transmission-voltage characteristic. The latter variation is higher than for TN displays, and needs improvement.

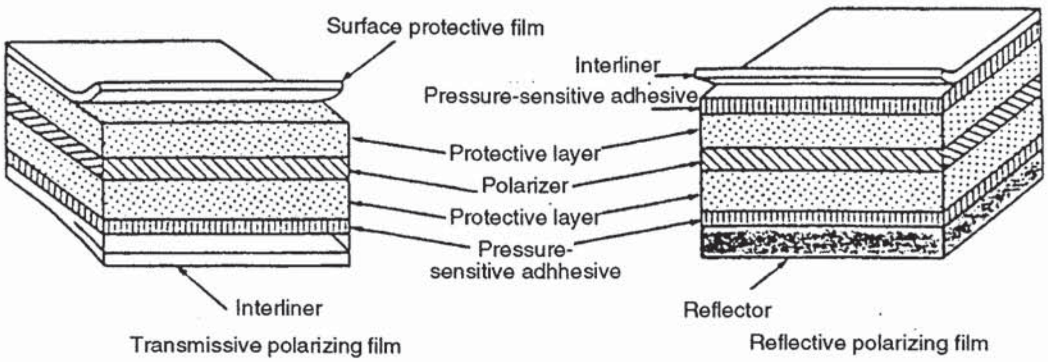
3.12 Polarizers/Compensation Films

Polarizing films are applied to both sides of an LCD display. Any trapped air in the interface between the film and the LCD causes a reflection loss of about 4%. Therefore, uniform bonding of the film is critical. A multilayer structure has been developed to protect the polarizer both before and after application, to ensure good bonding, and maintain high transparency. Figure 3-14 shows the structure of transmissive and reflective polarizer films developed originally for watches. Transparent acrylic adhesive approximately 25µm in thickness is used in this film.

Persistent problems with air bubbles and delamination of the polarizer were solved by the introduction of vacuum bonding, applied as roller bonding combined with autoclaving in production. Conditions are:

- General purpose (to 80°C), 50°C, 0.49 MPa (5kg/cm²), 15 min
- Hi-durability (to 90°C), 70°C, 0.49 MPa, 15 min

Figure 3-14 *Structure of polarizer film for LCD*



Several types of protective layers, reflector materials and adhesives have been developed to suit special applications. For example, high durability polarizing film (Nitto type Q) had a newly developed dye polarizer between reinforcing cellulose triacetate (TAC)-acrylic protective layers. These polarizers are suitable for the conditions experienced by LCDs in automobiles and gasoline pump displays. Nitto type QE material employs iodine polarizer material in a similar structure. Types Q and QE are applied to the upper and lower parts of the display. Films of this type with added color are also available.

Improvements in materials performance resulted in newly designated polarizer materials Type F, with TAC support layers, and Type G, high contrast material. A summary of polarizer film designations is shown in Figure 3-15 and Table 3-19.

Figure 3-15
Polarizer film structures

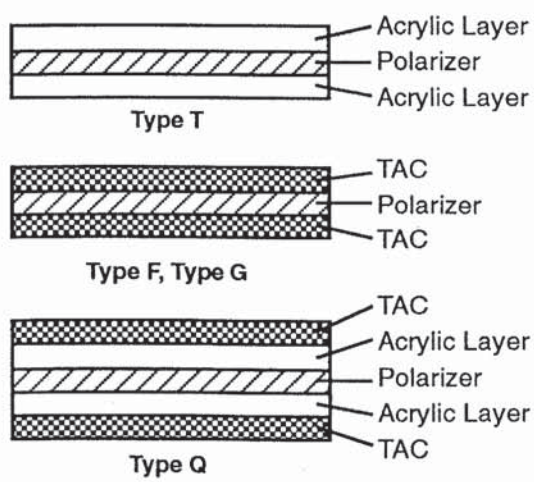


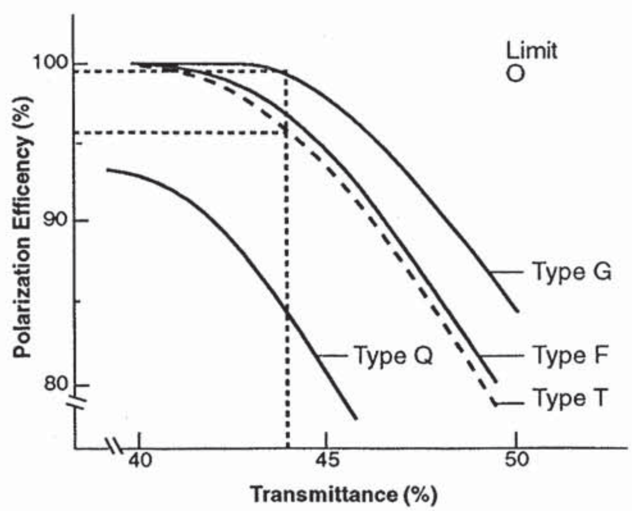
Table 3-19 *Polarizing Film Structures*

Designation	Polarizer Material	Protective Layer	Product Application
Type F	Iodine	TAC(cellulose triacetate)	Watches, calculator, general applications
Type G	Iodine	TAC	STN and AMLCD instrument displays
Type T	Iodine	Acrylic	Thin displays
Type QE	Iodine	TAC-acrylic 2 layer	Automotive, outdoor use
Type Q	Dye	TAC-acrylic 2 layer	Automotive, outdoor use

Other materials that can be added include aluminum reflector, high transmittance reflector, retardation films and antiglare films. The relation between polarizer transmittance and efficiency is shown in Figure 3-16.

A retardation film is a uniaxially stretched high molecular weight film which is formed by thermal stretching after film formation by a special T die extrusion method where polycarbonate resin is used as the raw material. The T die film

Figure 3-16 *Transmittance vs polarization efficiency of different polarizers*



formation method and uniaxial stretching are widely used for thin organic films. The optical performance of the retardation film for LCD applications must be equivalent to inorganic crystalline optical materials.

Nitto's new z-axis retarder, "NRZ" is a one component polycarbonate film, just announced in August, 1991. It represents an improvement over the 2-component film , which was composed of polycarbonate and styrene (for z-axis compensation).

Mounting the retardation film on the display requires maintaining the optical axis at a given relation to the polarizer, which increases the panel brightness by eliminating reflections. To ensure good adhesion to glass and to polarizer, special adhesives and laminating technology are used to provide an integrated retarder/polarizer product. Display designers may require unique retarder arrangements for each new display.

Retardation films have light transmittance of 90% or greater including the adhesive layer. The retardation value Δnd can be set to any value from 250nm to 800 nm. Retardation value of standard product is 300, 400, 500, and 600nm. Dispersion is less than ±2%. Under life test conditions for 500 hours at 70°C and 500 hours at 40°C/90% RH, retardation value was unchanged.

Elliptical polarizing film is obtained by bonding the retardation film to the polarizer at a specific angle, generally 45°.

Polarizers are supplied primarily by Nitto Denko and Sanritz. Arisawa also supplies polarizers. These companies also supply polarizers with compensation films attached, the usually embodiment of this product. Manufacturers of compensation films include Sumitomo Chemical and Kayapola.

Die Attach/Connector Materials

3.13

Die attach methods were described in Chapter 2, and make use of chip on board, chip on film, and chip on glass mounting techniques. Many aspects of die attach are identical to those for semiconductors and will not be described here. One example is standard printed circuit boards used in chip on board construction. However, the heat seal used in connecting the display to the printed circuit board can be a unique product for this application. Figure 3-17 shows two embodiments of such a heat shield connector, in which the graphite thermal conductor is covered by silver electrical conductor in two different ways. The pitch that is possible using screen printing to form the conducting and insulating patterns is 260μm. New kinds of heat shield connectors are being offered, constructed from etched copper foil combined with anisotropic conductive paste. In this case, patterns of 100μm pitch are possible.

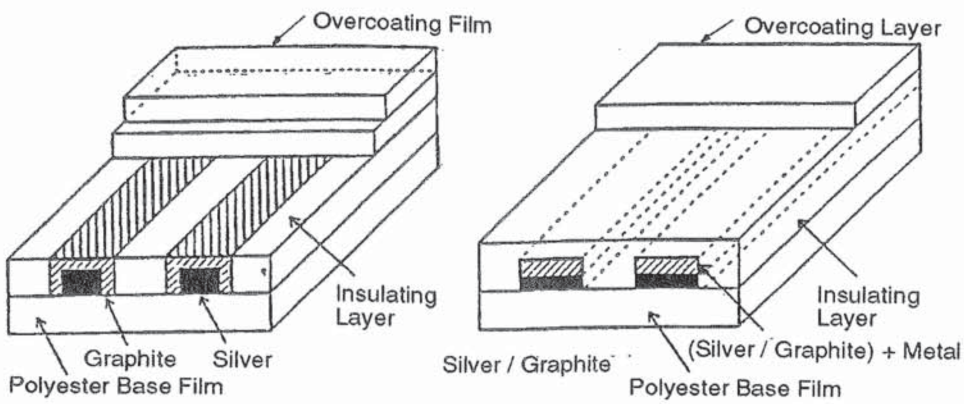
When chip on board and heat seal assembly methods are used, it is possible to repair the module by disconnecting the heat seal and cleaning the liquid crystal terminal leads with solvents.

Chip on film methods make use of tape automated bonding (TAB) die attach. In this method the die is first mounted to a flexible tape containing the electrical leads (inner lead bonding). These leads are then bonded to the connectors on the film or flexible circuit board (outer lead bonding). In the past, it was standard to bond the inner and outer leads using a tool which simultaneously attached all the leads (gang bonding). However, for very complex chips with as many as hundreds of leads, the complexity has lead to a return to single point bonding, in which leads are connected one at a time.

TAB ICs are used mainly in liquid crystal display applications, where savings in packaged display size and weight are of great importance. Figure 3-18 shows a pie chart representation of TAB IC usage by product. Including consumer products such as the schedular (which uses a display), LCD related TAB usage is about 80% of the total.
Flexible circuit boards are connected to the display using anisotropic conductive film, which has been described in Chapter 2. This film is electrically conducting in the thin dimension between display and film, and insulating in the other two directions. Anisotropic conductive film is available in thermosetting and thermoplastic versions. Thermoplastic film can be removed for repair. Thermoplastic resins such as SBR and polyvinylbutylene can be used. Thermosetting resins include epoxies, urethanes and acrylics. Conductive particles dispersed in the resin are of a variety of types, including carbon, metal, and metal-plated plastic spheres. Particle size determines the final separation of ITO and copper, and can range from 5μm to 10μm. Anisotropic films allow connections as close as 10 electrodes/mm. Suppliers include Hitachi Chemical.

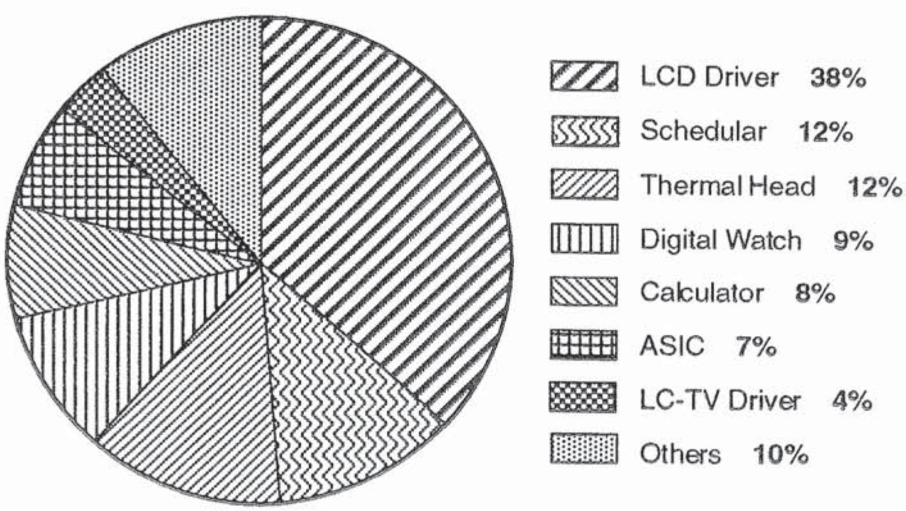
Direct connection of driver circuits to the glass substrate represents the ultimate reduction in size and weight of the display. A variety of techniques for chip on

Figure 3-17 *Heat seal connector construction* [17].



glass attachment have been developed[18]. Most of these make use of special bumps or protrusions on the IC chip instead of flat bonding pads used for wire bonding. These bumps are usually plated or formed by other means over the original bonding pads. The IC is aligned to the connections on the glass with a special tool. The bumps are then bonded to the ITO or metal on the glass substrate by solder, conductive adhesive or other means. Figure 3-19 summarizes the different chip on glass techniques including bonding parameters and whether or not faulty connections can be repaired. Repair is seen as an essential requirement for chip on glass manufacturing.

Figure 3-18 *Usage ratio of TAB ICs*



Shown in Table 3-20 is the cost breakdown of an STN display. This display represents the minimum cost possible using standard 2 layer PC board construction with chip on board mounting and a heat shield connector from the board to the display. This display does not make use of retardation films, so it is a blue mode display suitable for a "heavy" laptop weighing 7-10 pounds. Total factory cost is $180, and the selling price is below $200. Higher quality displays with retardation films for true B/W display, lightweight TAB mounting of circuits on flexible boards command a premium of $30-40 over this example.

Some industry observers expect the LCD driver IC market to reach $770 million in 1995. LCD driver IC production is estimated at over $200 million in 1991. Driver IC costs vary from $2 each to $6 each, depending on complexity andvolume required. Sharp has a monthly production capacity of 10 million units, mainly TAB (tape-automated bonding) packages. Oki Electric plans to boost its production capacity from the current 5 million units monthly to 7.5 million units. Hitachi's production capacity will reach 6 million units. Toshiba has increased LCD driver IC production to 2 million units per month, and NEC will double monthly production to 2 million units in 1992.

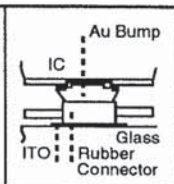
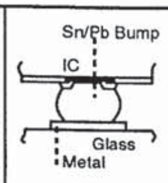
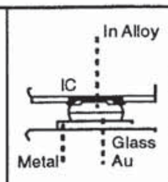
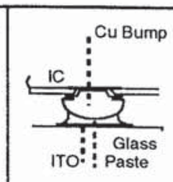
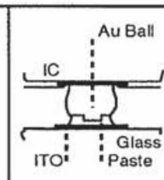
3.14 Display Backlighting

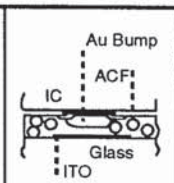
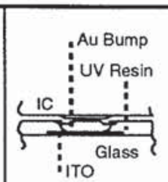
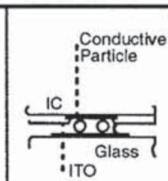
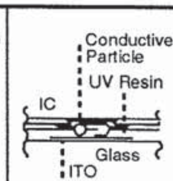
Backlight technology is an important consideration in terms of portable computer performance. High brightness at low power consumption is essential for long battery life between recharging. Improvements in transmittance of liquid crystal displays themselves will be limited in the next few years. In fact, overall transmittance is going down as manufacturers add retardation films, color filter arrays, thin film transistors, and other performance enhancing layers. Therefore all improvements in the brightness/power ratio must come from backlight improvements.

At one time, electroluminescent panels were considered as backlight sources, and at some point in the future, these may constitute a viable option. At the present time, the industry standard is the cold cathode fluorescent lamp, supplied by Ushio, Mitsubishi Rayon and other Japanese firms. The lamp is incorporated in a diffuser housing to spread the light uniformly behind the liquid crystal display. The basic arrangement was shown in Chapter 2.

Recent improvements in backlighting technology were reported by Hathaway

Figure 3-19 *IC bonding methods in chip on glass packaging*

Bonding Configuration						
Bonding Method		**Rubber Connector**	**Solder**	**In Alloy**	**Conductive Paste**	**Conductive Paste**
Driver IC	Pad	Au Bump	Sn/Pb Bump	Au/In Bump	Cu/Au Bump	Au Ball
	Pitch	100-300um	200-300um	50-150um	100-150um	60-130um
LC Panel ITO		Au	ITO	ITO	ITO	ITO
Bond-ing	Temp	RT	300-350°C	120-150°C	100-120°C	100-120°C
	Pressure	<5 g/Pad	—	<20 g/Pad	1-2 g/Pad	<50 g/Pad
		—	—	—	—	—
Repa Rability		O	X	O	O	O

Bonding Configuration						
Bonding Method		**AFC**		**Conductive Particle**	**Conductive Particle**	
Driver IC	Pad	Au Bump	Au Bump	Al Pad	Au Pattern	
	Pitch	150-200um	<50um	60-130um	50-300um	
LC Panel ITO		ITO	ITO	ITO		
Bond-ing	Temp	160-180°C	RT	150-200°C	RT	
	Pressure	<50g/Pad	10-20 g/Pad	10-20 g/Pad	—	
		—	UV Light	—	UV Light	
Repa Rability		Δ	O	Δ	O	

and coworkers at Display Engineering, San Mateo, CA [19]. One such improvement involves the use of a wedge-shaped plastic light pipe which spreads light from a single lamp over the display area in a uniform fashion. Figure 3-20 show the construction of this device.

The wedgelight construction allows a single lamp to illuminate the display. The plastic molded light pipe contains prismatic specular reflectors which spread the light uniformly across the front plane of the device. Figure 3-21 shows the spatial brightness uniformity measurement.

In addition to improvements in conventional cold cathode lamp, a flat fluorescent lamp that directly illuminates the display is under development. Figure 3-22 shows the construction of the display, which measures only 3mm thick. Diagonal lengths from 25mm to 350mm should be possible using conventional cold cathode technology. The envelope of the lamp is constructed using one flat plate and one formed plate. A typical lamp consists of a serpentine channel of 4 intervals and an electrode on each end. This creates an effective lamp length of 800mm. Design of the flat lamp includes phosphor coating on both plates, with a reflective coating on the bottom plate. Currently, high voltages of 2,000-3,000 volts are required to operate the lamp. Table 3-21 provides a comparison of current backlight technologies.

Figure 3-20 *Construction of WedgeLight™ backlight*

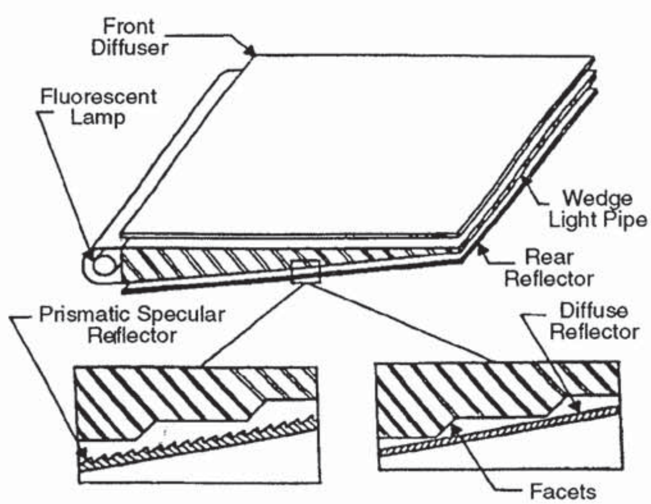


Table 3-20 *STN Display Cost*

Item	Total Cost ($)	Unit Cost
Control Circuits	12	
Driver ICs	44	$2
Printed circuit board	13	6x11" @ $.20/sq in
Frame	4	
Elastomer connector	3	
Liquid crystal display (incl. polarizer)	45	
(polarizer)		$3 each w/o retarder
Backlight	(5-7)	$2.40 lamp + $2.30 diffuser
Total materials	126	
Assembly cost	24	
Standard cost	150	
Overhead	30	
Total cost	**180**	

Figure 3-21 *Spatial brightness uniformity of Wedgelight ™*

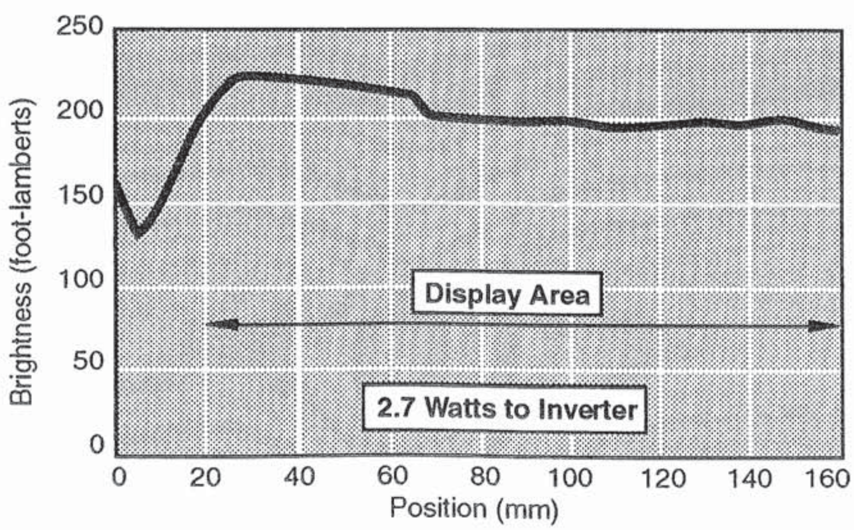


Table 3-21 *Comparison of Backlight Technologies*

Parameter	Light Curtain	Conventional Lightpipe	Flat Fluorescent	Wedgelight Lightpipe
Total Length (mm)	280	225	235	220
Total Width (mm)	180	173	138	165
Display Length (mm)	188	188	200	188
Display Width (mm)	142	142	132	142
Thickness (mm)	18	6	3	5
Weight gm/cm^2 display area	0.9	0.63	1.00	0.31
Brightness (ft-L @ 2.5 watts)	114.5	112	90.4	175
Efficiency (lm/watt)	19	18.6	15	23
Uniformity (%)	±20	±10	±20	±10
Life (hours)	20000	20000	20000	20000

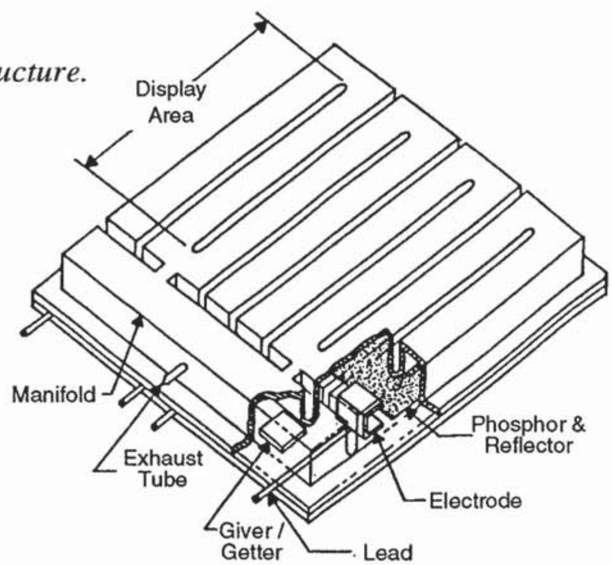


Figure 3-22 *Flat fluorescent lamp structure.*

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Manufacturing Equipment

Some of the characteristics of flat panel display manufacturing equipment are described in this section. For some equipment, such as substrate flatness measuring equipment, the outstanding feature is the similarity to IC manufacturing equipment in terms of equipment function and specifications. On the other hand, other kinds of equipment, like laser deposition, are found only in the flat panel manufacturing line. Even when the equipment function is the same as for IC's, the substrate size is much greater for a flat panel display, on the order of 1-2 ft^2 in area. Then too, the substrate is glass, which is more brittle and more liable to static charge buildup than a silicon wafer. Automation of process equipment is a question at every level, from cassette to cassette transfer of substrates in and out of process equipment, to automated transfer of cassettes from one station to another. Questions of cleanliness and particle generation in the equipment area are an issue only for certain kinds of equipment like plasma-enhanced CVD and orientation film rubbing. Otherwise, the same considerations and level of performance as for semiconductor manufacturing are required.

Substrate Cleaning

4.1

Substrate cleaning is a repetitive process performed in long in-line systems that feed the glass plates one sheet at a time through the process chemicals and rinse stations. Batch-type tank systems can also be used. The kinds of chemicals, rinses, drying and baking methods have been described previously.

SPC (Shimada Riken) is a prominent supplier of substrate cleaning equipment. Equipment for LCD processing includes batch-type substrate cleaning, with ultrasonic agitation at 28KHz, 40KHz, and 850KHz using solvent or water, brush scrubbing, high pressure jet or shower. Hot water drying is available. Post polishing cleaning equipment is also available, with detergent, solvent, and ultrasonics.

Sheet fed, horizontal process equipment is used for developing, etching, and flaking. Flaking consists of removal of photoresist flakes by chemicals and water shower. Water and solvent removal processes make use of an air knife, IR heating, and UV illumination.

4.2 Photoresist Application/Baking

Both passive and active matrix displays make use of photolithographic processing, and the photoresist process equipment is very similar to that used in integrated circuit manufacturing. The exposure systems vary from relatively simple proximity aligners for passive matrix electrode definition to sophisticated step and repeat or mirror projection systems for TFT definition.

Photoresist coating and baking equipment for flat panel manufacturing is available from a number of suppliers, including Dainippon Screen, Chuo Riken, and Hamatech.

4.2.1 SPIN COATING

Photoresist application consists of spin coating, with the appropriate modifications for substrate size and shape. Just a few percent of the photoresist remains on the substrate after coating. Concern about the materials consumption has led to evaluation of roll coating equipment.

4.2.2 ROLL COATING

Experimental roll coating equipment is being developed by Dainippon Screen and Chou Riken. This equipment allows deposition of up to 70% of the dispensed photoresist, but so far, film thickness uniformity is lower than for spin coating.

4.2.3 CONVEYOR OVENS

Dainippon Screen and Chuo Riken manufacture tunnel ovens for soft and hard baking of photoresist. These are either hot plate or infrared heated units that work in tandem with coating, developing, and stripping systems. Complete units may exceed 30 meters in length.

4.3 Photolithography

Photolithography equipment includes proximity, step and repeat, and mirror projection units.

A novel approach to imaging employing a "view camera" type of projector is available from Nippon Seiko K. K. [1]. This is a 1x projection unit, with a large camera resembling a bellows type camera used for professional portrait photography. Mask sizes up to 17" (432mm) can be used on the 26"x26" stage. A mercury arc source is used, and 8µm resolution is currently achieved. Price for this unit is 15 million yen, which is approximately $100,000.

4.3.1 STEPPERS

Step and repeat units are typically used for thin film transistor manufacturing. These units are adapted from semiconductor production equipment, and are available from Nikon and MRS Technology.

The Nikon 1:1 step and repeat system is capable of 3µm isolated lines, and 4µm lines and spaces over large substrates. Alignment accuracy is 0.6µm or better. The model FX-210B can process 35 substrates per hour, and substrates of up to 550x500mm size can be handled. These substrates are large enough for six 10" displays per panel. Fields as large as 100mm can be exposed in one shot. Stitching of patterns is performed with an accuracy of 1.5µm or better. 6" reticles with pellicles are employed, so that the same maskmaking equipment and materials can be used as for IC manufacturing. Reticle storage library capacity is 13 reticles.

Special compensation is made for the glass compaction or shrinkage during TFT processing [2]. The scaling factor for correction of dimensions varies linearly from the center of the glass substrate to the edge. That is, the maximum process temperature of the center of the substrate is slightly higher than the edge, resulting in a linear change in compensation from center to edge. For example, a 20ppm decrease in dimension in the center would decrease by perhaps 0.02ppm for each 1mm distance from the center, resulting in a decrease in dimension of 15.6µm at a point 250mm away from the center. Design rules for TFT linewidths range from 4-10µm, and the overlay tolerance required is about 1/3-1/5 of the linewidth, or ±1.3-±0.8µm. This means that substrate compaction is a very serious problem for lithography.

Two approaches can be used for correcting glass shrinkage. The first compensates by adjusting the step pitch of the stepper. For the example above, when a 100m shot is printed at a distance of 200mm from the center, displacement of the center can be reduced to zero by adjusting the pitch of the stepper. However, errors will still remain at the edge of the pattern. In order to correct these errors, the lens magnification is adjusted, reducing the error due to glass scaling to less than 0.1µm when both methods are used together. Alignment marks on the panel are measured in order to determine the shrinkage and calculate the optimum position of each shot. These marks can be place between the TFT arrays or in the connector areas.

The MRS Technology 5000 Panelprinter is similar in many respects to an IC stepper. It uses a 2X reduction lens with a resolution of 3.0μm or better, critical dimension control to ±10% or better, and depth of focus of 15μm. Substrates of 450x500mm size can be processed at rates of up to 80 substrates per hour. Two 10" displays per panel are possible, depending on layout. Automatic adjustment to substrate size variation is achieved for scale adjustments of up to 100ppm in x and y axes. This allows butting accuracy of 0.75μm and overlay accuracy of 0.5μm or better.

A dual camera optical system with 0.15 numerical aperture lens is used. With dual cameras, 38 reticles can be accommodated, while 19 reticles are stored in the single camera system. Laser interferometry is employed for alignment.

The two camera system consists of a projection lens, mirror, focusing system, g-line illuminator, reticle chuck and reticle changer. Each camera focuses independently to compensate for substrate flatness. After stepping to the exposure location, it is possible to open both shutters simultaneously, exposing a 50mm square. For example, a 400x400mm substrate can be imaged with 64 subfields of 50mm each, enhancing throughput compared to a single lens system.

The laser interferometer controls x-y stage position, and also controls stage rotation to correct yaw.

A 3500 watt high pressure mercury arc lamp is used for each lens, delivering 200 mW/cm^2 of g-line illumination at the image plane, resulting in exposure times of 0.5-1.5 seconds with 1.5μm of positive photoresist.

System stability is achieved using stable optical columns, atmospheric pressure feedback to calibrate projection lens magnification, and substrate compaction correction by reticle chuck alignment. Measured system stability over 20 hours resulted in compensation within 2ppm of the desired value.

4.3.2 MIRROR PROJECTION

The new MPA-2000 unit was described recently [3]. Figure 4-1 shows the optical schematic. Claims include a 480mm field illumination width without stitching, and 160 panel per hour throughput. A pair of concave and convex mirrors and a flat mirror make up the 1:1 projection system. The mask pattern is formed on a curved area which is 20mm wide. The area is 280mm long, and the radius of curvature is 148mm. Photomask and substrate are scanned together to expose the image. Full sized quartz masks are required for this application. Specifications are shown in Table 4-1.

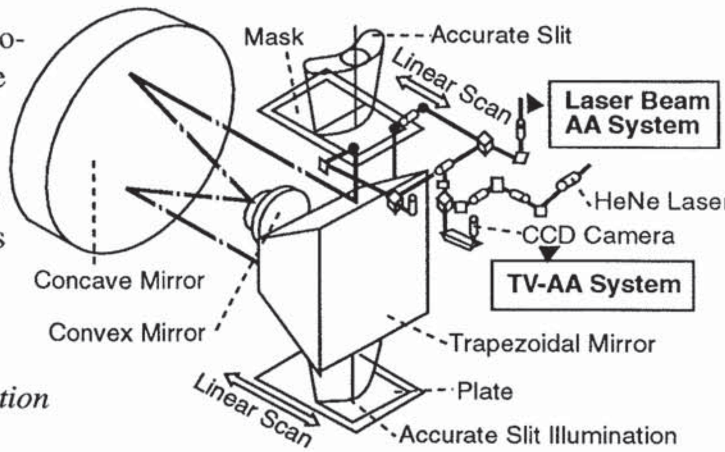


Figure 4-1 *Mirror projection schematic diagram*

Table 4-1 *Canon MPA-2000 Specifications*

Resolution (μm)	3	4	6
Depth of Field (μm)	±20	±30	±40
Slit Width (mm)	9	14	20
Overlay Accuracy	10μm, 3 sigma		

In mirror projection, resolution and exposure time depend on slit width. If the slit is narrowed, higher resolution and longer exposure time will result. For wider slit width, lower resolution and shorter exposure time will result.

Display manufacturers are exposing 2 10" panels on a single 300x400mm plate. With a conventional aligner, four masks are used, and are stitched together, which might cause some inaccurate alignment. But the projection system can expose two 10" panels at once, and doesn't have a stitching problem.

High throughput of 160 panels per hour is achieved because the waiting time for changing masks is not required. This time amounts to 20 seconds, and limits throughput to 80 panels per hour for steppers.

A glass shrinkage rate of 5ppm is typical of thin film deposition, e.g., 1μm per 200mm span. Two alignment marks are measured at a time to align the mask and the plate. The error range on the plate against the mask is measured by magnified compensation marks set at the top and bottom of both the mask and the plate. Both laser alignment and TV camera alignment are used.

4.4 Etching/Stripping

Photoresist developing, etching, and stripping can be performed in continuous process lines available from Dainippon Screen and Chuo Riken. These lines incorporate a post bake step after developing. Where the etching process is well understood, it can be automatically included as the next step in the process track.

4.4.1 WET ETCH EQUIPMENT

Wet etch equipment is therefore usually one module in a process line, in which preceding units develop and bake the photoresist, and subsequent ones strip it off after the etching step.

Batch etching can be used for processing flat panels, but is less common than the continuous track system. Wet etching will be used where possible in flat panel display manufacturing, due to its low cost, and effectiveness in removing particles and contaminants. However, for critical thin film transistor features, dry etching will be employed.

4.4.2 PLASMA ETCHING/ASHING

Dry etching or reactive ion etching equipment is made specifically for LCD applications by Plasma Systems, Plasma Therm, and Tokuda. Fine control of etched figures is one benefit from dry etching, at the expense of throughput and equipment cost. In some cases, it may be possible to combine wet and dry etching, as previously mentioned for ITO patterning. The speed and low cost of wet etching are employed for most of the material removal, while the control of linewidth and profile come from the final, dry etch step.

Tokuda's TPE-700A L/L reactive ion etch system is a cassette/cassette load lock system for etching a-Si, aluminum, molybdenum, tantalum, SiO_2, Si_3N_4, and other films. It is possible to load 12 substrates into the feed cassette, and maximum size is 350x450mm. The etcher can be bulkhead mounted, and beltless substrate feeding is employed.

Tokuda's CDE-700A L/L chemical dry etch system is a cassette to cassette, load lock system for etching a-Si, silicon nitride, polysilicon, and metals such as molybdenum and tantalum. It features a 12 substrate send cassette, 350x450mm substrate size, and end point monitor for a-Si etching.

Nextral, a French subsidiary of Alcatel, has designed a batch RIE system for TFT applications. The stainless steel cathode is covered with a quartz plate to minimize metal contamination. Substrates up to 14"x14" can be accepted. In addition to deposited inorganic films like a-Si, polymer films for tri-level systems can also be etched. System specifications are shown in Table 4-2.

Table 4-2 *Nextral NE550 RIE System Specifications*

Material	Thickness (µm)	Etch Rate (Å/min)	Uniformity (%0)	Throughput (panels/hr)
Amorphous Silicon	0.5	800	±5	6
Silicon Nitride	0.3	500	±3	6
Silicon Dioxide	0.2	500	±3	8
Polymer Film	1.5	1500	±5	3

Table 4-3 summarizes currently available dry etching systems. Where available, price and throughput are noted.

Thin Film Deposition

4.5

Thin film deposition includes sputtering for ITO and metal deposition, chemical vapor deposition, CVD, for polysilicon, and plasma-enhanced CVD, PECVD, for amorphous silicon and silicon nitride. Insulators such as silicon dioxide can be deposited by any of these techniques. Some thin films require thermal treatment and impurity doping. This applies especially to polysilicon, in order to produce films with high mobility and good transistor performance characteristics.

4.5.1 SPUTTERING

Ulvac manufactures in-line sputtering and CVD equipment. Sputtering equipment is available in four substrate sizes, 350x360mm, 450x450mm, 550x600mm, and 650x750mm. Typical systems consist of four chambers; loading, heating, sputtering, and unloading. A full system has the loading station positioned in a clean room, with the rest of the system in a semiclean adjoining room. Total length of the system is about 12 meters. A return conveyor sends substrate holders back to the loading station in the cleanroom. Typical parameters for ITO deposition in

Table 4-3 *Dry Etch Systems*

Firm /Model	Max Substrate Size (mm)	Etch Chambers	Throughput (panel/hr)	Features /Price
Plasma Systems				$300-750K
DES-A125	600	1	10	cassette/cassette
DES-A324	450	1	30	beltless arm
DES-A525	450	2	30	
DES-A725	450	1-4	60	
Anelva				~$1.6M
ILD-4802	700	1	8	
ILD-4803	700	1	20	
ILD-4804	700	2	20	
Tokuda				
TPE-700AL		1	-	through the wall
CDE-700AL		1	-	
TEL				~$1-1.5M
MEA-450SA	450	2	-	dual chamber
MEA-450SR	450	2	-	PE, dry ashing
MEA-450SP	450	2	-	RIE
Thermco Int'l	297x209	1	-	
Ulvac	350	1	-	in-line
Nextral NE550	350	1	6-8	2 panel chamber

a pass-by mode of operation are shown in Table 4-4. A system is also available for horizontal upward sputtering. This method may allow fewer adhering particles.

Leybold Heraeus in-line sputtering systems are available for two sided deposition, continuous operation with substrate heating up to 400°C on substrate areas as large as 900x1500mm. Load-lock introduction of substrate carriers is accomplished in two stages, with the second stage also containing a preheater. The sputtering module also contains an infrared heater positioned between the two panels, and DC magnetron sputtering units are mounted outboard on both sides. Three sputtering cathodes are mounted side by side. These targets measure approximately 19.5"x3.5".

Tokuda's sputtering System 522 is designed for in-line DC magnetron

Table 4-4 *Ulvac SDT-VT In-line Sputtering Systems*

Substrate Size	350x360mm, 450x450mm, 550x600mm, 650x750mm
Sputtering Method	DC magnetron, both sides, pass-by
Film Thickness Uniformity	±5% or better
Deposition Temperature	200°C±15°C (typical)
Throughput	25,000 substrates/month, 2.5 min. cycle, 24 hour/day, 22 days/month
Ultimate Pressure	$5x10^{-6}$ Torr (sputter chamber)
Carrier Transfer	Bottom rack and pinion gears
Main Pump	Turbomolecular

sputter-deposition of metals such as molybdenum, tantalum, chromium, and aluminum. ITO deposition is also possible. Maximum substrate size is 350x450mm, and a 16 sheet substrate loader is available.

4.5.2 CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition of thin films is well developed for IC manufacturing, and the equipment cost and performance are extremely favorable compared to other wafer fab equipment. In contrast, thin film CVD equipment for flat panel manufacturing is expensive and inefficient, compared to other equipment in the manufacturing line. The primary thin film is the semiconductor silicon. Right now, amorphous silicon is the standard material, but polysilicon is also used, and may become even more important in the future. These two kinds of silicon are deposited in different ways.

Other kinds of thin films deposited by CVD include silicon nitride and occasionally silicon dioxide. Plasma-enhanced CVD is standard for silicon nitride, and silicon dioxide can also be deposited by sputtering.

The various methods of deposition for amorphous silicon and polysilicon are described below. Polysilicon can be obtained from amorphous material by a sequence of heat treatments, or a deposited poly-Si source can be used; usually the grain size of deposited poly-Si must be enlarged by thermal processing. Polysilicon can also be deposited by sputtering. Some of the companies making relevant equipment are shown in Table 4-5.

Table 4-5 *CVD Systems and Suppliers*

Thin Film Type	Equipment Supplier
PECVD for Amorphous-Si (20% hydrogen content)	Anelva, Ulvac, Shimadzu, Elletrorava, Nextral
LPCVD, poly-Si	ASM Japan, Leybold/Rytrac
APCVD, poly-Si	Watkins-Johnson
Sputtering, poly-Si	any sputter equipment

The critical process of PECVD for a-Si is described further on. Generally the equipment manufacturer does not guarantee a process. Hydrogen content of the film is determined during deposition and subsequent heat treating; hydrogen content is critical to thin film properties. While polysilicon deposition is well understood from its development for IC applications, the high temperature process, too high for a glass substrate, produces the best transistors. A good low temperature process is required.

Polysilicon films require annealing to enhance grain growth. Performance of TFTs made from polysilicon depend on the number, size and other characteristics of grain boundaries between grains. The carrier mobility of the films is low when the extent of grain boundaries is large compared to the area of single crystal grains. Annealing methods that create large grains produce films with higher mobilities. There are a number of compromises involved in recrystallizing material on either a glass or quartz substrate. Of course, the temperature capability of the substrate is paramount. The high temperature poly-Si deposition techniques for either LPCVD or APCVD require quartz, limiting applications to small displays for video cameras, about 1" on a side, or for projection displays, where 3" LCD shutters are typical. Direct view displays require a low temperature process and a glass substrate. The temperature capability of typical glasses has been discussed in a previous section of the report.

Source material for recrystallized polysilicon includes amorphous silicon deposited by PECVD at low temperatures, 350°C or less. This material contains hydrogen that must be removed by annealing prior to recrystallization. Low temperature CVD of polysilicon is also possible, but control of materials properties is more difficult for low temperature deposition. Sputtering is a potentially low cost, low temperature deposition method, and one example has been mentioned previously.

Recrystallization techniques, already investigated for integrated circuit processing, include the following:

- Rapid Thermal Annealing, focused or unfocused beam (a-Si or poly-Si)

Rapid thermal annealing is a commercial process for annealing of implant damage, and can be applied to recrystallization of a-Si with at least 700°C annealing. In order to reach this temperature yet stay below the strain point of the glass substrate, the annealing must be limited in physical area, and must be very short in time, less than 1 second. Unfocused lamp annealing, used for implant activation in silicon wafers, may not be directly applicable. Instead, some kind of focusing will be required, to limit the physical extent of the high temperature region. Aktis Corporation is researching the applications for lamp annealing in TFT manufacturing.

- Zone Melting Recrystallization (poly-Si)

- Solid State Recrystallization (a-Si or poly-Si)

Solid state recrystallization requires very long times of 5-75 hours at temperatures between 500°C and 625°C. Commercial furnaces are employed.

- Laser Recrystallization (a-Si or poly-Si)

An XeCl excimer laser has been used to recrystallize a-Si films at temperatures as low as 150°C [4]. The films were first raised in temperature to release hydrogen, then lowered in temperature to induce recrystallization. The glass substrate reached a temperature no greater than 200°C at 600nm below the surface during this annealing. Very thin films of 15-120nm were deposited, and complete melting of the films occurred. It may be possible to use laser recrystallization for polysilicon devices at the edge of the display, converting a-Si to poly-Si, then building driver circuits on-board the glass substrate. A commercial system from XMR for annealing has been described by Chu and Chen [5]. This system was used to recrystallize a-si films deposited by PECVD, and poly-Si films deposited by LPCVD. For a-Si material, grain size ranged from 10-90nm, depending on laser energy density. For poly-Si, much larger grains of 200-400nm were obtained.

4.5.3 PLASMA CVD

Anelva is a major supplier of both plasma-enhanced chemical vapor deposition, PECVD, and physical vapor deposition, PVD equipment. In-line vertical both-sided deposition systems have been described recently [6]. These systems have several vacuum chambers connected with gate valves. Degassing is performed in the loading chamber. Heating prior to deposition may be done in a dedicated heating chamber, after which the substrates are moved to the deposition chamber. A sequence of depositions can be performed one after the other without removing the substrates from the system. After deposition processes, trays which hold the substrates are removed and returned to the loading chamber. Three or four substrates, 300x400mm can be loaded onto each side of the tray.

A typical PECVD sequence involves silicon nitride followed by a-Si, then n^+ a-Si. Each material is deposited in a dedicated deposition chamber. The interface between the nitride and the a-Si must be free of any contaminants. In addition, the SiN film is deposited at high temperatures, 300-350°C, and a cooling chamber is usually set up between the SiN and a-Si deposition chambers.

Figure 4-2 shows a schematic of an in-line system for depositing the sequence of thin films mentioned above. Substrates pass through each chamber on racks in a fashion shown in Figure 4-3, a schematic outline of chamber construction for TFT fabrication. Figure 4-4 shows the cross-section of the deposition electrode. Substrates are on both sides of a central heater, usually an infrared heater. The RF electrodes face the substrates on both sides, and reactive gases are introduced through the electrode surfaces. Baffles are placed between the chamber and the pump exhaust port to minimize particle generation during initial pumping.

Figure 4-2 *Example of PECVD system for thin film deposition*

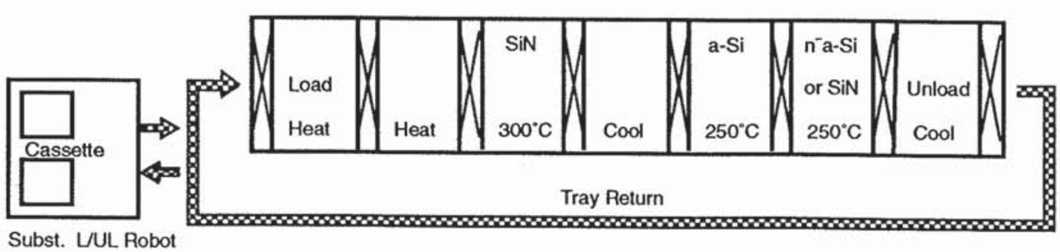
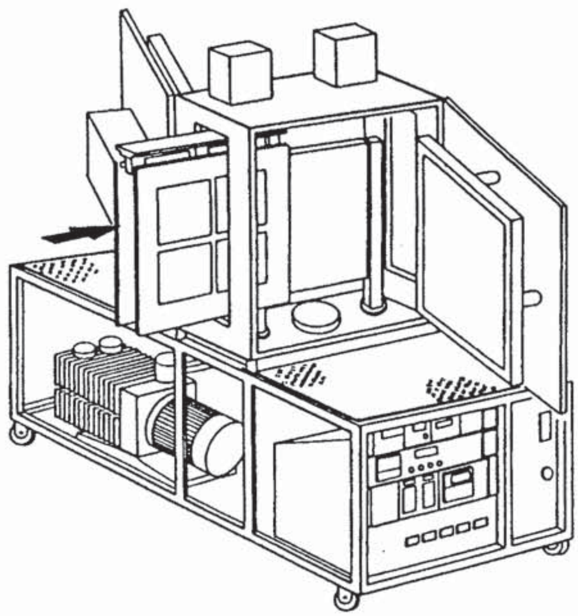


Figure 4-3 *Deposition chamber cutaway schematic*



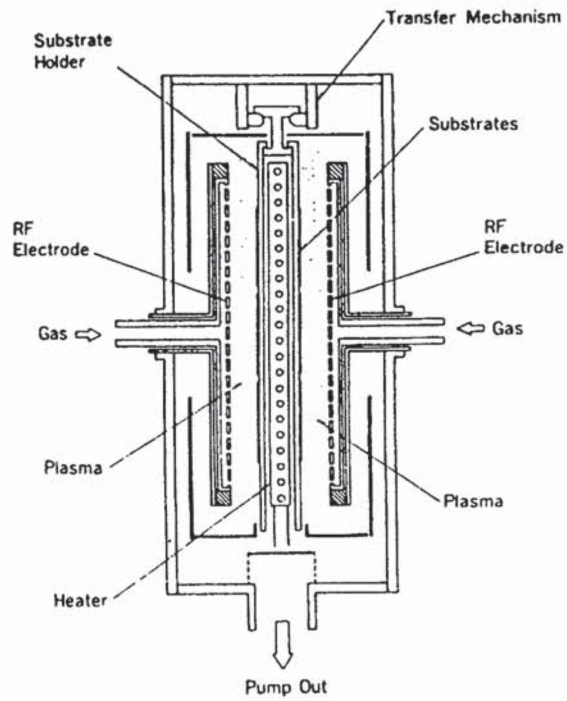


Figure 4-4 *Cross section of PEVD electrode*

Table 4-6 shows the specifications for the various models.

Table 4-6 *Anelva In-Line Plasma CVD Systems (dimensions in millimeters)*

	ILV-9100	ILV-9300	ILV-9300L	ILV-9300E
Chamber Size (HxWxD)	900x800x350	1200x1100x350	-	1200x1450x430
Electrode Size (HxW)	570x570	800x800	800x900	800x1080
Tray Size (HxW)	625x600	920x910	920x1000	930x1200
Deposition Area	450x450	650x650	650x750	650x900

Typical deposition conditions and results are shown in Table 4-7.

Table 4-7 *Amorphous Silicon Deposition*

	ILV 9100	ILV 9300
Deposition Temperature	250°C	300°C
Gas Flow		
SiH_4	200 SCCM	300 SCCM
H_2	800 SCCM	1200 SCCM
Electrode Power	100 W	148 W
Total Pressure	110 Pa	110 Pa
Electrode Gap	45mm	45mm
Deposition Rate	240Å/min	154Å/min
Deposition Uniformity	±20Å/min over substrate	±15Å/min over substrate

Shimadzu, another supplier of plasma CVD equipment, recently introduced a new vertical, dual surface PECVD machine, which can accept eight 300x400mm substrates in a single run. The system includes lower particle generation and deposition than earlier units.

Elettrorava in Italy manufactures a multichamber PECVD unit which allows deposition of multiple films in up to 7 process chambers arrayed around a central isolation chamber which includes a robotic arm for movement of substrates from one chamber to the other. Elettrorava is a Turin, Italy based company with experience in vacuum components and semiconductor deposition systems. The system is designed by MV Systems in Golden, CO, USA. MV Systems is a small company whose founder, Aron Madan, has considerable experience in thin film deposition. Systems have been sold to the University of Utrecht, the Netherlands and to CNRL-Lamel (Italy).

Nextral has developed a PECVD system based on a-Si deposition technology from Solems, the French solar cell manufacturer. The system is designed for process development and pilot production of sequential thin films for TFTs. Substrates up to 14"x14" size can be accommodated. Process specifications are shown in Table 4-8.

Table 4-8 *Nextral ND 400 PECVD System Specifications*

Material	Deposition Rate (Å per minute)	Uniformity (%)	Throughput (panels/hr)
a-Si 0.4μm thick	120	±3	2
Si_3N_4 0.3μm thick	100	±5	2
SiO_2 0.2μm thick	250	±3	4

Applied Materials has announced its entry into the flat panel display equipment business, although an actual product does not yet exist. Their plasma CVD and etch equipment is likely to be a single substrate cluster tool type of arrangement, similar to that used for CVD and etching in some advanced semiconductor processing operations. Equipment is expected to be available at the end of 1992.

4.5.4 LPCVD AND APCVD

Leybold Heraeus provides a low pressure CVD deposition system for polysilicon which can be used in AMLCD applications. This equipment was previously manufactured by Rytrack, Liverpool, UK. A similar system is supplied by ASM Japan. Polysilicon films can be deposited as low as 580°C, while amorphous silicon can be deposited as low as 550°C. (This amorphous material is not suitable for devices in the as-deposited form. It must be recrystallized to produce large grain polysilicon.) The furnace is a hot wall batch type bell jar system that can accommodate 30 substrates per run. Substrate sizes of up to 300mmx300mm can be accommodated. Table 4-9 shows typical process specifications for a-Si and poly-Si films.

Atmospheric CVD allows very high throughput of material, ranging from 3-6 square meters per hour. In one case, a belt furnace design is semicontinuous in operation. Applications for LCD panel manufacturing include SiO_2 deposition systems, and AMCVD deposition of polysilicon on quartz for viewfinder displays.

The silicon dioxide system can coat substrates up to 12.5" wide, and CVD is performed in 3 chambers. Specifications on film properties include ±10% film thickness uniformity, ±10% dopant concentration uniformity, 10MV/cm dielectric film breakdown strength, and particle counts of <0.1/cm² (0.5μm or larger). Table 4-10 shows the relation between belt speed, film thickness, and throughput.

Table 4-9 *LPCVD Silicon Films (Leybold LC350 Reactor)*

	a-Si	poly-Si
Deposition Temperature	570°C	630°C
Growth Rate	25Å/min	50Å/min
Uniformity		
Within Plate (300x300mm)	±5%	±5%
Plate to plate (30 plates)	±5%	±4%
Run to run (10 runs)	±3%	±3%
Throughput	9 plates/hr	8 plates/hr
Film Properties	recrystallizes at low temperature	grain size = 1000Å, no twinning

Table 4-10 *Watkins-Johnson SiO_2 Deposition System*

Belt Speed (inches/min)	Max. Film Thickness (1000Å)	Throughput (m^2/hr)
6	10	2.74
8	7.5	3.66
10	6	4.57
12	5	5.49
14	4.2	6.4

Applications for the high quality oxides produced in this system include glass substrate initial coating, transistor gate oxide, crossover dielectric, and final passivation.

4.5.5 THERMAL PROCESSING

Thermal processing refers to recrystallization of polysilicon by some sort of heating after deposition. If transistors are made from polysilicon, the source and drain regions will probably be implanted, which means another heating step is required to activate the implant, therefore more thermal processing is required. In order to achieve low cost, polysilicon thermal processing should be done on glass, which greatly restricts the possible heating schemes.

Aktis is a California company formed as a joint effort of Peak Systems and Mitsubishi. Peak is a manufacturer of lamp annealing equipment used in IC processing, and Aktis' focus is on application of lamp annealing for polysilicon recrystallization. This kind of annealing is one of the only ways to bring the temperature of the thin film to the melting point without heating the underlying glass. One alternative is an extremely long anneal in a standard furnace to induce solid state recrystallization. Since the latter is a time consuming batch process, lamp annealing is more attractive for its long term productivity potential. Laser annealing, mentioned previously, is also an alternative for recrystallization, at least for selective areas. For example, recrystallization may be restricted to the area around the outside of the display where on-board ICs are fabricated. The as-deposited polysilicon may be good enough for TFT switches at each pixel.

A low thermal budget process for poly-Si TFTs on 7059 glass was described by Liu and Fonash[7]. This process combines several technologies for material processing and low temperature including

- Rapid thermal annealing to obtain recrystallized polysilicon from a-Si:H films. a-Si films were deposited at 250°C. Thickness of the deposited amorphous silicon layer was 2000Å. Polysilicon films were formed by annealing at 650-700°C for 50-5 minutes, with grain size of about 1μm. Source/drain regions had been implanted, and recrystallization also served to activate the implants.

- Magnetron sputtering at 220°C for deposition of the gate oxide from a SiO_2 target. Oxide etch rate was 40Å/sec in dilute HF, comparable to oxides deposited in other ways

- Electron cyclotron resonance generation of hydrogen to passivate the gate oxide. TFTs were passivated at 300°C for 5 or 15 minutes. Total pressure in the system was $1.2x10^{-4}$ Torr, and power was 600W. TFT mobility was found to be in the 60 cm^2/Vs range

4.5.6 ION IMPLANT/DOPING

Polysilicon transistors source and drain regions have to be doped with conventional doping methods, unlike amorphous silicon devices for which the doped layer is deposited by CVD. For small substrates, such as the quartz substrates now being used for projection TV displays, standard IC equipment can be used, including a normal ion implanter. The situation will be quite different if a low temperature polysilicon process is developed for large substrates; standard ion implanters will be difficult to use. Two different approaches have been adopted to large area, high throughput implantation of dopants.

Phased Linear Scanner

The phase linear scanner from Superion is designed to permit ion implantation of large area substrates without the use of a conventional rotating disc substrate holder[8]. Ion implanters for silicon wafer integrated circuit processing make use of batch processing, and wafers are placed on a rotating substrate holder. For large substrates such as 300x400mm glass substrates for liquid crystal displays, the rotating substrate approach is inefficient.

Ion implantation must be accomplished holding the beam fixed, and moving the substrate underneath. If a single substrate is scanned back and forth under the beam, a significant amount of time is required to reverse the scanning direction at each end of the traverse, which limits the productivity of the implanter. The phased linear scanner moves two substrates past the ion beam in a synchronized motion so that one of them is always under the beam, and the dead time due to reversing the scan is accommodated by implantation of the second substrate. The concept can be applied to any number of substrates.

An end station using the phased linear scanner is shown in Figures 4-5 and 4-6, in plan and side view cross-sections. The substrates are supported on two target carriages which are scanned along the track as determined by the position of the followers in the racetrack driver. The carriages are driven by wire drives from pulleys driven by two oscillatory rotary drives, labelled X1 and X2. The scan frequency is in the range 1-3 Hz, that is, 2-6 passes through the beam per second. The end station is only 75mm deep, and can accommodate secondary electron collector plates. An external magnet controls the secondary electron trajectories and an electron flood gun can be installed in order to prevent substrate charging.

A typical implantation requirement might be 1-3x10^{15}/cm^2 of phosphorus ions at 100keV and 5% uniformity, substrate size of 300x400mm, and a maximum temperature rise of 200°C. A 2-substrate system operating at 3Hz would achieve a throughput of 10-20 substrates per hour, assuming the beamline can deliver the required beam current.

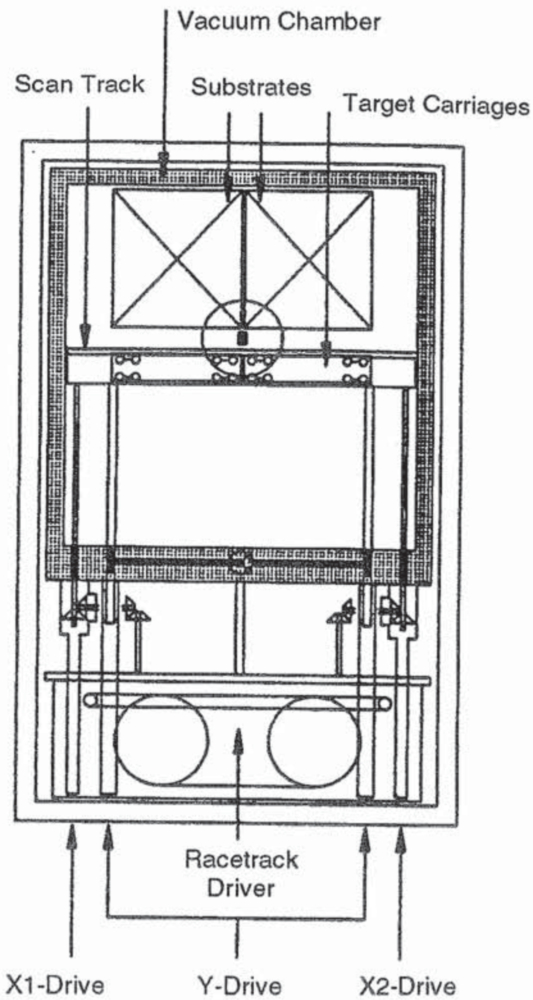


Figure 4-5 *Plan view of phased linear scanner showing two substrates*

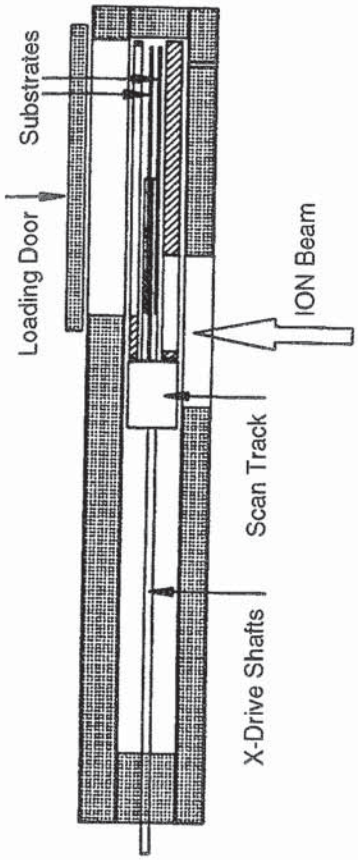


Figure 4-6 *Cross-section view of linear scanner end station*

Ion Flux Doping

Part of the expense of an ion implanter comes from the magnetic focusing to separate ions from each other as they travel toward the substrate. In some cases, isotopes of an element are separated from each other and only one is selected. On the other hand, a non-selective implantation might be used, as long as the ions that hit the substrate contribute to doping, or at least don't interfere with it. Ion flux doping is the way to do this, and is already in industrial use in other industries for the coating of metal parts with wear resistant thin films and other applications.

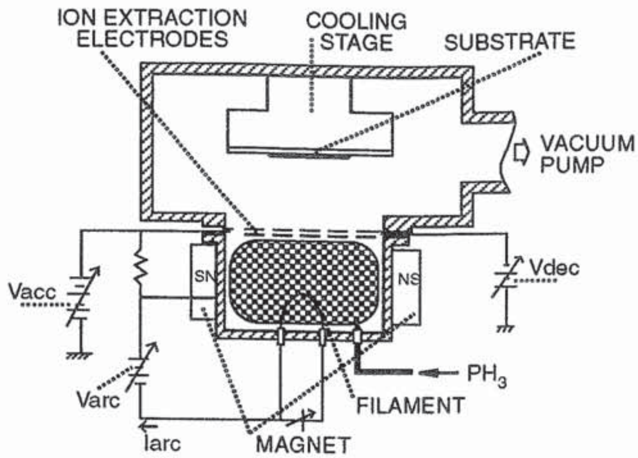
A low temperature poly-Si process combined with ion-flux doping was reported by Asahi Glass[9]. The polysilicon was recrystallized after deposition by CW argon laser scanning at 13.0 m/sec. An average grain size of 30nm was obtained, and mobility was 40 cm^2/Vs.

One difference between TFT fabrication on amorphous and polysilicon materials is in the doping for transistor source and drain formation. N-type doping can be accomplished in the deposition of amorphous silicon, and typically an undoped a-Si layer is followed with the n^+ a-Si layer deposition in sequence in the same in-line PECVD system. Polysilicon needs some kind of recrystallization process, which would diffuse the dopant throughout the layer, so some kind of doping process must be used. Ion implantation of the kind used for IC manufacturing can be used, but less expensive alternatives are attractive. One of these is non-mass-separated ion flux doping, in which gaseous sources are ionized and accelerated onto the substrate.

In the study reported here, the source gas was either pure phosphine, or 5% phosphine in hydrogen. The ion flux was created by a bucket type ion source using RF discharge and a magnetic field. The flux was extracted and accelerated by 2.5-10.0kV onto samples that were neither heated nor cooled. For pure phosphine source gas accelerated at 5.0kV, the phosphorus concentration peak is at 10nm. Sheet resistance of the doped layer is a function of the subsequent annealing temperature. At 300°C, a sheet resistance of $10^4\Omega$/square was obtained for 5kV acceleration. With 10kV acceleration, a higher annealing temperature is required, possibly due to more extensive implantation damage. Functional transistors were obtained, and the highest process temperature for transistor formation, including polysilicon deposition and several annealing operations was less than 450°C.

A bucket ion source for doping polysilicon was described by Kawachi and coworkers at Hitachi[10]. The ion source arrangement consists of a cylindrical plasma chamber, 250 mm diameter. 24 permanent magnets surround the chamber, which contains ion extraction electrodes and a hot filament cathode. Figure 4-7 shows the chamber schematic. The 150mm ion beam was extracted from the arc discharge plasma and irradiated the sample directly, without mass separation. The discharge gas was 1% phosphine, diluted with either hydrogen or helium. Ion acceleration voltage was 500V, and ion current density was varied from 0.125mA/cm^2 to 0.5mA/cm^2.

Figure 4-7 *Ion bucket source and deposition chamber schematic*



A 100mmx100mm sample was irradiated by the ion source, and uniformity of irradiation was ±5% at 0.125mA/cm^2. Activation of implanted samples was performed with a XeCl excimer laser using a fly's eye lens integrator to achieve ±6% uniformity of laser beam intensity over a 8x8mm area. The sheet resistance of doped films was less than 1000Ω/square after an irradiation time of only 10 seconds!

4.6 Test Equipment

Many kinds of testing and test strategies are in use for TFT panel manufacture. These include the common kinds of in-process testing for particles, film thickness, metal resistivity, critical dimension, substrate flatness, and so forth. In general, a modification of equipment designed for making these measurements on silicon wafers is satisfactory. However, there are test requirements that are unique for flat panels, or requirements where a simple modification such as a larger stage for the substrate are not enough. These include automated optical inspection, parametric testing (capacitance testing of circuit and pixel elements), and functional in-process testing. In addition, inspection information must be delivered to a laser repair station, which is also unique to the flat panel industry.

4.6.1 VISUAL AND FUNCTIONAL TEST

Examples of equipment for flat panel display measurement include the Nanometrics critical dimension (CD) equipment, model 210LCW/SP400. Optical inspection systems based on modified optical microscopes include the Olympus MHL100 for up to 450x400mm substrates, soon to include an automatic substrate transfer system. Nikon also supplies macroscopic and microscopic optical inspection systems for flat panels. The macroscopic system is used for visual inspection for particles, scratches, and surface irregularities.

4.6.2 OPTICAL IMAGING

Automatic, high speed imaging and cataloging of defects requires complex hardware and software, originally developed for applications like integrated circuit photomask inspection, and for image processing in satellite photographs. Two types of equipment that have been adapted for flat panel display inspection are described here.

There are many similarities between optical inspection for IC mask or wafer manufacturing and for flat panel displays. However, some key differences exist as well. Common practices for masks and wafers are compared to the flat panel display inspection requirements by Hendricks and Kawamura of KLA Acrotec[11].

For IC mask shops, one function of optical inspection is to serve as a "Pass/Fail Gate". Automated inspection is performed immediately after the last cleaning process and if defects are detected, their coordinates are transferred to a repair station, the mask is repaired, then recleaned. Finally, the mask is re-inspected to verify that all defects have been repaired. The corresponding function at the wafer manufacturer is "Mask Qualification", where optical inspection is used to verify the perfection of incoming mask shipments. These functions are identical for IC masks and reticles for optical steppers.

Many mask shops and wafer fabs use optical inspection for "Engineering Analysis." Many papers on defect source analysis have been presented, in which optical inspection is used to inspect the wafer at different points in the process, to determine where defects are occurring. The object is to identify a faulty process, rather than to identify and correct specific defects on a given wafer.

A companion function of optical inspection is "Process Audit". For this function, optical inspection serves to monitor and compare defect levels, to give early warning of manufacturing problems.

These functions of optical inspection can be applied to flat panel manufacturing as well. For example, a "Pass/Fail Gate" can be established using optical inspection. However, in a photomask, every defect greater than a certain size is a fatal one. This may not be the case for defects on a TFT substrate. The automated inspection routines many be able to distinguish fatal and non-fatal defects. Engineering analysis will be the most important function of optical inspection during the early phase of flat panel manufacturing. For example, to distinguish between a fatal and non-fatal defect for pass/fail inspection, an engineering analysis has to be performed first.

For the initial stages of TFT manufacturing, the inspection methods are similar to those for photomasks, and only the substrate size is different. Later in the process, TFT construction and geometries become very complicated. These patterns closely resemble those on IC wafers, and appropriate inspection technologies can be used.

Optical image processing has been used in non-semiconductor applications, for example in filtering noise from electronic images. For optical image processing, a Fourier-plane filter blocks out repetitive patterns and leaves the non-repeating features. Defect identification should be simple threshold detection of the filtered imaging. Advantages of this method are:

- High inspection speed can be achieved with simple electronics, since the complicated part of the image processing is done by the optical filter.

- Relatively large depth of field can be achieved and it is possible to detect defects with relatively low resolution. This latter benefit may not be too important in TFT array inspection, since design rules are large compared to integrated circuits.

Disadvantages of optical image processing include the following.

- False defects can arise from the use of coherent (laser) illumination. Very small changes in film thickness and refractive indices of thin films will lead to false defect detection.
- It is difficult to distinguish a fatal from a non-fatal defect.

- Because the Fourier transform limits the inspection to repetitive patterns, a border area exists at the edge of the array that cannot be inspected.

- Long term stability of laser intensity may be a problem.

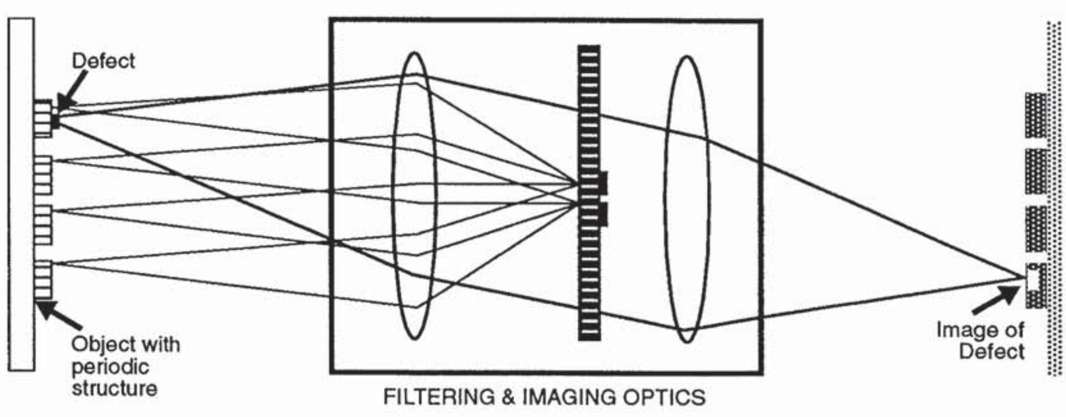
Optical Image Processing Equipment

Inspection of panels using optical image processing was described by Lin and Carroll of Insystems[12]. In optical pattern filtering, collimated, coherent laser light shines on a repetitively patterned substrate. Light reflected from the patterned surface diffracts in specific directions determined by the pattern layout. An objective lens collects the light and produces a pattern of bright spots in its back focal plane. This pattern of bright spots is the "optical Fourier Transform" of the pattern on the substrate. A spatial filter (hologram) placed in the backplane can selectively suppress light corresponding to specific pattern elements. The light which remains can then be imaged or further processed.

If all the repetitive information is suppressed, the spatial filter would have opaque dots corresponding to the bright spots of the optical Fourier Transform. A defect-free substrate would therefore show no image at all, since the diffracted light would be exactly canceled by the spatial filter. Where defects are present on the substrate, diffracted light passes through the filter, and can be imaged either optically or electronically. Typically, a video camera is used. Since the field of view of the camera is small relative to the substrate size, the substrate must be scanned. During the scan, the spatial filter is stationary because the pattern of dots is independent of substrate position. Figure 4-8 shows a conceptual diagram of the method.

The speed and accuracy of inspection of LCD substrates is dependent on the intrinsic noise level of the sensor and other system components. Some intuition

Figure 4-8 *Optical pattern filtering for defect imaging*



about the number, spacing, and size of defects is necessary in order to achieve sensitive detection at high scanning speeds. The practical limit on the coarseness of resolution of the sensor might be taken as twice the expected spacing of the defects. For example, if we expect no more than one defect per 100x100μm area, and wish to know the defect location with a precision of 20μm, the picture elements on the sensor might correspond to 20x20μm area. Such a sensor would have a wide field of view and correspondingly high throughput, up to 400x400cm/sec.

Other factors which reduce this theoretical scanning rate include the irregularities of the substrate, which create a dim residual background noise pattern with a periodicity similar to that of the device pattern. Textured surfaces such as metal patterns exhibit such noise prominently. Other noise sources include scattering and reflection in lens elements of the inspection optics, and diffractive effects in the spatial filter itself. A critical signal to noise ratio of 5 to 7 is needed to distinguish defects from this background noise. For detection of a 1μm sized defect on a substrate, which might be typical of TFT processing, the imager pixel size is about 4x4μm. Assuming that information can be processed at a rate of 10^8 pixels/sec, then the substrate can be scanned at a rate of 16x16cm/sec. This means that a 320x350mm substrate with two 10" TFT panels could be inspected in less than one minute.

Analog image processing employs two inspection heads that scan identical parts of an image in parallel. The output of the two channels is compared by analog electronics. These systems are useful for mask inspection, but not for complex patterns on wafers. The advantage of analog optical inspection is

- High speed inspection can be achieved with simple electronics

Disadvantages include

- Restricted image processing capability
- Analog filtering limits flexibility

Digital image processing takes the output from a camera or other sensor, digitizes it, stores it in memory, and then applies any one of a number of algorithms (procedures) in order to locate the defects. Both the electronics and the algorithms are complicated, and the optical subsystems have to be designed together with the design of the defect detection procedures. This results in a complex, expensive system. Its advantages are

- Flexibility in distinguishing between kinds of defects, fatal vs non-fatal and so forth

- High sensitivity even on complicated images

- Repeatable and predictable defect detection due to the digital nature of the procedures.

Disadvantages include

- A very large engineering effort is required to develop the electronics, algorithms, and optics
- The resulting systems are very expensive

Digital Image Processing Equipment
The KLA Acrotec 6000 series inspection systems employ digital image processing to identify defects on flat panel display during the manufacturing process. The technology is an extension of that used for IC wafer inspection. KLA Acrotec is a joint venture of KLA Instruments (San Jose) and Nippon Mining (Tokyo). The company was founded in October of 1990 with the charter to produce equipment for inspection of flat panel displays.

Panel size of up 500x500mm can be accommodated. The optical system is set up in two modes, for low magnification to locate defects, and high magnification to identify them. The currently available system is a manual load system that inspects the repeating pattern only, and does not locate defects on the periphery of the panel. Table 4-11 shows the operating parameters of the system in the two magnification modes.

4.6.3 ELECTRICAL EVALUATION
Electrical evaluation includes standard measurements of film resistivity and mobility, performed using the same equipment as for semiconductor manufacturing. On the other hand, parametric testing of partially completed TFT panels requires substantial modification of the test procedures used for integrated circuits. Two approaches have been recently reported.

Table 4-11 *KLA Acrotec 6000 Parameters*

	High Magnification	Low Magnification
Objective Lens	8x	4x
Depth of Field	>50μm	>100μm
Pixel Size	3.25μm	6.50μm
Size of Smallest Defect	4μm	7μm
Scan Speed	5cm²/sec	20cm²/sec
Stage Speed	120mm/sec	240mm/sec
Scan Time	140 sec	35 sec

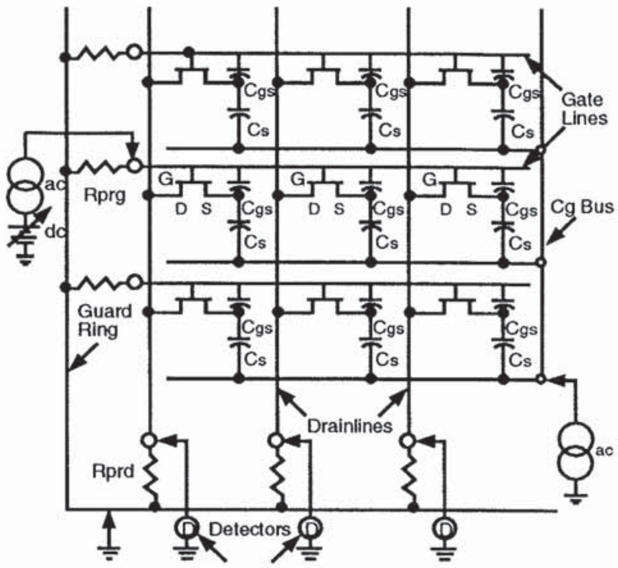
Transfer Admittance

The transfer admittance method has been adapted from other circuit testing applications to TFT arrays, as described by Hall and coworkers at GenRad[13]. An electrical prober makes contact with gate and drain lines. Figure 4-9 shows the test method for the case where storage capacitors are connected together using a separate (common) bus. A combined AC and DC test signal is applied to each gate line, and currents are measured simultaneously by detectors connected to many drain lines. The transfer ratio is admittance whose phase components give conductance, G, and capacitance, C. Conductance and capacitance differences are sensitive measures of faults because they vary only slightly over the area of a panel.

Substrate guard rings are often used to protect the TFTs from high electrostatic voltages during panel manufacture. These rings are removed prior to completing the manufacturing process, but their presence can complicate the electrical measurements performed by the admittance method. Basically, the guard ring must be designed with such testing in mind, as well as the electrostatic protection function.

Most common electrical defects are detectable by this test method. These include most open circuits and shorts, as well as TFTs with high on resistance and leakage of the storage capacitor. Many of these defects can be located and identified as well as simply detected. A typical test setup might employ a probe array to contact all 480 gate lines of a 10" display. A second set of probes would contact 240 of the 1920 drain lines. This second set would be stepped to make the other drain line connections. A defect-free panel could be tested in 3-4 minutes, depending on the number of detectors used. Identifying and recording any faults would require extra measurement time.

Figure 4-9 *Transfer admittance testing*



IBM Test Set

An electrical test system has been built by IBM to test in-process TFT arrays[14]. The set consists of a probe contact assembly to contact the gate and data lines of the active matrix, circuitry to perform the test, and a PC to control test operation and interpret test results. Software control of testing procedures allows the hardware to perform a variety of different tests.

The test circuit can write charge on any cell in the active array, hold the charge on the cell for a predetermined length of time, and then read the charge from the cell and measure it. This sequence of events is called a basic test. By varying the parameters of the test, such as gate pulse height and width, hold time and so on, it is possible to extract the gate threshold voltage, cell charging time constant, cell OFF current, and other cell parameters.

The first step in a single charge test is to stabilize the data voltage at the value desired for the test. At this point the gate voltage is in the off state, switch S1 is open to disconnect the data line from the data voltage source, and switch S2 is closed to reset the integrator to the preselected level. Next, S1 is closed, connecting the data voltage to the data line. The gate voltage is then turned on. At the end of the gate pulse the tester enters a hold time, and during this period the charge that has been transferred to the cell is stored on the cell capacitance. This emulates the display, where charge is stored on the cell capacitance for a frame time. During the hold time the data line is disconnected from the data voltage source by opening switch S1. The data line is then connected only to the inverting input of the operational amplifier, which is used as a virtual ground, and the voltage on the data line must then relax to ground.

After the data line voltage has relaxed to ground, the integrator capacitor (C1) is released from the reset voltage level. The integrator will now begin to integrate the negative of the current into the inverting input of the operational amplifier.

At the end of the hold time, the gate voltage is turned on to connect the cell capacitance to the data line. The gate voltage is held on for several cell discharge time constants to insure that all of the charge on the cell capacitance can return to ground through the operational amplifier input.

After the gate voltage is turned off, the system waits for at least a gate line time constant, and then takes a reading using the analog to digital converter that is connected to the output of the operational amplifier. The difference in voltage between the reset voltage of the integrator V_{ref} and the reading of the analog to digital converter is proportional to the charge that was stored on the cell capacitance ($Q_{cell}=(V_{A/D}-V_{ref})C_1$). The reset voltage of the integrator can be externally adjusted to keep the integrator output voltage within the range of the analog to digital converter.

The output voltage of the integrator can be measured as a function of time during the test. The output voltage shows an initial decrease as the gate voltage is raised to remove the stored charge from the cell. Previously, the output voltage of the integrator had been held constant by the reset circuitry. The increase in the gate voltage is capacitively coupled to the data line by the total capacitance between gate and data line. The thin film transistor is turned on long enough to ensure complete discharging of the cell capacitance to the virtual ground of the operational amplifier. When the gate voltage is turned off, the integrator output voltage shifts, and now represents the charge that had been stored on the cell.

Because the shift in the integrator output voltage depends on the total capacitance, the total capacitance of the cell between gate line and cell can be determined. If there is a discontinuity in the channel of the transistor, the capacitance due to the channel and the source of the transistor will be reduced. This will be seen as a reduction in size of the initial decrease of the integrator output voltage. The test can ensure that crossover and transistor capacitances are correct. It is also possible to determined low resistance between the gate line and the data line or pixel flag. If a low resistance exists, current will flow to the virtual ground of the transistor when the gate line is biased ON, and the current will continue to flow as long as the gate is biased ON, saturating the output of the integrator.

A quick scan through every cell can be made, writing and reading charge in each cell. Cells that do not store enough charge, and cells that store too much charge are marked as suspect cells for detailed analysis using other tests. This constitutes a rapid GO/NOGO test.

Cells that do not store enough charge may have a charge leakage path, which can be checked by using the leakage current test, or the cells may have a transistor which is not providing sufficient ON current. The transistor performance can be tested using the dynamic threshold test and the charging time constant test.

To estimate the value of the dynamic threshold voltage, the data voltage is scanned at fixed gate voltages. The charge transferred to the cell capacitance saturates a certain charge value in each scan. The data voltage at the saturation point determines the threshold voltage of the thin film transistor since the saturation is due to the transistor being cut off. Dynamic threshold voltages of about 3 volts have been observed.

By varying the write gate pulse width, the charge on the cell will saturate at a certain width. This is the minimum gate pulse width that will ensure good image quality. Experimental data indicate a value of 5 microseconds in the tests performed here.

Leakage current can be measured on each cell. The source of leakage current can be the transistor channel, insulating films, or the liquid crystal material. Experimentally, the charge on the cell decreases by about 5% over a frame time of 15ms.

The testing procedure allows only good transistor arrays to continue processing. This can be a significant cost savings. An acceptable defect level is expected to be only 1 in 50,000 cells to 1 in 100,000 cells. It will be impossible to determine whether an array meets this requirement without individual cell testing.

4.6.4 VOLTAGE IMAGING

Photon Dynamics has developed a unique form of testing in which TFT arrays can be electrically addressed, and the voltage patterns imaged visually[15]. This allows both point and line defects to be displayed.

Voltage or capacitance imaging is used, and a two dimensional map of an area under inspection is imaged on a monitor. The inspection equipment configuration, shown in Figure 4-10, includes an electro-optical transducer element which is placed over the TFT array to be sampled. The spacing between the element and sample is a few tens of microns.

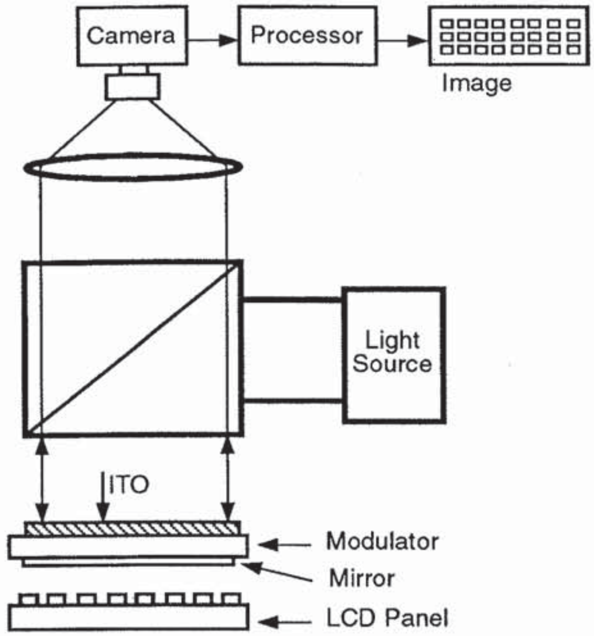


Figure 4-10 *Schematic diagram of voltage imaging of a TFT array*

The transducer is an optically transparent piezoelectric material. The TFT array is electrically addressed by probes at the edges of the display, and the voltages present on the devices are spatially detected by the transducer with a spatial resolution of 30μm and voltage resolution of 100mV. The transducer is modulated with circularly polarized light whose reflected properties are affected by the transducer's detection of TFT voltages.

An image of the substrate is obtained, and false color presentation shows both point and line defects. The transducer is stepped over the panel, and a complete scan can be made in a few minutes. Defective sites are registered in computer memory, and the information can be used to repair defective sites prior to completing the TFT array.

4.7 TFT Repair

Strategies for achieving a high yield in TFT manufacturing include a redundant design, with two transistors per pixel. Repair of transistors is also part of the strategy, and a combination of laser cutting and redundancy is also sometimes used. High yield manufacturing will probably incorporate some kind of redundancy and repair scheme for the near term.

4.7.1 LASER CUTTING

Laser repair can be made on a redundant TFT array[16]. The application described here is for a polysilicon shift register, which is located at the periphery of the display.

A serious problem for AMLCD circuits is defects in the peripheral drive circuits, because they often cause area defects in the displays, while defects in pixel arrays with TFT switches cause point or line defects. Therefore, it is essential to have repair capability on the peripheral drive circuits. Redundant TFT circuits are not sufficient for repairing open defects in the circuits. A laser connection and disconnection scheme was therefore implemented by NEC researchers.

Figure 4-11 shows the redundant shift register blocks, and the laser connection and disconnection methods. The faulty shift registor can be exchanged for a spare by disconnecting the input/output (I/O) lines of the faulty circuit, and connecting the I/O lines of the spare.

Laser repair is made using a pulsed YAG laser, operating at 1.06μm with a pulse duration of 8nsec. Figure 4-12 shows the laser connection and disconnection methods using doped polysilicon as the conduction layer. Several metal layers

Figure 4-11 *Laser connect and disconnect alternatives*

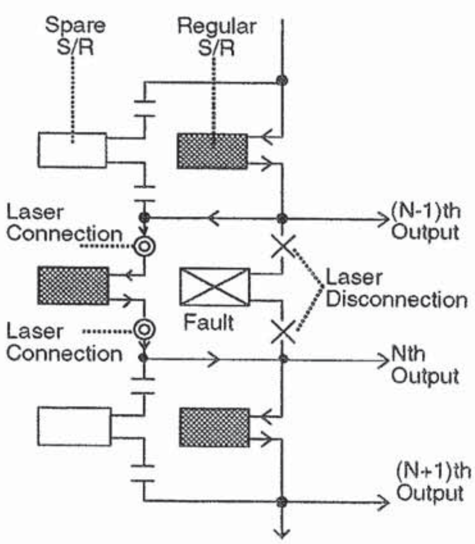
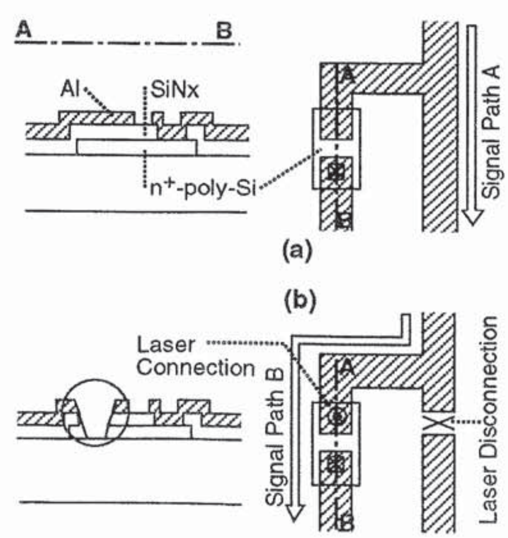


Figure 4-12 *Laser connect and disconnect using polysilicon*



were evaluated for the laser connection method, but these cannot always be applied to the polysilicon TFTs. Laser connections are formed in this method between existing Al(3000Å) and n^+ polysilicon (2000Å) lines. Initially, the Al and poly are separated by silicon nitride. Ohmic contact is made through the SiN_x layer by irradiating with the YAG laser at the overlap site. The illustration shows how the spare line is connected by irradiation. YAG laser pulses of 20-60 W/μm^2 power density are used in an air ambient, and the pattern is 4μmx4μm in size. When the laser irradiation was performed from the front side (Al side), a diode connection was obtained.

To avoid the problems which resulted from the irradiation of the aluminum side, the irradiation was performed through the glass, forming ohmic contacts between the polysilicon and aluminum. No diode behavior was observed, and current passed freely in either direction. The contact resistance was about 100Ω. Through-the-glass repair techniques can be used even on finished displays if the repair has to be made on a drive circuit. The low temperature of the laser connect/ disconnect process is fully compatible with displays where the liquid crystal material has already been introduced into the cell.

4.7.2 LASER-ASSISTED DEPOSITION

The Micrion laser repair system is used to repair both open and short line defects, and to implement redundancy schemes using laser cutting and laser induced deposition[17]. The L-1 system is automated, and compatible with several data transfer protocols from inspection systems. A localized vacuum system enables repairs on 400x400mm substrates without vacuum chamber redesign as substrate size increases. The reaction chamber for deposition maintains a 50μm gap above the substrate, and vacuum is maintained by differential pumping. Substrate position is controlled with an x-y-z stage which moves the defect location under the vacuum chamber.

Visible laser radiation is used for both deposition and cutting. A continuous argon ion laser (514nm) deposits metal and metal oxide lines, while a frequency doubled (530nm) YLF laser provides pulsed energy for material removal. Typical panels are repaired in a 5 minute period, which includes substrate loading, moving to defect locations, imaging the defects, and performing the operator-selected repair.

Laser induced deposition of cobalt lines is a patented process licensed by Micrion from MIT Lincoln Lab. Deposition from cobalt carbonyl gas is enhanced by a photolyic mechanism, and cobalt can be deposited without thermal damage to the substrate on a wide variety of underlying materials, including ITO on glass. Other than surface-absorbed oxygen and carbon, the cobalt is contamination free. Electrical resistivity of the cobalt lines is 20-50 μΩ-cm. The cobalt lines can be deposited at selectable rates of 5-25μm per second (linear rate). Line widths and line heights range from 5-20μm and 0.05-1μm respectively.

Other materials are being investigated for deposition in the system. These include metallic platinum and high resistance cobalt oxide. Platinum deposition of 15-20μΩ-cm lines is achieved (bulk value is 10.6 μΩ-cm). Cobalt oxide can be used as a passivating oxide layer on repaired areas for protection prior to the orientation layer deposition. Resistivities of 10^5 μΩ-cm have been measured.

Another approach to laser deposition has been adopted by Photon Dynamics, which is using palladium metal as the connector. A liquid solution of metal organic is applied by local spray or drop dispense, air dried, and annealed with an argon laser where metal conduction is required. The laser converts the compound to metal, and remaining compound is removed by IPA cleaning.

4.8 Assembly

This section summarizes the equipment available for liquid crystal display assembly. Completed TFT and color filter panels are processed, joined, and filled with the magic liquid crystal material, polarizers are attached, and the completed display is formed by adding a backlight and display driver circuits.

Equipment for flat panel display assembly is often very unlike anything found in IC assembly. For some processes it is adapted from equipment designed for completely unrelated industries, such as food or drug processing. Examples include the equipment for attaching polarizers and other films, and printing equipment adapted for polyimide orientation film deposition.

4.8.1 POLYMER PRINTING

The polyimide orientation film is applied to finished TFT and color filter panels. The film, which is just 300-1000Å thick, is applied primarily by flexographic printing. Polyimide printers are available from Nissha and Hitachi; the Hitachi unit is described below. Cleaning equipment for pre- and post-rubbing is manufactured by SPC.

Figure 4-13 is an outline of Hitachi's thin film coating equipment based on flexo-printing method[18]. The illustration shows a material dispensed from a source tube onto an anilox roll, thickness of coating controlled by a doctor roll, then transferred to a printing plate. The plate can rotate onto the substrate, while the substrate is moved in under the printing cylinder. A comparison of this method to coating by spinner is shown in Table 4-12. Comparison figures include throughput which is higher by a factor of two or three for print coating, consumption of material, which is lower for print coating by a factor of five, and deposition of very thin films, 300Å or so, by print coating. In addition, the authors point out that spin coating is best suited only for round or disc shaped substrates. Square panels such as those for LCD manufacturing can have a buildup of coating in the center of the panel compared to the edges. Print coating can avoid this problem, and can allow large substrate coating. The print coating machine is combined with an automatic loader, multiple chamber drying zone, and unloader to form a semi-automatic coating module.

Rubbing equipment is available from Kyoei Semiconductor. The model L-400 accepts up to 400x400mm substrates, and the following specifications for rubbing apply, Table 4-13.

Figure 4-13 *Polymer printing schematic*

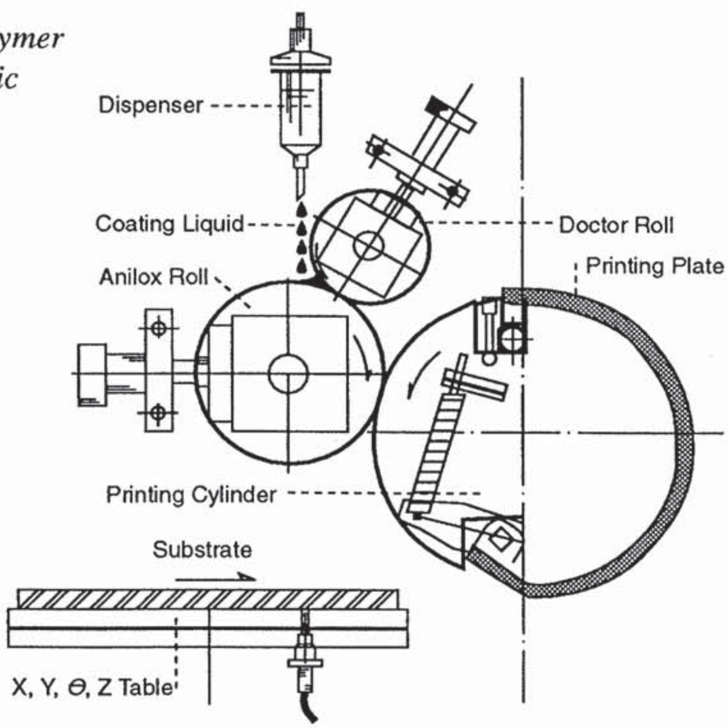


Table 4-12 *Spin Coating vs Print Coating*

	Spin Coat	Print Coat
Throughput	1-2 sheets/min	5-6 sheets/min
Coating Solution Consumption	100%	20%
Substrate Shape	Disc (optimum) diameter	Disc, square, large
Film Thickness	3000Å-a few microns	300Å- a few microns

Post rubbing cleaning equipment serves to remove the charged particles of polyimide, which remain on the panel surface after rubbing. Ultrasonic cleaning with 850KHz, air knife, IR drying and spin drying are available from SPC.

Table 4-13 *L-400 Rubbing Machine*

Substrate Size	400x400mm
Roller Revolution	0-900 RPM
Substrate Stage Travel Speed	0-200mm/sec
Rubbing Pressure	Contact pressure adjusted by setting clearance between roller and substrate, increments of 0.01mm
Rubbing Direction	forward/backward/back and forth
Static Eliminator	prevents static electricity and dust buildup

4.8.2 ASSEMBLY/FINAL TEST

One step prior to assembly is spacer spraying. Spacers are uniformly-sized spheres or rods made of glass and plastic that maintain the cell spacing to the specified value, 5-10μm thick. Equipment for deposition is made by Sekisui, the company that supplies the spacers. Spacer deposition is performed in a spraying operation in which static electricity assists the bonding of the spacers to the substrate. After deposition, spacers are maintained in position for sealing.

Screen printing of the seal epoxy is possible using screen printing equipment from New Long. Alternatively, an automated tube dispense may be preferable for large displays, to avoid the effects of physical contact from the screen surface.

The assembly process and examples of assembly equipment have been discussed in a previous section of the report. Equipment for rubbing, assembly, sealing and curing is manufactured by Kyoei Semiconductor and Ketek. Glass scribers are available from Kawaguchiko Seimitsu, Joyo Engineering, and Villa Precision. The S451A from Kawaguchiko accepts 450x450mm substrates, and is controlled by preselected scribe instructions stored on the control computer's floppy disc.

Villa Precision offers scribers with alignment stages accepting 16" and 24" maximum substrate sizes. Up to 100 scribing programs can be stored in the microprocessor-based electronics control system. Video imaging allows verification of scribe location. Specifications for the 16" (400x400mm) model are shown in Table 4-14.

Table 4-14 *Villa Precision GS 110 16 L Scriber Specifications*

Substrate Size	400x400mm
Cell Thickness	0.29-3mm
Scribes/Substrate	99 lines
Scriber	Tungsten carbide or diamond cutter
Scribing Speed	0-508mm/sec
Resolution of Pitch Feed	25µm
Scribing Accuracy	±50µm

Panels are scribed so that one side of the display (often the front side) is smaller than the other. This is to allow access for attaching the connectors to conducting lines on the inner side of the glass plate. For AMLCD displays, all the electrical connections are made to the rear or TFT glass plate. Scribed glass can be broken by applying pressure to one side of the scribe line, and the amount of pressure determines the rate of break propagation. The lines on one side of a panel can be broken before turning the panel over and breaking the other lines.

Post liquid crystal sealing cleaning is a batch process, performed in a walking beam tank sequence. Recent restrictions on fluorocarbons led SPC to the use of a petrochemical solvent, S-34, together with ultrasonic agitation. The sequence consists of ultrasonic with solvent, IPA rinse, and hot DI dry.

Retardation films are applied at the correct angle to the polarizer by the polarizer supplier, and are made to specification for each customer. For example, Sanritsu uses Suntec machines to apply retardation films. The operation is performed in a clean room. Polarizers are precut, then stacked and loaded onto the Suntec attachment machines where retardation films are added. A Thompson die cutter removes the final 1/16" of material. Polarizers are applied to the finished display using similar machines, which are adaptations of labelling equipment used in other industries.

Final testing includes verifying the performance of the completed display. This may be performed on a display alone, using probe testers from Tokyo Cathode or TEL, or may be done after the die attach process, which allows complete electrical operation. The procedure differs from manufacturer to manufacturer.

LCDs for military avionics require final test procedures that may differ from those for commercial applications[19]. Important parameters for military avionics displays include mechanical electrical, environmental, and optical test. Mechanical tests include dimensional measurements, cell flatness, dimensions and integrity of the contact fingers. Electrical measurements include row and column line impedances and the backplane crossover impedances. Environmental tests include altitude, operating temperature, temperature-humidity, and environmental storage stress tests. Altitude and temperature-humidity tests are spot tested on incoming cells. The environmental stress test is a 6 cycle -40°C-75°C test.

Optical tests measure pixel defect counts, cell brightness uniformity, grey-scale and contrast ratio measurements at different viewing angles, and color tests. Cell brightness at 9 points is measured by a photometer with a 1-cm spot size in ON, OFF, and grey-scale conditions. When brightness nonuniformities are observed, large-area, small-area or periodic measurements are performed, depending on the anomaly. The large area measurement is made by scanning the 1-cm photometer spot across the problem area to detect brightness variations caused by such things as liquid crystal contamination. The small area measurement is conducted with a 1-mm diameter photometer spot scanned across the defect to measure small spot brightness variations, perhaps due to a high spot from a particle. It can also detect brightness variations near the edge of the cell. The periodic measurement is similar to the small area one, and is used to test defects occurring at regular intervals, such as those caused by a stepper.

A pixel is labeled defective if the brightness deviates from the average brightness by 30% in both the ON and OFF conditions. The total number of defective pixels in both ON and OFF conditions are counted and measured against a standard.

Defective pixels next to each other are called clusters. A very small number of clusters are allowed on a panel.

Contrast ratio between the ON and OFF condition are measured at 90°, left-right 55°, and top 45°. The area colorimetries of the center of the cell are measured under conditions of ON, OFF, red, blue, and green. The cell typically has an AR coating on both the cell surface and the front polarizer surface. The specular reflectance of the panel is measured using MIL-C-14806A.

An optical bench is used, with the panel mounted on a stage with a specially designed RGB fluorescent backlight. The stage has two rotational axes with 90° relative motions. The photometer has two translational motions. Pixel defects are measured with a 512x512 CCD black and white camera, analyzing a 50x36 pixel area on the display. The full display measures 6.25"x6.25", with 1024x1024 pixels. Each LC pixel is covered by about 145 CCD pixels in the test, and only signals from the central CCD cells are used for average brightness calculations. Testing of the whole cell is accomplished by mounting the cell on an x-y movement table under the camera and stepping the cell in a serpentine route. At each step, the brightness data of each pixel and its location are calculated and stored in a computer. At the end of the test, maximum, minimum, and average brightness, pixel defect and cluster defect locations are calculated and printed out.

Major cause for cell rejection during the development phase of the program were pixel defect, pixel cluster defect, window frame effect, variations in the grey scale operation, and fill-hole contamination. Pixel defects could be either permanently ON or OFF. Typical causes of these defects were metal bridging or through-insulator shorts. Pixel cluster defects were typically due to metal bridging in the TFT array, color filter damage, or loss of liquid crystal surface alignment in either the TFT array or the color filter.

Measuring brightness in the OFF state was difficult. A slight variation in cell thickness (<0.1μm) could cause a large variation in OFF-state brightness, especially at high temperatures. The window frame effect resulted from a slight increase in cell thickness near the edges of the panel. Trapped particles in the cell with a diameter greater than the cell thickness cause high spots with resulting brightness variations in the OFF state. Localized contamination of the liquid crystal resulted in a localized variation in the cell brightness in the grey scale test. Optical bench equipment for performing tests of this sort is available from Otsuka Electronics and other suppliers.

4.8.3 DIE/PCB ATTACH

Integrated circuits are attached to the flexible circuits described in the previous section. ICs can be bare chips, TAB chips, or even surface-mount devices. The most common arrangement at present is TAB packaging, for which specialized lead attach equipment is employed.

TAB attach equipment is manufactured by Shinkawa and other firms. TAB refers to tape automated bonding, in which the integrated circuit chip is connected to a flexible tape, usually a composite of polyimide support material and copper as an electrical conductor, patterned according to the contacts required to the IC. Two distinct steps are employed, referred to as inner lead bonding and outer lead bonding. Inner lead bonding is the attachment of the IC chip to the tape, and outer lead bonding is the attachment of the tape/IC combination to the PC board or flexible circuit.

In order to apply TAB attach methods, the integrated circuit die must be prepared for attachment by creating raised metal "bumps" where contact to the chip is required. The bumps can be either gold or tin solder. Two types of connecting methods are used for inner lead bonding, attaching the bumped chip to the tape. The first involves melting and reflow of the solder, where solder bumps are employed. A matching area of solder has to be present on the leads of the tape. The upside down (flip chip) is aligned to the substrate, and all joints made simultaneously by solder reflow. Another alternative is pressure contacts. In this case, gold bumps on the chip are glued to the substrate. The shrinkage of the glue causes a compression force on the gold bump and substrate metal pattern.

In some cases, the gang bonding approach for inner lead bonding is giving way to single point bonding, in which the leads are connected rapidly one at a time. For a complex chip with several hundred pins, gang bonding of all the contacts at one time is too difficult, since it is hard to apply pressure evenly around the chip. Single point bonders can attach the leads rapidly, although they require more time than the few seconds for gang bonding. Outer lead bonding is somewhat easier to perform than inner lead attach, since lead pitch is greater, and bonding materials are copper on both sides.

In addition to Shinkawa, TAB bonding equipment is available from Kaigyo Denki, Anarad, and NEC. Single point bonders for TAB are made by Orthodyne and K&S.

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Materials Suppliers

5.1

This section contains a list of suppliers of materials to the flat panel industry. Suppliers are listed alphabetically with indication of product category. Section 6.4 provides a listing of supplier address and phone numbers for reference.

Suppliers' products are organized into the following categories

1. Liquid Crystals
2. Glass Substrates
3. ITO
4. Photoresist
5. Gases/Chemicals
6. Color Filters
7. Photomasks
8. Polarizers
9. Backlight
10. Tab, IC
11. Other

Materials Suppliers	1	2	3	4	5	6	7	8	9	10	11	Remarks
Arisawa								*				
Asahi Glass		*	*									
BKL									*			
Bokusui											*	Carrier,Coater
Brewer Science						*						Color filter materials
Casio										*		
Central Glass		*	*		*							
Chatany Sanyo									*			
Chisso	*											Color filter & orientation film materials
Clean Surface Technology			*				*					
Cookson		*										ITO targets
Copal									*			
Corning Japan		*										
Courtaulds		*										Coated substrates
Dainippon Printing						*	*					
Daisei											*	Seal materials
Dana Enterprises					*			*			*	Spacers
Denshitron											*	Interface board
Densitron									*			
Display Engineering									*			
Displays Inc.											*	Sealants

Materials Suppliers	1	2	3	4	5	6	7	8	9	10	11	Remarks
Enplas									*			
Elix									*			
Endicott Research									*			
Erebamu									*			
Flat Candle									*			
Flex Products		*										Coated films
Foster-Grant								*				
Fuji Rubber											*	Connector
Fuji-Hunt				*		*						
Fujitsu Kasei									*			
Hamlin LCD									*			
Harrison									*			
Hitachi Chemical				*	*					*	*	Printing & conductor matls, topcoat
Hoechst Japan	*			*								
Hoffman LaRoche	*											
Hoya		*	*			*	*					
Irie		*										
JSR				*	*						*	Orient. film, passivation
Kayapola					*							
Kokusai Denki	*											
Komatsu Elec. Metals					*							
Koyo		*										
LCD Lighting									*			
Lamplighter Indus.									*			
Libbey Owens Ford		*	*									
MRC					*							Sputtering Targets
Matsusaki Shinku		*	*									
Merck Japan	*											
Metak Systems									*			
Micro Technology						*				*		
Mikase									*			
Mitsubishi Rayon									*			
Mitsui Mining			*									ITO Targets

1. Liquid Crystals **2.** Glass Substrates **3.** ITO **4.** Photoresists **5.** Gases/Chemicals **6.** Color Filters **7.** Photomasks **8.** Polarizers **9.** Backlight **10.** Tab,IC **11.** Other

Materials Suppliers	1	2	3	4	5	6	7	8	9	10	11	Remarks
Mitsui Toatsu					*						*	Seal Materials
Modutec									*			
Moroboshi Ink						*						
Nagase					*							
Nagase Sanyo											*	Seal Materials
Nihon Denyo									*			
Nihon Shokubai											*	Spacer Materials
Nippon Electric Glass		*										
Nippon Ita Glass		*	*			*						
Nippon Kanko Shikiso											*	2 color system
Nippon Philips										*		
Nippon Polaroid								*				
Nippon Sekiyu Kagaku											*	assembly boards
Nippon Kayaku											*	Seal materials
Nippon Mining			*									
Nissan Kagaku					*							Orientation Film
Nitto Denko		*										
Okaya									*			
Oki										*		
Ono									*			
Plikington		*										
Polytronix					*						*	Sealants
Rayonics									*			
Rodik	*											
Rolm										*		
Sanritz								*				
Sansei Diamond											*	Scribe tools
Sanyo Shinku		*	*									
Shashin Kagaku							*					
Schott		*										
Sekisui Fine											*	Spacers, color
Chemicals												filter material
Shashin Kagaku							*					
ShinEtsu Polymer											*	Interconnect products

1. Liquid Crystals **2.** Glass Substrates **3.** ITO **4.** Photoresists **5.** Gases/Chemicals **6.** Color Filters **7.** Photomasks **8.** Polarizers **9.** Backlight **10.** Tab,IC **11.** Other

Materials Suppliers	1	2	3	4	5	6	7	8	9	10	11	Remarks
Shindo Denshi Kogyo										*		TAB tape
Shinto Chemitron						*						
Shipley				*								
Shokubai Kasei											*	Spacer Materials
Sonocom							*					
Sony Chemical										*		Anisotropic conductor
Stanley Denki									*			
Sumitomo 3M										*		
Sumitomo Bakelite										*	*	Transp. film, orient. film
Sumitomo Chemical				*	*			*			*	Assembly film
Tamara											*	Backlight inverter
Tanaka											*	Conducting pastes
Teijin			*								*	Plastic LCD conduc. film
Teisan					*							
Texas Instruments										*		
3M/Optical Sys.									*			
Tokuyama Soda											*	Silica spacers
Tokyo Cosmos									*			
Tokyo Kagaku					*							
Tokyo Ohka				*							*	Color filter overcoat
Tomoegawa										*		TAB material
Toppan Printing						*	*					
Toray						*				*		
Toshbia Lightec									*	*		
Toshiba										*		
Toshiba Ceramic							*					
Tosoh					*							Sputtering Targets
Toyo Shigyo						*						
Ushio									*			
VMC					*							Sputtering Targets
Viratec		*										Coated substrates
West Denki									*			

1. Liquid Crystals **2.** Glass Substrates **3.** ITO **4.** Photoresists **5.** Gases/Chemicals
6. Color Filters **7.** Photomasks **8.** Polarizers **9.** Backlight **10.** Tab,IC **11.** Other

Materials Supplier Listing 5.2

Materials Supplier Alphabetical Listing
Address, phone, fax, and product type are provided.
Phone number is shown first, then fax number.

ASAHI GLASS CO. LTD.
Chiyoda Bldg. 2-1-2 Marunouchi
Chiyoda-ku, Tokyo 100 Japan
03-3218-5774 03-3213-5486
Glass substrates

BOKUSUI CORP.
1-2-2 Uchisaiwaicho, Chiyoda-ku
Tokyo 100 Japan
03-3506-7604 03-3506-7623
Manufacturers Rep.

BREWER SCIENCE INC.
PO Box GG
Rolla, MO 65401
314-364-0300 314-364-7150
Color filter materials

CASIO KEISANKI
2951-5 Ishikawa-cho Hachioji-shi
Tokyo 192 Japan
0426-44-6113 0426-42-0118
Driver IC

CENTRAL GLASS CO. LTD.
Kowa-Hitotsubashi Bldg
3-7-1 Kanda-Nishikicho
Chiyoda-ku, Tokyo 101 Japan
03-3259-7326 03-3293-2145
Glass substrates

CHISSO CORPORATION
Tokyo Blg.
7-3, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100 Japan
03-3284-8580 03-3215-3692
Liquid crystal materials

CLEAN SURFACE TECHNOLOGY
378 Ohmagari Samukawa-machi
Koza-Gun, Kanagawa-ken 253-01
Japan
81-467-741935 81-467-751131

COOKSON PLASMATERIALS
3223 Crow Canyon Road
Suite 290
San Ramon, CA 94583
510-277-0440 510-277-0469
ITO sputtering targets

CORNING JAPAN
No. 35 Kowa Bldg 14-14 1-chome
Akasaka Minato-ku
Tokyo 107 Japan
03-3586-1053 03-3582-5150
Glass substrates

COURTAULDS PERF. FILMS
21034 Osborne Street
Canoga Park, CA 91304
818-882-5744 818-882-6519
ITO coating service

DANA ENTERPRISES
1440 S. Saratoga-Sunnyvale Rd
San Jose CA 95129
408-257-6686 408-973-9620
Manfacturers Rep.

DENSITRON CORP.
2540 W. 237 St.
Torrance, CA 90505
213-530-3530 213-534-8419
Backlight

DAINIPPON PRINTING
1-1 1-chome Ichigaya Kagacho
Shinjuku-ku
Tokyo 162-01 Japan
03-3266-7211 03-3266-2678
Color filters, photomasks

DISPLAY ENGINEERING
480 Tesconi Circle
Santa Rosa, CA 95401
707-571-8700 707-571-8787
Backlight

ENDICOTT RESEARCH GROUP
PO Box 269
2601 Wayne Street
Endicott, NY 13760
607-754-9187 607-754-9255
Backlight

ENPLAS CORP.
2-30-1 Namiki, Kawaguchi
Saitama 332 Japan
0482-53-3131 0482-57-0191
Backlight

F. HOFFMANN-LA ROCHE LTD.
Bldg 49/325 Postfach
CH-4002
Basel, Switzerland
41-61-688-6468 41-61-691-3856
Liquid crystal material

FLAT CANDLE COMPANY
PO Box 49174
Colorado Springs, CO 80949
719-260-8088 719-260-8089
Backlight

FLEX PRODUCTS INC.
2793 Northpoint Parkway
Santa Rosa, CA 95407-7350
707-525-9200 707-525-7725
Coated flexible substrates

FUJI-HUNT ELECTRONICS
38th Kowa-Bldg 4-12-24 Nishiazabu
Minato-ku, Tokyo 106 Japan
03-3406-6911 03-3498-0567
Photoresist, color filter material

HAMLIN LCD
W7514 CTHV
Lake Mills, WI 53551
414-648-1000 414-648-1001
LCDs, LCD backlight assemblies

HITACHI CHEMICAL CO. LTD.
Shinjuku Mitsui Bldg, 2-1-1
Nishi-shinjuku, Shinjuku-ku
Tokyo 163 Japan
03-3346-3111 03-3346-3475
Anisotropic conductor, orientation

HOECHST JAPAN LTD.
8-10-6 Akasaka, Minato-ku
Tokyo 107 Japan
03-3479-5120 03-3479-4770
Ferroelectric liquid crystal material

HOYA CORP.
2-7-5 Naka-ochiai, Shinjuku-ku
Tokyo 161 Japan
03-3952-1151 03-3952-7854
Photomask blanks, color filters

IRIE KOKEN CO. LTD.
4-11-7 Ginza Chuo-ku
Tokyo 104 Japan
03-3542-4692 03-5565-7064
Vaccuum components for coating

JAPAN SYNTHETIC RUBBER CO
2-11-24, Tsukiji, Chuo-ku
Tokyo 104 Japan
81-3-5565-6600 81-3-5565-6641
Orientation film, photoresist

KOKUSAI DENKI
Dai 100 Seimei Osaka Bldg 4-8
2-chome Minamisenba Chuo-ku
542 Japan
06-271-6771 06-264-7084
Glass substrate

KOMATSU ELECTRONIC METALS
2612 Shinomiya, Hiratsuka,
Kanagawa 254 Japan
0463-23-1301 0463-24-0071
Process chemicals

KOYO LINDBERG LTD.
229 Kabata-cho, Tenri
Nara Prefecture 632 Japan
81-7436-40981 81-7436-40989

LCD LIGHTING INC.
PO Box 3070
11 Cascade Blvd.
Milford, CT 06460-0870
203-876-1520 203-877-7212
Backlight

LAMPLIGHTER INDUSTRIES
96 Lamplighter Street
Oak Hill, WV 25901
304-469-2474 304-469-3380
Backlight

LIBBEY OWENS FORD
(Pilkington subsidiary)
811 Madison Avenue
PO Box 799
Toledo, OH 43695-0799
419-247-3931
Glass substrates

MRC
Route 303
Orangeburg, NY 10962
914-359-4200 914-425-6075
Sputtering targets and equipment

MATSUSAKI SHINKU
45-6 1-chome Ohi Shinagawa-ku
Tokyo 140 Japan
03-3774-6006 03-3771-6005
ITO coated glass

MERCK JAPAN LIMITED
No. 11 Mori Building
6-4, Toranomon 2-chome
Tokyo 105 Japan
03-3591-7884 03-3508-77408
Liquid crystal materials

MICRO TECHNOLOGY
1-33-14 Tomigaya Shibuya-ku
Tokyo 151 Japan
03-3469-1133 03-3469-1557
Color filters, glass TAB

MITSUBISHI KASEI CORP.
Mitsubishi Bldg. 2-5-2 Marunouchi
Chiyoda-ku
Tokyo 100 Japan
03-3283-6451 03-3283-6461

MITSUI MINING CO. LTD.
Mitsui Main Bldg
2-1-1 Nihonbashi
Muromachi, Chuo-ku
Tokyo 103 Japan
03-3241-1339 03-3241-1365
ITO sputtering targets

MITSUI TOATSU CHEMICALS
8F Kasumigaseki Bldg 3-2-5
Kasumigaseki, Chiyoda-ku
Tokyo 100 Japan
03-3592-4715 03-3592-4255
Seal materials

MODUTEC, INC.
920 Candia Road
Manchester, NH 03103
603-669-5121 603-622-2690
Backlight

NAGASE & CO.
5-1 Nihonbashi Kobunecho
Chuo-ku
Tokyo 103 Japan
03-3665-3306 03-3665-3980
Process chemicals

NIHON ITA GLASS
8-1 5-chome Nishi Hashimoto
Sagamihara 229 Japan
0427-74-0920 0427-73-4851
Glass substrates

NIPPON ELECTRIC GLASS
10F Sumitomo Seimei Kita Bldg.
1-14 4-chome Miyahara
Yodogawa-ku 532 Japan
06-399-2711 06-399-2731
Glass substrates

NIPPON MINING
2-10-1 Toranamon Minato-ku
Tokyo 105 Japan
03-3505-8762 03-3505-8691
ITO sputtering targets

NIPPON POLAROID
No. 30 Mori Bldg. 3-2-2 Toranomon
Minato-ku
Tokyo 105 Japan
03-3438-8811 03-3433-3537
Polarizing films

NITTO DENKO CORP.
3F Mori Bldg 31, 5-7-2 Kojimachi
Chiyoda-ku
Tokyo 102 Japan
03-3264-2101 03-3222-4459
Polarizing and retardation films

PHILIPS JAPAN LTD.
Philips Bldg. 2-13-37 Kohnan
Minato-ku
Tokyo 108 Japan
03-3740-5172 03-3740-5190
Driver IC

PILKINGTON MICRONICS LTD.
811 Madison Avenue
PO Box 799
Toledo, OH 43695-0799
419-247-4787 419-247-4912
Glass substrate

SANRITZ
1-30-13, Narimasu
Itabashi-ku
Tokyo 175 Japan
03-3930-1101 03-3930-1167
Polarizing and retardation films

SCHOTT AMERICA
3 Odell Plaza
Yonkers, NY 10701
914-968-8900 914-968-4422
Glass substrate

SEKISUI FINE CHEMICALS
Dojima Kanden Blg.
2-4-4 Nishitemma
Kita-ku, Osaka 530 Japan
Plastic spacers, color filter mater

SHASHIN KAGAKU
436D5 Tatetomita-cho
1-jo Noboru Horikawa-dori
Kamikyo-ku Kyoto 602 Japan
075-432-1152
075-414-1539
Photomasks

SHINETSU POLYMER
Togin Bldg. 1-4-2 Marunouchi
Chiyoda-ku Tokyo 100 Japan
03-3212-4141 03-3212-4144
Interconnect

SHINDO DESHI KOGYO
1027 Washinoya, Shonan-machi,
Higashi Katsushika-gun,
Chiba 270-14 Japan
0425-60-1231 0425-60-7322
TAB tape

SHIPLEY COMPANY
2300 Washington Street
Newton, MA 02162-1440
617-969-5500 617-969-1735
Photoresists

STANLEY ELECTRIC CO. LTD.
1-3-1 Eda Nishi, Midori-ku
Yokohama 225 Japan
81-45-911-1111 81-45-911-0089
Backlight

TEISAN K.K.
1-9-1 Shinonome, Koto-ku
Tokyo 135 Japan
03-3536-2313 03-3536-2341
Process gases

TEXAS INSTRUMENTS
PO Box 655303
MS 8209
Dallas, TX 75265
214-997-3050
Driver ICs

3M OPTICAL SYSTEMS
3M Center
225-4N-14
St. Paul, MN 55144
800-328-7098 612-736-3305
Films for backlighting LCDs

TOKUYAMA SODA CO. LTD.
1-4-5 Nishi-shinbashi
Minato-ku
Tokyo 105 Japan
03-3597-5120 03-3597-5168
Silica spacers

TOKYO OHKA
Shinosaka Marusho Bldg 3-2 4-chome
Nishinakajima Yodogawa-ku
Osaka 532 Japan
06-303-8772
Photoresists, overcoat

TOMOEGAWA PAPER CO. LTD.
5-15 Kyobashi 1-chome
Chuo-ku
Tokyo 104 Japan
81-3-3272-4117 81-3-3274-4739
Adhesive tape for TAB

TOPPAN PRINTING
1101-20 Myohoji-cho, Yokkaichi-shi
Shiga 527 Japan
0748-24-3501 0748-24-3555
Color filters, photomasks

TORAY INDUSTRIES
1-8-1 Mihama, Urayasu
Chiba 279 Japan
0473-50-6041 0473-50-6070
Color filter materials, orientation

TOSHIBA CERAMICS
Shinjuku-Nomura Bldg 26-2
1-chome
Nishi-shinjuku
Shinjuku-ku Tokyo 163 Japan
03-3348-7411 03-3345-8648
Photomask blanks

TOSOH CORP.
1-7-7 Akasaka
Minato-ku
Tokyo 107 Japan
81-3-585-3311 81-3-582-7846
Sputtering targets

TOYO SHIGYO
Nakayoki Matsushige-cho
Itano-gun
Tokushima 771-02 Japan
0886-99-7511 0886-99-6565
Color filter

USHIO ELECTRIC
14-6 5-chome Utsukushigaoka
Midori-ku
Yokohama 225 Japan
045-901-2572 045-901-0883
Backlight

VIRATEC THIN FILMS
2150 Airport Drive
Faribault, MN 55021
507-334-0051 507-334-0059
Coated substrates

5.3 Equipment Suppliers

This section contains a list of suppliers of equipment to the flat panel display industry. The following two sections present suppliers organized to indicate what kind of equipment they supply. In the first section, suppliers of manufacturing equipment are segmented into ten product categories. In the second section, the suppliers of test, inspection and repair equipment are segemented into ten other categories appropriate to that classification. The final section is a listing of company addresses and phone numbers for reference.

5.3.1 MANUFACTURING EQUIPMENT SUPPLIERS

Suppliers' products are organized into the following categories:

1. Lithography
2. CVD
3. Sputter
4. Etch
5. Clean
6. Photoprocessing
7. Asher
8. Ion Implant
9. Assembly
10. Other

Equipment Suppliers	1	2	3	4	5	6	7	8	9	10	Remarks
ASM Japan		*									
Abel				*	*	*					
Advanced Energy										*	power supply
Japan											
Anelva		*	*	*							
Applied Materials		*		*							CVD/etch in 1992
Billco					*						
Bokusui					*				*		alignment film printer, rubbing equip., seal & encapsulation dispenser, spacer disseminator, tester, alinger, LC injection, press, scriber, end seal, polarizer attach equip.
Chuo Riken				*	*	*	*			*	baking oven
Daiko				*	*						
Dainippon Screen	*			*	*	*					
Dainisshoji				*	*						carrier
Daiwa Shinku									*		LC injection equipment
Denko Systems		*									
EHC									*		
Eagle Kogyo										*	bellows sputterer etcher
											electrode shower heads
Elettrorava		*									cluster PECVD
Elionix				*							
Fujioka Seisakusho									*		rubbing equip., screen printer, spacer disseminator substrate aligner, seal drying, US cleaning equip.
General Signal Japan	*										
Hakuto	*					*					
Hamatech					*	*					
Harada Sangyo Kaisha										*	antistatic equipment
Hirayama										*	Autoclave
Hitachi Chemical					*	*			*		anisotropic conductive film thermocompression equipment
Honda Denshi					*						
Hugle Electronics					*					*	non-contact US substrate cleaner

Equipment Suppliers	1	2	3	4	5	6	7	8	9	10	Remarks
Ihara High Pressure Fittings										*	couplings for pipes and valves
Iriye Corp.				*	*						
JBA	*										
JEOL	*	*	*								
Joyo Engineering Lab									*		rubbing, alignment, seal printing, glass scriber, spacer disseminator
Kashiyama Ind.										*	vacuum exhaust equip.
Kawaguchiko Seimitsu									*		
Ketek									*		
Kokusai Electric		*		*							
Koyo Lindberg		*								*	prebake drying equip. for alignment film
Kusumoto Chemicals										*	vacuum oven for drying and foam expelling, heat/ pressure/hardening oven
Kuwata Technical Service					*					*	ultra pure water mfg.equip., waste water treatment equip.
Kyoei Semiconductor	*			*	*	*			*		rubbing equipment
Lapmaster SFT Corp.					*						
Leonix		*	*								
Liquid Concerned										*	electrostatic filter for cleaning fluids, vacuum pump lubricant, processing fluids, cooling water
M Setek					*	*					
MBK Microtech		*			*						excimer laser
MKS Japan										*	vacuum measuremnt, mass flow controller, pressure/flow volume controller
MV Systems		*									cluster PECVD
Mabuchi						*					
Marubeni Hitech Corp.		*									
Mecs										*	substrate transport robot

1. Lithography **2.** CVD **3.** Sputter **4.** Etch **5.** Clean
6. Photoprocessing **7.** Asher **8.** Ion Implant **9.** Assembly **10.** Other

Equipment Suppliers	1	2	3	4	5	6	7	8	9	10	Remarks
Mikasa	*					*					
Mistuboshi Diamond Ind.										*	substrate analyzer, substrate polisher
Mitsui Toatsu										*	waste silane decomposition equip.
Mitsui Trading										*	annealing equip.
Motoyama					*				*		insertion equip., adhesion assembly equip., hardening furnace
Musashi Engineering					*						
Nagase & Co.					*	*	*				
New Long									*		
Newlong Seimitsu									*		automated screen printing
Kogyo											forLCD sealing, rubbing
Nextral		*		*							batch PECVD/Etch
Nikon	*				*					*	reticle stocker, pellicle attach equip.
Nippon Pillar										*	fluorine resin coupler, pump,
Paacking											valve, heat converter
Nippon Plate Glass										*	SiO2 coating equip.
Nippon S. T. Johnson										*	high precision screen printer
Sales Co.											
Nippon Seiko	*										
Nippon Tylan										*	mass flow controller, baking system
Nissha									*		
Nissin Electric								*		*	ion doping, ion shower equip.
Nomura Micro Science										*	ultra pure water mfg. equip.
Ogino Seiki									*		
Okura Electronics				*	*	*					
Optical Radiation	*										
Orion Machinery										*	water cooler, air conditioner
Osaka Shinku Kikai			*								
Plasma System				*							
Plasma-Therm				*							

1. Lithography **2.** CVD **3.** Sputter **4.** Etch **5.** Clean
6. Photoprocessing **7.** Asher **8.** Ion Implant **9.** Assembly **10.** Other

Equipment Suppliers	1	2	3	4	5	6	7	8	9	10	Remarks
Protek					*						
RKC Instrument										*	temperature control unit
Rix Corp.					*						
Rorze Corp.										*	clean robot for vacuum, LCD conveyor system
Rubmaster SFT									*		
Samco International		*		*							
Sanyo Vacuum Indus.			*								
Semicon Created					*						
Semiconductor Energy Research		*									
Shimada Riken Kogyo				*	*	*					
Shimadzu		*	*								
Shin-Etsu Engineering										*	automated plate assembly equip.
Shinko					*					*	antistatic equip.
Shinko Pantec										*	ultra pure water mfg. equip.
Sigma										*	anode oxidation equip., substrate drying equip.
Sonic Fellow					*						
Sonocom									*		dry spacer dissemination equip.
Sumitomo Eaton Nova								*			
Sun-Tec									*		
Tabai Espec									*		fully automated clean curing system
Taiyo Serv. Ctr. (Taitec)										*	heat conversion, cooling water, circulation equip.
Tazmo					*	*					
Tegal				*							
Tokuda			*	*							
Tokuyama Soda					*						
Tokyo Cosmos		*									
Electric											
Tokyo Electron				*							
Tokyo Ohka Kogyo				*		*	*				
Topcon	*										

1. Lithography **2.** CVD **3.** Sputter **4.** Etch **5.** Clean
6. Photoprocessing **7.** Asher **8.** Ion Implant **9.** Assembly **10.** Other

Equipment Suppliers	1	2	3	4	5	6	7	8	9	10	Remarks
Toray							*				
Toshiba Lightec	*								*	*	optical cleaning equip., UV adhesive and hardening equip.
Toto										*	air slide, precision x-y table
Toyoko Kagaku		*		*	*					*	rinser dryer, pipe components
Ulvac Cryogenics		*	*	*				*			cryopump
Ulvac Japan		*	*	*			*	*			
Ulvac Service										*	pure waterstatic electricity control , pure water mfg. equip.
Unit Instr. Japan										*	mass flow controller
Villa Precision									*		
Watkins Johnson		*									
Yamada Corp.										*	teflon pump
Yutaka Engineering										*	gas control equip.,pressure ensor, pressure reduction valve

Test, Inspection & Repair Equipment Suppliers

5.4

Suppliers' products are categorized by the following classifications:

1. Electrical Test
2. Optical Test
3. Electrical Prober
4. Mask Inspection
5. Substrate Inspection
6. Microscope
7. Mask Repair
8. Substrate Repair
9. Burn-in
10. Other

Firm	1	2	3	4	5	6	7	8	9	10	Remarks
Advantest	*										
Astrodesign			*							*	signal genrator
Chuo Riken									*		
Chuo Seiki										*	alignment equipment
Dainippon Screen										*	film thickness measurement
Elionix						*					
GenRad	*										
Hakuto			*	*	*		*	*			

Firm	1	2	3	4	5	6	7	8	9	10	Remarks
Innotech			*							*	LCD probe card
Insystems/JSR					*						
Irie					*						
Japan Hitech										*	microscope heating &
cooling											
JEOL				*	*	*					
KLA/Acrotec					*						
Kusumoto Chemicals									*	*	temp/humidity test
Kyoei Semiconductor		*	*								
Lapmaster SFT				*	*						
Lasertec				*		*					
Lehighton Electron.										*	film resistivity
Leonix				*			*				
MBK Microtech	*	*			*			*			begin sales 1991
Mikasa					*	*					
Minato	*	*	*								
Electronics											
Micrion								*			
Mitsui Trading	*										
Motoyama	*	*				*			*		
Nagase Sanyo					*						
Nakamura Precision	*		*							*	sheet resistance
Nanometrics Japan										*	film thickness, line width
Napson					*						
NEC							*	*			laser repair
Nidek					*	*		*			
Nihon Micronics			*		*						
Nikon				*	*	*					
Nippon Seiko				*	*						
Nippon Shashin Insatsu									*		
Okatani Electric	*										
Olympus						*					
Ono Technology Lab.										*	inspection light source
Orion Machinery										*	environmental testing
Otsuka Electronics		*									final optical inspec.

1. Electrical Test **2.** Optical Test **3.** Electrical Prober **4.** Mask Inspection **5.** Substrate Inspection **6.** Microscope **7.** Mask Repair **8.** Substrate Repair **9.** Burn-In **10.** Other

Firm	1	2	3	4	5	6	7	8	9	10	Remarks
Oyama			*								
Photon Dynamics					*			*			
Rika Kogyo										*	temperature control
Rix					*					*	x-ray inspection
Sankei						*					
Soei Tsushi										*	Autronic LC eval. equip.
Sonic Fellow										*	cleaning
Sononcom										*	spacer particle analyzer
Tabai Espec									*		
Tencor Japan										*	film thickness, particle and defect
Tokyo Cathode Lab	*		*		*			*		*	inspection
Tokyo Denshoku			*					*			
Tokyo Semitsu					*					*	film thickness
Ulvac PHI				*	*					*	panel surface inspection
Ulvac		*			*					*	surface roughness
XMR								*			
Yasunaga					*						
Yokogawa HP	*				*						test systems

Equipment Supplier Listing

5.5

Equipment Supplier Alphabetical Listing
Address, phone, fax, and product type are provided.
Phone number is shown first, then fax number.

ASM JAPAN KK
6-23-1 Nagayama, Tama
Tokyo 206
Japan
81-423-37-6312 81-423-37-6320
Low pressure CVD reactors

ADVANCED ENERGY JAPAN KK
1F, Daishinkyo Bldg. 1-5-8 Fujimi
Chiyoda-ku
Tokyo 102 Japan
81-3222-1311 81-3222-1315
Power supplies

ADVANTEST
Shinjuku NS Blg
4-1 Nishi-shijuku, 2-chome
Shinjuku-ku, Tokyo 163 Japan
81-3342-7500 81-3342-7510
Electrical test systems

ANVELA CORP.
5-8-1 Yotsuya, Fuchu
Tokyo 183 Japan
81-423-34-0220 81-423-60-2277
PECVD, PVD equipment

APPLIED MATERIALS JAPAN
2-7-1 Nishi-shinjuku
Shinjuku-ku
Tokyo 163 Japan
81-3348-3881 81-3348-3442
CVD, etch equip in 1992

BILLCO
Grandview Blvd.
Zelienople, PA 16063 USA
412-452-7390 412-452-0217

BOKUSUI CORP.
1-2-2 Uchisaiwaicho
Chiyoda-ku Tokyo 100 Japan
81-3506-7604 81-3506-7623
Assembly equipment

CHUO RIKEN CO. LTD.
8-5-1 Higashisuna, Koto-ku
Tokyo 136 Japan
81-3646-3511 81-3646-3573
Photo process equipment

DAINIPPON SCREEN MFG. CO.
4 Teranouchi Agaru
Horikawadori, Kamikyo-ku
Kyoto 602 Japan
81-75-414-7128 81-75-431-3410
Photolith., photoprocess, cleaning

DENKO SYSTEMS INC.
6-1 Sakae-cho, Tachikawa
Tokyo 190 Japan
81-425-37-3552 81-425-37-1399
LPCVD

ELIONIX INC.
3-7-6 Motoyokoyama-cho
Hachioji Tokyo 192 Japan
81-426-26-0611 81-426-26-9081
Ion shower

GEN RAD
300 Baker Avenue
Concord, MA 01742 USA
508-369-4400 508-369-6974
TFT electrical parametric testers

GENERAL SIGNAL JAPAN CORP
4-17-13 Kamitoda, Toda
Saitama 335 Japan
81-484-41-1134 81-484-41-1142
Prober

HAKUTO CO. LTD.
1-1-13 Shinjuku
Shinjuku-ku Tokyo 160 Japan
81-3225-8910 81-3354-8608
Mfgr. Rep.

HAMATECH GMBH
Talweg 8
D-7130 Muhlacker-Lomersheim
Germany
49-7041-8 81-0 49-7041-8 8133
Photoprocessing

HARADA SANGYO KAISHA LTD
Tokyo Kajio Bldg. Shinkan
1-2-1 Marunouchi, Chiyoda-ku
Tokyo 100 Japan
81-3213-8391 81-3213-8399
Clean room supplies

HIRAYAMA MFG. CORP.
2-16-16 Yushima, Bunkyo-ku
Tokyo 113 Japan
81-3813-5572 81-3813-5576
Pure water systems

HITACHI CHEMICAL CO. LTD.
Shinjuku Mitsui Bldg.
2-1-1 Nishi-shinjuku
Shinjuku-ku Tokyo 163 Japan
81-3346-3111 81-3346-2836
Polymer printing equip.

HUGLE ELECTRONICS, INC.
4-5-7 Iidabashi, Chiyoda-ku
Tokyo 102 Japan
81-3263-6661 81-3263-6668
Electrostatic discharge control equ

IHARA HIGH PRESSURE FIT.
6-17-20 Shinbashi, Minato-ku
Tokyo 105 Japan
81-3434-3431 81-3434-1480
High pressure valves and fittings

INNOTECH CORP.
6F C. Itoh Bldg. 2-5-1 Kita-Aoyama, Minato-ku Tokyo 107 Japan
81-3297-4400 81-3497-4425
Mfgr. Rep.

IRIE SEISAKUSHO CO. LTD.
4-5-14 Nihonbashi Honcho, Chuo-ku
Tokyo 103 Japan
81-3241-7671 81-3241-7659
Spin drier

JBA (J. BACHUR ASSOC.)
6280 San Ignacio Ave, Suite M
San Jose CA 95119 USA
408-225-0865 408-225-0868
Mask alignment and exposure systems

JEOL LTD.
3-1-2 Musashio, Akishima
Tokyo 196 Japan
81-425-43-1111 81-425-46-3533
Electron microscope, lithography

JAPAN HIGH TECH CO. LTD.
8-6 Shimo-Gofukumachi, Hakata-ku
Fukuoka 812 Japan
81-92-281-7055 81-92-281-7056
Microscope stage

JOYO ENGINEERING LAB. CO.
1-23 Kajigaya, Miyamae-ku
Kawasaki, Kanagawa 213 Japan
81-44-855-0558 81-44-854-6579
Assembly, glass scriber

KLA/ACROTEC
12-1 Fujimi 1-chome
Chiyoda-ku
Tokyo 102 Japan
Substrate defect inspection

KASHIYAMA IND. CO. LTD.
1-32 Koenjiminami
Suginami-ku Tokyo 166 Japan
81-3314-5521 81-3314-5526
Vacuum pumps

KOKUSAI ELECTRIC CO. LTD.
2-3-13 Toranomon, Minato-ku
Tokyo 105 Japan
81-3591-2261 81-3508-2178
Ultrasonic cleaner

KOYO LINDBERG LTD.
229 Kabata-cho, Tenri
Nara Prefecture 632 Japan
81-7436-4-0981 81-7436-4-0989
Clean ovens

KUSUMOTO CHEMICALS CO.
No. 1 Kusumoto Bldg 1-11-13
Uchikanda, Chiyoda-ku
Tokyo 101 Japan
81-3295-8681 81-3233-0217
Temp/humidity chamber

LASERTEC
4-10-4 Tsunashima-higashi
Kohoku-ku Yokohama
Kanagawa 223 Japan
81-45-544-4111 81-45-543-7764
Laser microscope

LEHIGHTON ELECTRONICS
PO Box 328
Lehighton, PA 18235 USA
215-377-5990 215-377-6820
Thin film resistivity, mobility mon

LEYBOLD AG
Siemenstr. 100, PO Box 1145
D-8755 Alzenau, Germany
49-6023-39-0 49-6023-39-3690
Sputter, LPCVD equipment

LIQUID CONCERNED
Dai 6 Chisan Bldg. 4-3-4 Nishi-
Nakajima, Yodogawa-ku
Osaka 532 Japan
81-6-301-0759 81-6-304-5488
Electrostatic filters

M. SETEK CO. LTD.
Daiwa Bldg. 3-6-16 Yanaka
Taito-ku Tokyo 110 Japan
81-3824-3241 81-3824-0939
Mfgr. Rep.

MBK MICROTEK
Ninomiya Bldg 18-4 Sakuraoka-cho
Shibuya-ku
Tokyo 150 Japan
81-3770-6661 81-3770-5360
Mfgr. Rep.

MKS JAPAN
Dai-ichi Shinkoh Bldg 4-28 Yotsuya
Shinjuku-ku
Tokyo 160 Japan
81-3352-5791 81-3352-5790
Vacuum gauges

MARUBENI HYTECH CORP.
3-9 Moriya-cho Kanagawa-ku
Yokohama, Kanagawa 221 Japan
81-45-459-2462 81-45-461-2248
Mfgr. Rep.

MECS CORP.
28 Jono, Kitaima, Bisai
Aichi 494 Japan
81-586-62-4848 81-586-62-3566
Transfer robot

MIKASA CO. LTD.
2-8-1 Shibakouen, Minato-ku
Tokyo 105 Japan
81-3433-8216 81-3433-8229
Photoprocess equip.

MINATO ELECTRONICS INC.
4105 Minamiyamada-cho
Kohoku-ku Yokohama
Kanagawa 223 Japan
81-45-591-5611 81-45-591-5618
Electrical tester

MITSUBOSHI DIAMOND IND.
14-7 Koroen, Settsu
Osaka 566 Japan
81-726-32-5131 81-726-33-9361
Substrate polisher

MITSUI TOATSU CHEMICALS
8F Kasumigaseki Bldg
3-2-5 Kasumigaseki, Chiyoda-ku
Tokyo 100 Japan
81-3592-4715 81-3592-4255
Silane decomposition equip.

MUSASHI ENGINEERING
1-11-6 Iguchi, Mitaka
Tokyo 181 Japan
81-422-33-8111 81-422-33-8177
Liquid dispensing equip.

NEC CORP.
5-7-1 Shiba, Minato-ku
Tokyo 108-01 Japan
81-3798-6116 81-3798-6153
Laser repair

NAGASE & CO.
5-1 Nihonbashi, Kobunecho
Chuo-ku Tokyo 103 Japan
81-3665-3662 81-3665-3950
Mfgr. Rep.

NAKAMURA PRECISION
Kujiraoka No. 1 Bldg 1-16-8 Kameido
Koto-ku Tokyo 136 Japan
81-3684-2548 81-3684-2287
Mfgr. Rep.

NANOMETRICS JAPAN
34 Shin-izumi, Narita
Chiba 286 Japan
81-476-36-1831 81-476-36-1866
Film thickness & CD measurement

NAPSON CORP.
2-2-11 Kameido, Koto-ku
Tokyo 136 Japan
81-3636-0286 81-3636-0976
Resistivity monitor

NIDEK CO. LTD.
34-14 Maehama, Hiroishi-cho
Gamagori Aichi 443 Japan
81-533-67-6611 81-533-67-6650
Inspection microscopes

NIHON MICRONICS
6-8 2-chome Hon-machi
Kichijoji, Musashino-shi 180 Japan
81-422-21-0155 81-422-21-0141
Probers

NIKON CORP.
Fuji Bldg 3-2-3 Marunouchi
Chiyoda-ku, Tokyo 100 Japan
81-3214-5311 81-3214-2836
Steppers

NIPPON PILLAR PACKING CO.
2-11-48 Nonakaminami, Yodogawa-ku
Osaka 532 Japan
81-6305-1941 81-6305-0606
Pumps, heat exchangers

NIPPON SEIKO
Nissei Bldg 1-6-2 Ohsaki
Shinagawa-ku Tokyo 141 Japan
81-3779-7218 81-3779-7432
Projection exposure system

NIPPON SEIKO
Nissei Bldg, 1-6-3 Ohsaki
Shinagawa-ku, Tokyo 141 Japan
81-3-779-7218 81-3-779-7432
Pattern inspection system

NIPPON TYLAN CORP.
4-29-15 Kamiogi, Suginami-ku
Tokyo 167 Japan
81-3395-9141 81-3397-1015
Mass flow controller

NISSIN ELECTRIC CO. LTD.
47 Umezu Takase-cho, Ukyo-ku
Kyoto 615 Japan
81-75-922-4611 81-75-922-4615
Ion shower

NOMURA MICRO SCIENCE CO.
1697-1 Okada Nishinomae, Atsugi
Kanagawa 243 Japan
81-462-28-3944 81-462-28-3506
Pure water systems

OLYMPUS OPTICAL CO. LTD.
San-Ei Bldg 1-22-2 Nishi-shinjuku
Shinjuku-ku
Tokyo 163-91 Japan
81-3340-2181 81-3346-8380
Microscopes

OPTICAL RADIATION CORP.
1300 Optical Drive
Asusa, CA 91702 USA
818-969-3344 818-969-3681
UV exposure systems

ORION MACHINERY
3-35-15 Kamiikebukuro, Toshima-ku
Tokyo 170 Japan
81-3576-6117 81-3576-6359
Water cooler, air conditioner

OTSUKA ELECTRONICS CO.
3-26-3 Shodai-Tajika, Hirakata
Osaka 573 Japan
81-720-55-8550 81-720-55-8557
Optical final inspection

OYAMA CO.
Koshiyama Bldg 1-15-2 Minamiaoyama
Minato-ku Tokyo 107 Japan
81-3403-0771 81-3403-0813
Prober

PHOTON DYNAMICS
641 River Oaks Parkway
San Jose, CA 95134 USA
408-433-3922 408-433-3925
TFT inspection and repair

PLASMA SYSTEM CORP.
992 Yaho, Kunitachi
Tokyo 186 Japan
81-425-74-2111 81-425-74-2112
Plasma etching equipment

RKC INSTRUMENTS
5-16-6 Kugahara, Ohta-ku
Tokyo 146 Japan
81-3751-8111 81-3754-3316
Temperature control

RORZE CORP.
1118 Nishichujo, Kannabe-cho
Fukayasu-gun
Hiroshima 720-23 Japan
81-849-67-1955 81-849-67-1956
Robot, conveyor system

SPC ELECTRONICS
2-1-3, shibasaki, Chofu-shi
Tokyo 182 Japan
81-424-81-8518 81-424-81-9696
Substrate cleaning equipment

SAMCO INTERNATIONAL
33 Tanakamiya-cho Takeda
Fushimi-ku
Kyoto 612 Japan
81-75-621-7841 81-75-621-0936
Plasma CVD, RIE, ashing systems

SANKEI CO. LTD.
2-25-7 Yushima, Bunkyo-ku
Tokyo 113 Japan
81-3839-7354 81-3839-7359
Slicing equipment

SEMICON CREATED CORP.
Yamato Bldg 5-1-6 Ueno, Taito-ku
Tokyo 110 Japan
81-3831-4117 81-3836-9390
Carrier transfer

SHIMADA RIKEN KOGYO
see SPC Electronics

SHIMADZU CORP.
1 Nishinokyo-Kuwabaracho
Nakagyo-ku Kyoto 604 Japan
81-75-823-1111 81-75-811-3188
Plasma CVD system

SHINKO CO.
5-8-84 Minamiokajima, Taisho-ku
Osaka 551 Japan
81-6552-3170 81-6552-3371
Antistatic equipment

SIGMA CORP.
45-2 Shimoasao, Asao-ku
Kawasaki, Kanagawa 215 Japan
81-44-987-9381 81-44-987-1417
Metal etch system

SOEI TSUSHO CO.
2-7 Bakuro-machi 4-chome
Chuo-ku Osaka 541 Japan
81-6-262-0710 81-6-262-0709
Mfgr. Rep.

SONIC FELLOW CO.
3039-15 Tana, Sagamihara
Kanagawa 229 Japan
81-427-63-2300 81-427-63-2305
Cleaning equipment

SUMITOMO EATON NOVA CORP
10F Mita 43 Mori Bldg 3-13-16 Mita
Minato-ku Tokyo 108 Japan
81-3452-9022 81-3452-9025
Ion implanter

TABAI ESPEC CORP.
3-5-6 Tenjinbashi, Kita-ku
Osaka 530 Japan
81-6358-4741 81-6358-5500
Curing system

TAITEC CORP.
2693-1 Nishikata-Kamite
Koshigaya, Saitama 343 Japan
81-489-88-3267 81-489-88-8350
Cooling pump

TAZMO CO. LTD.
6186 Kinoko-cho, Ibara
Okayama 715 Japan
81-866-62-0923 81-866-63-1944
Clean transfer modules

TEGAL JAPAN
Tamahan Bldg 1-1 Kugenuma, Higashi
Fujisawa, Kanagawa 251 Japan
81-466-27-7351 81-466-22-5982
RIE system

TENCOR INSTRUMENTS JAPAN
35-4 Ibukino Midori-ku
Yokohama-shi Kanagawa 227 Japan
81-45-985-7500 81-45-983-7234
Particle and flatness testers

TOKUDA SEISAKUSHO CO. LTD
6-25-22 Sagamigaoka, Zama,
Kanagawa 228 Japan
81-3783-2301 81-3783-5507
RIE systems

TOKUYAMA SODA CO.
1-4-5 Nishi-shinbashi, Minato-ku
Tokyo 105 Japan
81-3597-5120 81-3597-5168
IPA cleaning

TOKYO CATHODE LAB.
1-10-14 Itabashi, Itabashi-ku
Tokyo 173 Japan
81-3962-8311 81-3962-8316
Probers, probe cards

TOKYO ELECTRON LTD.
2-3-1 Nishi-Shinjuku, Shinjuku-ku
Tokyo 163 Japan
81-3340-8111 81-3340-8400
Etcher, inspection

TOKYO OHKA KOGYO CO. LTD.
1-403 Kosugi-cho Nakahara-ku
Kawasaki 211 Japan
81-44-722-7191 81-44-733-7948
Photo processing

TOKYO SEIMITSU CO. LTD.
9-7-1 Shimorenjaku, Mitaka
Tokyo 181 Japan
81-422-48-1011 81-422-42-3816
Flatness testers

TOPCON CORP.
75-1 Hasunuma-cho, Itabashi-ku
Tokyo 174Japan
81-3966-3141 81-3965-6821
Radiometer

TORAY INDUSTRIES
1-8-1 Mihama, Urayasu
Chiba 279 Japan
81-473-50-6041 81-473-50-6070
Asher

TOTO LTD.
1-1-28 Toranomon, Minato-ku
Tokyo 105 Japan
81-3595-9415 81-3595-9400
X-Y table

TOYOKO KAGAKU CO. LTD.
370 Ichinotsubo,Nakahara-ku
Kawasaki, Kanagawa 211 Japan
81-44-422-0151 81-44-433-5332
Rinser dryer, clean fittings

ULVAC CRYOGENICS, INC.
1222-1 Yabata, Chigasaki
Kanagawa 253 Japan
81-467-85-0303 81-467-85-9356
Cryopump

ULVAC JAPAN
Hattori Bldg. 1-10-3 Kyobashi
Chuo-ku Tokyo 104 Japan
81-3535-6381 81-3535-2569
Vacuum components, surface profiler

ULVAC PHI
2500 Hagisono, Shigasaki-city
Kanagawa 253 Japan
81-467-85-6522 81-467-85-4411
Evaluation equipment

ULVAC SERVICE CORP.
9F Hattori Bldg 1-10-3 Kyobashi
Chuo-ku Tokyo 104 Japan
81-3567-4431 81-3567-4434
Antistatic system for pure water

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