

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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NICHIA CORPORATION,

Petitioner,

v.

DOCUMENT SECURITY SYSTEMS, INC.,

Patent Owner.

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Case IPR2018-00965  
Patent 7,919,787

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**PATENT OWNER'S PRELIMINARY RESPONSE**

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## IPR2018-00965 Patent Owner's Preliminary Response

Pursuant to 37 C.F.R. § 42.107, Patent Owner Document Security Systems, Inc. (“DSS” or “Patent Owner”) files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review (“IPR”) of U.S. Patent No. 7,919,787 (the “’787 patent”), claims 1-14, as requested by Nichia Corporation (“Petitioner”) should be denied.<sup>1</sup>

### I. INTRODUCTION

To obtain institution of a challenge presented in the Petition, the Board’s Rules require Petitioner to show that the challenge demonstrates a reasonable likelihood of success. The Board’s Rules also require an evaluation of all such challenges on a ground-by-ground and claim-by-claim basis. Because *SAS Institute Inc. v. Iancu*, 584 U.S. \_\_\_, 138 S. Ct. 1348 (2018), requires a binary institution decision, if **any** challenge in the Petition is deficient, there can be no institution of the entire Petition. Nichia’s Petition includes numerous deficient challenges, both against all grounds and claims in those grounds, which should result in no institution of an IPR against the ’787 patent.

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<sup>1</sup> By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file “a response to the petition addressing any ground for unpatentability not already denied” should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

The '787 patent, entitled "Semiconductor Device Incorporating with a Light Emitting Semiconductor Die," discloses a semiconductor device having a semiconductor die arranged on a packaging device. The packaging device includes a substrate having opposed major surfaces and interconnecting elements arranged on at least one sidewall of the substrate. A first interconnecting element connects a bonding pad arranged on a first major surface of the substrate with a connecting pad arranged on the other major surface (a second major surface) of the substrate. The second interconnecting element connects another bonding pad arranged on the first major surface of the substrate with another connecting pad arranged on the second major surface of the substrate. A semiconductor die is arranged on the packaging device, and more specifically on the bonding pads of the substrate.

To avoid use of a bonding wire linking the semiconductor die with a bonding pad, the semiconductor die has both an anode and a cathode on a bottom major surface of the semiconductor die, where the bottom major surface is *also* a bottom surface of a substrate of the semiconductor die. The anode and cathode are respectively connected to the conductive bonding pads on the first major surface of the substrate. The bonding pads are respectively connected to connecting pads arranged on a second major surface of the substrate via the interconnecting elements.

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