## Outdoor Exposure Guide

### for the Kodak Senior Six-16 with the Kodak Anastigmat Lens *f*.6.3

| Subject | Stop Opening | Shutter Speed |
|---|---|---|
| Nearby landscapes showing little or no sky. Nearby subjects in open field, park or garden. Street scenes. | *f*.11 | 1/25 |
| Ordinary landscapes showing sky, with a principal object in the foreground. | *f*.16 | 1/25 |
| Marine and beach scenes. Distant landscapes. Snow scenes without prominent dark objects in the foreground. Mountains. | *f*.22 | 1/25 |
| Portraits in the open shade, not under trees or the roof of a porch. Shaded nearby scenes. | *f*.6.3 | 1/25 |
| Narrow and slightly shaded streets. | *f*.8 | 1/25 |
| Moving objects. When photographing a moving object such as a runner, train or an automobile, the subject should be moving towards or away from the camera at an angle of about 45 degrees. | *f*.6.3 | 1/100 |

Exposures are for the hours from one hour after sunrise until one hour before sunset on days when the sun is shining. If pictures are made earlier or later, or if it is a *slightly* cloudy or hazy day, use a larger stop opening. This table is for Kodak Verichrome, Super Sensitive Panchromatic and Panatomic Films; if using Kodak N. C. Film, exposures can be made from 2½ hours after sunrise until 2½ hours before sunset.

Kodak Super Sensitive Panchromatic Film is about fifty per cent faster with morning or afternoon light than Kodak Verichrome Film.

The largest stop opening is *f*.6.3. The *higher* the number the *smaller* the opening.

*Picture taking with the*

# Kodak Senior Six-16

**Kodak Anastigmat Lens *f*.6.3**


EASTMAN KODAK COMPANY
Rochester, New York, U. S. A.

# SERVICE DEPARTMENT

ADDITIONAL ASSISTANCE FOR MAKING BETTER PICTURES

ALTHOUGH we give in this manual the essential directions for using the camera it accompanies, there are amateurs who wish for further knowledge of photography.

The Service Department is at their service, *your* service.

Do not hesitate to call on us for information on any photographic subject.

*We are at your service, write to us—there is no charge, no obligation.*

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SERVICE DEPARTMENT

EASTMAN KODAK COMPANY

ROCHESTER, N. Y.

*Picture taking with the*

# Kodak Senior Six-16

**Kodak Anastigmat Lens *f*.6.3**

*Published by*
EASTMAN KODAK COMPANY
ROCHESTER, N. Y. U. S. A.

## THE CAMERA


1. Lock for Back
2. Button for Opening Front
3. Bed
4. Vertical Support
5. Horizontal Support
6. Shutter
7. Lens
8. Optical Direct View Finder
9. Tripod Socket Screws
10. Release for Closing Front
11. Winding Knob

A—Speed Indicator
B—Stop Opening Lever
C—Exposure Lever
D—Exposure Button
E—Focus Pointer

## IMPORTANT

BEFORE loading your Kodak with film, and before taking any pictures with it, read these instructions carefully. Take especial care to learn how to operate the shutter, see page 9.

While loading and unloading, be very careful to keep the protective paper wound tightly around the film to prevent light striking it. The Kodak can be loaded or unloaded in daylight. This should be done in a subdued light, *not* in direct sunlight.

## TO LOAD

Use film number:

**V 616, SS 616, F 616,** or **616** for the Kodak Senior Six-16.

Push the button of the lock towards the arrow.

Open the back.

Lift up the spool holder in the recess adjoining the hinge of the back and place the roll of film in it, springing out the flanges until the pins engage the holes in the spool. Make sure that the word "TOP" on the paper is on the side opposite the winding knob.





Remove the paper band and pass the protective paper *over* the two rollers. Thread the paper through the *longer* slit in the empty reel, *as far as it will go.*

Turn the winding knob once or twice to bind the paper on the reel, and be sure that the paper is started straight.

Close the back, pressing it so that the spring lock snaps into place, securely fastening the back.

Push back the slide that covers the red window on the back of the Kodak. This slide prevents fogging the film.

Turn the winding knob, watching the red window. After a few turns, a warning hand will appear; then turn slowly until the figure 1 is in the center of the window.

Push the slide over the red window. The window should be uncovered only when winding the film.

The film is now in position for the first exposure. After each exposure wind the film to the next number. This prevents making two pictures on the same section of film.





## Opening the Front

Press the button 2, page 2, to open the Kodak; then draw down the bed until it locks. This brings the lens and shutter into position.

## To Focus

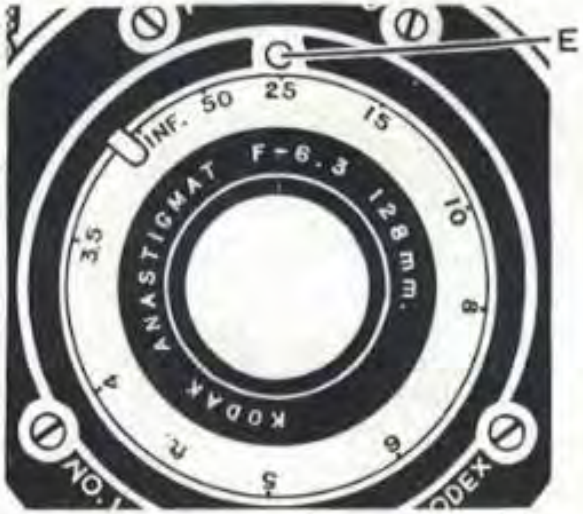
The various distances at which the Kodak may be focused are engraved on the beveled edge of the lens mount.

The scale is marked for 3.5, 4, 5, 6, 8, 10, 15, 25, 50 feet, and INF. (infinity).

To focus the Kodak, revolve the lens mount by turning it to the right or left until the figure representing the distance *from the subject to lens* is under the pointer E at the top of the lens, see diagram, page 8.

When facing the Kodak, turn the lens mount to the right for distant graduations on the scale, and turn to

the left when focusing on nearby or close subjects.




The distance between the subject and Kodak can be estimated without measuring, when the subject is *beyond fifteen feet;* for instance, if the focus is set at 25 feet (the usual distance for ordinary street scenes) the sharpest part of the picture will be the objects at that distance from the camera, but everything from about 18 to about 45 feet will be in good focus.

For ordinary street pictures the focus may be kept at 25 feet, but where the *principal object* is nearer or farther

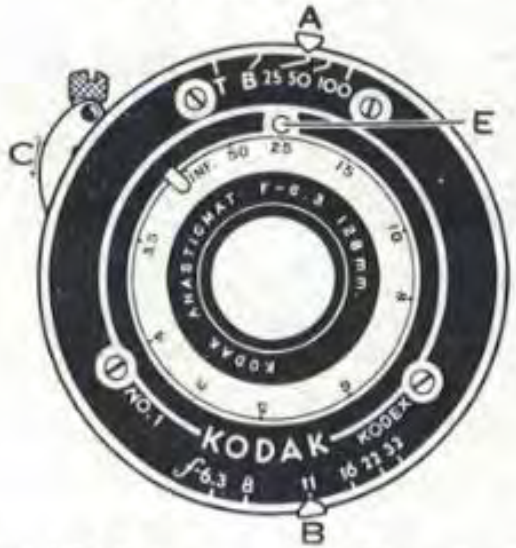




away, the focus should be changed accordingly.

For *distant* views turn the lens mount to INF. (infinity). Nothing nearer than 3½ feet can be focused without using a Kodak Portrait Attachment, see pages 31 and 32, or a small stop opening, see page 14.

## THE SHUTTER




A—Speed Indicator C—Exposure Lever
B—Stop Opening Lever E—Focus Pointer

### Instantaneous Exposures

Move indicator A to 25, 50, or 100 (see Exposure Guide on back cover or table on pages 12 and 13).

Move lever B to the correct stop opening. See Exposure Guide on back cover or table on pages 12 and 13.

Press button D on the side of the Kodak. *This makes the exposure.* The exposure can also be made by pressing the lever C. The use of button D, however, is recommended for snapshots, as it assures a steadier holding of the camera.

### Time Exposures

Move indicator A to the letter "T."

Move lever B to *f*.6.3, 8, 11, 16, 22, or 32, according to the time of exposure and nature of the subject. See tables on pages 12, 13, 28, 29 and 34.

Press lever C or button D. This *opens* the shutter. Time the exposure by a watch. Again press lever C or button D. This *closes* the shutter.

For short time exposures from one-half second to ten seconds, "Bulb" Exposures are recommended.

### "Bulb" Exposures

Move indicator A to the letter "B."

Move lever B to *f*.6.3, 8, 11, 16, 22, or 32. See tables on pages 12, 13, 28, 29 and 34.





Press lever C or button D to open the shutter, which will remain open as long as lever C or button D is held down.

*Time and "Bulb" Exposures must never be made with the Kodak held in the hands.*

***Important:*** *Never oil the shutter.* In case of accident, return the camera to your dealer or to us for repairs.

**Cable Release:** A cable release (No. 29) can be used with this Kodak if it is desired to use the Kodak Self Timer for self-portraiture. The cable release should be removed before closing the camera.

To attach the cable release, remove the screw directly behind the lever C and replace it with the cable release. After using the cable release, detach it and replace the screw in the opening. The screw may be loosened and tightened with a thin coin.

### Stop Openings

The stop openings regulate the amount of light passing through the lens. The openings are enlarged or

reduced by moving the lever B, see page 9.

***f*.6.3**—For rapidly moving objects in bright sunlight, use speed 100. For exposures on cloudy days and during rain in the middle of the day, use speed 25. For portraits outdoors, when the sun is shining, see page 30.

***Important:*** When using stop *f*.6.3 and the distance between the subject and camera is ten feet or less, the distance must be accurately measured as the depth of focus is limited, see table on page 14.

***f*.8**—For instantaneous exposures on *slightly* cloudy or hazy days, use speed 25. For scenes on narrow and slightly shaded streets, use speed 25. For moving objects in very bright sunlight, use speed 100.

***f*.11**—For *all ordinary outdoor pictures*, such as nearby landscapes showing little or no sky, groups and street scenes, when the subject is in bright sunlight, use speed 25.

***f*.16**—For open views, when the sunlight on the subject is *unusually strong* and there are no heavy shadows, such





as views at the seashore and on the water, use speed 50; for ordinary *landscapes*, in bright sunlight, with clear sky overhead, use speed 25; also for Interior Time Exposures, the time for which is given in the table on page 28.

***f*.22**—For instantaneous exposures of extremely distant landscapes, marines, snow scenes without prominent dark objects in the foreground, and clouds only, in bright sunlight, use speed 25; also for Time Exposures.

***f*.32**—For Time Exposures Outdoors on cloudy days, see table on page 34. For Interior Time Exposures, see pages 28 and 29. *Never for instantaneous exposures.*

*Failure* will result, if stop *f*.32 is used for *instantaneous exposures.*

The smaller the stop opening the greater the depth of focus or range of sharpness, see pages 14 and 15.

All exposures given for outdoor subjects are for the hours from one hour after sunrise until one hour before sunset, when using Kodak Verichrome, Super Sensitive Panchromatic or Panatomic Film. If Kodak N. C. Film is

# The Depth of Focus for Different Stop Openings

By "depth of focus" is meant the distance, in front of and behind the subject focused on, within which details in the picture will be sharp and distinct.

**Table for use with the Kodak Senior Six-16**

| Distance Focused Upon | *f*.6.3 | *f*.8 | *f*.11 | *f*.16 | *f*.32 |
|---|---|---|---|---|---|
| INF. | 66 ft. to inf. | 52 ft. to inf. | 38 ft. to inf. | 26 ft. to inf. | 13 ft. to inf. |
| 50 ft. | 28½ ft. to inf. | 25½ ft. to inf. | 21½ ft. to inf. | 17 ft. to inf. | 10½ ft. to inf. |
| 25 ft. | 18½ ft. to 40½ ft. | 16½ ft. to 48½ ft. | 15 ft. to 75½ ft. | 12½ ft. to inf. | 8½ ft. to inf. |
| 15 ft. | 12½ ft. to 19½ ft. | 11½ ft. to 21½ ft. | 10½ ft. to 25 ft. | 9½ ft. to 36½ ft. | 6½ ft. to inf. |
| 10 ft. | 8½ ft. to 11½ ft. | 8½ ft. to 12½ ft. | 7½ ft. to 13½ ft. | 7½ ft. to 16½ ft. | 5½ ft. to 45½ ft. |
| 8 ft. | 7½ ft. to 9½ ft. | 7 ft. to 9½ ft. | 6½ ft. to 10½ ft. | 6 ft. to 13½ ft. | 5 ft. to 21½ ft. |
| 6 ft. | 5½ ft. to 6½ ft. | 5½ ft. to 6½ ft. | 5½ ft. to 7½ ft. | 5 ft. to 8 ft. | 4½ ft. to 12 ft. |
| 5 ft. | 4½ ft. to 5 ft. 3 in. | 4 ft. 7 in. to 5½ ft. | 4 ft. 5 in. to 5 ft. 9 in. | 4 ft. 2 in. to 6 ft. 2 in. | 3 ft. 7 in. to 8 ft. 2 in. |
| 4 ft. | 3½ ft. to 4 ft. 3 in. | 3 ft. 8 in. to 4½ ft. | 3 ft. 7 in. to 4 ft. 6 in. | 3 ft. 6 in. to 4 ft. 9 in. | 3 ft. to 5 ft. 9 in. |
| 3½ ft. | 3½ ft. to 3 ft. 8 in. | 3 ft. 3 in. to 3½ ft. | 3 ft. 2 in. to 3 ft. 10 in. | 3 ft. 1 in. to 4 ft. | 2 ft. 9 in. to 4 ft. 9 in. |

The depth of focus is not given for *f*.22. The depth for this opening can be estimated by comparison.

"Inf." is the abbreviation for Infinity—meaning an unlimited distance from the lens.





used, exposures can be made from 2½ hours after sunrise until 2½ hours before sunset. If earlier or later, the exposures must be longer.

For a subject in the shade, under the roof of a porch, or under a tree, a time exposure must be made, see page 34. When making pictures under these conditions, the camera must be placed on some steady, firm support.

## Depth of Focus

Depth of focus is the distance from the nearest to the farthest objects that will appear sharp in the negative or print. It depends upon the distance between the subject and lens, the focal length of the lens, and the size of the stop opening used. The smaller the stop opening, the greater the depth of focus. See the table on page 14.

## The "*f*." System

A lens is said to work at a certain "speed;" this means that the lens will give a sharp image from corner to corner of the film with an opening a certain proportion of its focal length.

The focal length of a lens is the distance between the lens and the film when the Kodak is focused for INF. (infinity). It should be borne clearly in mind that this "speed" depends *not* upon the size of the opening, but upon the size of the opening *in proportion to the focal length of the lens.* The lens that will give sharp images with the largest opening is said to have the greatest "speed."

The proportional size or "value" of the stop opening is designated by the "*f.*" number and is the quotient obtained by dividing the focal length of the lens by the diameter of the stop opening.

## How to Use Your Kodak as a Fixed Focus Camera

SET THE FOCUS AT 25 FEET.
USE STOP OPENING *f.*16,
AND SPEED 25.

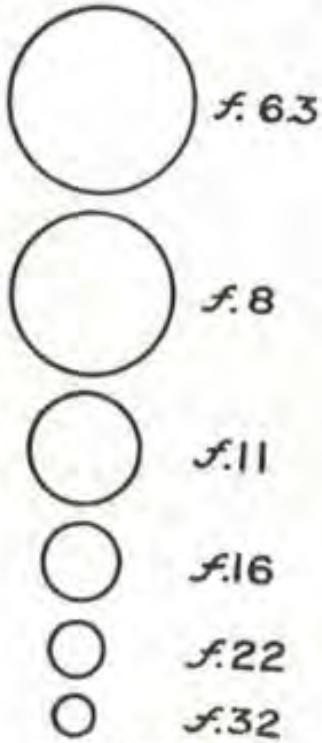
When using the Kodak as a fixed focus type, nearby subjects must be in bright sunlight, to obtain fully exposed negatives.





The range of sharpness when your Kodak is adjusted as a fixed focus camera will be found on page 14.

**Kodak Senior Six-16**






These circles are the same size as the stop openings of the shutter on the Kodak Senior Six-16. They clearly show the relative sizes of the stop openings and how their areas differ.

## Making a Horizontal Picture

*Hold camera firmly against the face.*

When making instantaneous exposures or snapshots, hold the Kodak firmly against your face and press the exposure button as shown in these two illustrations. When pressing the exposure button, hold the breath for the instant. If the Kodak is moved during the exposure, the picture will be blurred.





## Making a Vertical Picture

*Hold camera firmly against the face.*

### THE OPTICAL DIRECT VIEW FINDER

The camera is equipped with an optical direct view finder 8, page 2, attached to the side of the Kodak. To use this finder, raise the front frame by the button and both parts of the finder will spring into position. Hold the camera with the sight or rear frame

as close to the eye as possible with the camera held firmly against the face, and frame the picture within the front frame of the finder. All vertical lines in the subject should be kept parallel with the vertical sides of this frame, when holding the camera either in the vertical or horizontal position.

## Making Instantaneous Exposures or Snapshots

When ordinary instantaneous exposures or snapshots are made, the subject should be in the broad, open sunlight, but the camera must not. The sun should be behind your back or over the shoulder. If it shines directly into the lens, it will blur and fog the picture. For obtaining back- or side-lighted pictures, use a Kodak Adjustable Lens Hood No. 2.

Special instructions for making portraits are given on pages 29 to 33.

## Hold the Kodak Level

The Kodak must be held level. If all the subject cannot be included in the finder without tilting the lens





upwards, move backwards until it is all included *with the camera held level.*

*Effect produced by tilting the Kodak.*

If the subject is below the normal height, like a small child or a dog, the Kodak should be held down level with the center of the subject.

After an exposure has been made, turn the winding knob slowly, a few times, until No. 2 (or the next number) is in the *center* of the red window.

## Closing the Kodak

Before closing the Kodak, *it should be focused for INF. (infinity);* then press the plate release 10, page 2, as shown below, raise the bed and snap

it shut. The front and bellows fold automatically. If a cable release has been used, remove it before closing the camera.

## Removing the Film

After the last section of film has been exposed, turn the winding knob until the end of the paper passes the red window.

In a subdued light, open the back of the Kodak, see pages 3 and 4.

Hold the end of the paper taut, see illustration at top of page 23, and turn the knob until all the paper is on the





roll. If the sticker folds under the roll, turn the knob to bring it up.

Take hold of the ends of the paper and sticker to prevent the paper from loosening. Draw out the knob and re-

move the film. Fold under about half-an-inch of the protective paper, and fasten it with the sticker.

**"Cinch" Marks:** After removing the film from the Kodak, do not wind it tightly with a twisting motion, or the film might be scratched.

Wrap up the exposed film. It is now ready for development. This may be done by a photo finisher, or by yourself. Our Service Department will be glad to send you, upon request, complete instructions for developing and printing.

Remove the empty spool and place it in the winding end of the camera. The Kodak is now ready for reloading.





It is a good plan to reload the Kodak as soon as an exposed film has been removed, to be ready for the next pictures. For the best results, load with Kodak Film.

***Important:*** Film should be developed as soon as possible after exposure. The quality of the image on all sensitized products is retained by prompt development after exposure.

## TIME EXPOSURES—INDOORS

For time exposures the camera must always be placed on a firm support like a tripod, Optipod, table or chair, *never* hold it in the hands. The Kodak has two tripod sockets for use with a tripod, an Optipod, or a Kodapod, with the Kodak either in the vertical or horizontal position. The screws in the

tripod sockets can be removed and replaced with a thin coin.

Place the Kodak in such a position that the finder will include the view desired. The diagram on page 25 shows three positions for the camera. It should not be pointed at a window as the glare of light may blur the picture.

If the Kodak is placed on a table, for making a vertical picture, use the vertical support 4.

The camera must not be more than two or three inches from the edge of the table.





To make a horizontal picture, without a tripod, swing out the support 5, behind the shutter, and place the camera as shown below.

Adjust the shutter for a time exposure as described on page 10.

All being ready, press the exposure button or lever carefully, once to open, time the exposure by a watch, and again press the exposure button or lever to close the shutter.

After making an exposure, turn the winding knob until the next number appears in the red window.

If no more time exposures are to be made, adjust the shutter for an instantaneous exposure, see page 9.

EXPOSURE TABLE FOR INTERIORS USING STOP *f*.16

| | Bright sun | Hazy sun | Cloudy bright | Cloudy dull |
|---|---|---|---|---|
| White walls and more than one window. | 4 secs. | 10 secs. | 20 secs. | 40 secs. |
| White walls and only one window. | 6 secs. | 15 secs. | 30 secs. | 1 min. |
| Medium colored walls and furnishings and more than one window. | 8 secs. | 20 secs. | 40 secs. | 1 min. 20 secs. |
| Medium colored walls and furnishings and only one window. | 12 secs. | 30 secs. | 1 min. | 2 mins. |
| Dark colored walls and furnishings and more than one window. | 20 secs. | 40 secs. | 1 min. 20 secs. | 2 mins. 40 secs. |
| Dark colored walls and furnishings and only one window. | 40 secs. | 1 min. 20 secs. | 2 mins. 40 secs. | 5 mins. 20 secs. |

These exposures are for rooms where windows get the direct light from the sky and for hours from three hours after sunrise until three hours before sunset. If earlier or later the exposures must be longer.





## Exposure Table for Interiors

The table on page 28 gives suitable exposures for varying conditions of light, when using stop *f*.16.

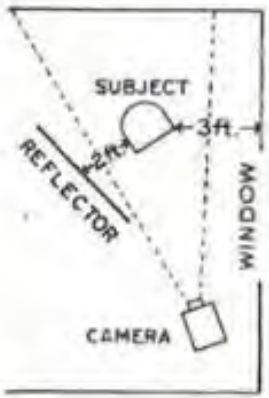
With stop *f*.6.3 give one-sixth;
" " *f*.8 " one-quarter;
" " *f*.11 " one-half;
" " *f*.22 " twice;
" " *f*.32 " four times
the exposures given in the table.

The smaller the stop opening the greater the depth of focus or range of sharpness, see page 14. Stop *f*.16 gives the best average results for Interiors.

## TO MAKE A PORTRAIT

The subject should be seated in a chair partly facing the light with the body turned slightly away from, and the face turned towards the Kodak which should be a little higher than an ordinary table. The subject should look at an object level with the lens or directly at the lens. Compose the picture in the finder. For a three-quarter figure the Kodak should be about eight feet from the subject; and for a full-length figure, about ten feet. The background should form a contrast

with the subject; a light background usually gives a better effect than a dark one. To get a good light on the face, follow the arrangement shown in the diagram at the left. A reflector helps to get detail in the shaded part of the face. A white towel or tablecloth held by an assistant or thrown over a screen or other high piece of furniture will make a suitable reflector; it should be at an angle and in the position indicated.




If the above suggestion for lighting is followed, an exposure of about one second with stop *f*.11 will be sufficient on a bright day.

## Making Portraits Outdoors

When making portraits outdoors, with the sun shining brightly, the subject should be in the shadow of a building or a large tree, but with clear and unobstructed sky overhead—use stop *f*.6.3 and speed 25. By following this





rule, unpleasant and distorting shadows on the face will be avoided. The best results are obtained with the subject fairly close to the camera and the lens adjusted accordingly. When the distance between the subject and Kodak is ten feet or less, measure the distance carefully, see table on page 14.

## Kodak Portrait Attachment

This Kodak can be focused at 3½ feet, which makes it possible to obtain excellent head and shoulder portraits without the use of the Kodak Portrait Attachment.

By using the Kodak Portrait Attachment, large images of flowers and similar "still life" subjects can be obtained. For the best results when making pictures of subjects at short distances, it is advisable to use the *f*.8 or a smaller stop opening.

Place the Attachment over the lens and compose the picture in the finder. When making vertical pictures, turn the Kodak just a *little* to the right, as the short distances at which the subject must be from the lens make it

necessary to center the subject by eye instead of by the finder.

| Distance Between Subject and Lens must be | The Focusing Collar must be turned to |
|---|---|
| 1 foot 11 inches | 3½ feet |
| 2 feet 1 inch | 4 " |
| 2 feet 4 inches | 5 " |
| 2 " 6 " | 6 " |
| 2 " 9 " | 8 " |
| 3 " | 10 " |
| 3 " 4 " | 15 " |
| 3 " 8 " | 25 " |
| 4 " | 50 " |
| 4 " 2 " | INF. (infinity) |

The subject must be at one of the distances from the Kodak, given in the table above. Measure the distance carefully from the lens to the subject, and revolve the lens mount until the correct figure is at the pointer E (page 8) according to the table.

The same exposure is required as without the Attachment.

Use *Kodak Portrait Attachment No. 5*, with the Kodak Senior Six-16, with the Kodak Anastigmat Lens *f*.6.3.





## Kodak Diffusion Portrait Attachment

The Kodak Diffusion Portrait Attachment is a supplementary lens used in the same manner as the regular Kodak Portrait Attachment. It produces a true, soft-focus effect.

Use *Kodak Diffusion Portrait Attachment No. 5*, with the Kodak Senior Six-16, with the Kodak Anastigmat Lens *f*.6.3.

"At Home with Your Kodak" is a booklet containing many diagrams and illustrations showing various lighting effects. It gives suggestions for making pictures in and around the home.

"Picture Taking at Night" is a booklet that describes in detail the methods of making pictures by electric light, flash-light exposures, campfire scenes, fireworks, lightning, moonlight effects, silhouettes and other novel and unusual pictures.

These two booklets are free, and copies of them will be sent upon request to our Service Department.

## Time Exposures—Outdoors

When the smallest stop opening (*f*.32) is used, the light passing through the lens is so much reduced that very short time exposures may be made outdoors.

For short time exposures described below, use the "Bulb" Exposure, see page 10.

**With Light Clouds**—From one to three seconds will be sufficient.

**With Heavy Clouds**—Four seconds to eight seconds will be required.

**With Sunshine**—Time Exposures should not be made.

When making time exposures the Kodak must be placed on some steady, firm support, do not hold it in the hands or the picture will be blurred.

## Clean Lenses

*Made with Dirty Lens. Made with Clean Lens.*





The pictures on page 34 illustrate the difference between results with a dirty and a clean lens.

Lenses should be cleaned as follows:

Open the back of the Kodak, see pages 3 and 4; then open the front as described on page 7. Wipe the front and back of the lens with Lens Cleaning Paper or a clean handkerchief. Never unscrew the lens.

## Keep Dust Out of the Camera

Wipe the inside of the camera and bellows, occasionally, with a slightly damp cloth, especially if the camera has not been used for some time.

EASTMAN KODAK COMPANY,
Rochester, N. Y.

## PRICE LIST

| | |
|---|---|
| KODAK VERICHROME FILM, V 616, for the Kodak Senior Six-16, 2½ x 4¼, eight exposures | $ .35 |
| KODAK SUPER SENSITIVE PANCHROMATIC FILM, SS 616, 2½ x 4¼, eight exposures | .40 |
| KODAK PANATOMIC FILM, F 616, 2½ x 4¼, eight exposures | .40 |
| KODAK N. C. FILM, 616, 2½ x 4¼, eight exposures | .30 |
| KODAK PORTRAIT ATTACHMENT, No. 5, for the Kodak Senior Six-16 | .75 |
| KODAK DIFFUSION PORTRAIT ATTACHMENT, No. 5 | 1.50 |
| KODAK SKY FILTER, No. 5 | 1.50 |
| KODAK COLOR FILTER, No. 5 | 1.50 |
| KODAK PICTORIAL DIFFUSION DISK, No. 5 | 2.50 |
| KODAK ADJUSTABLE LENS HOOD, No. 2 | 1.00 |
| KODAK METAL TRIPOD, No. 0 | 2.75 |
| No. 1 | 4.50 |
| No. 2 | 5.00 |
| OPTIPOD, for attaching camera to the edge of a table, chair, fence, etc. | 1.25 |
| KODAPOD, for attaching camera to a tree, fence or similar rough surface | 1.75 |
| CABLE RELEASE, No. 29, for the Kodak Senior Six-16 | .35 |
| KODAK SELF TIMER, fits on the cable release and automatically presses the push-pin, enabling the photographer to be included in the picture | 1.25 |
| KODAK NEGATIVE ALBUM, to hold 100 2½ x 4¼ or smaller negatives | 1.25 |

*All prices subject to change without notice.*

EASTMAN KODAK COMPANY,
ROCHESTER, N. Y.



## IMPORTANT

This manual should be read thoroughly, before you make any pictures.

While loading and unloading the camera, be very careful to keep the protective paper wound tightly around the film to prevent light striking it.

Before making an exposure be sure that the shutter is adjusted properly, for an instantaneous or time exposure, whichever is required. Use the correct stop opening and speed. The camera must be focused and an unexposed section of film in position.

The sun must be behind your back or over the shoulder. If the sun shines directly into the lens it will blur and fog the picture.

Hold the camera *level.*

Hold the camera *steady* when making instantaneous exposures or snapshots. The camera should be held firmly against the face, and when pressing the exposure button or lever, hold the breath for the instant. If the camera is moved during the exposure, the picture will be blurred.

Turn a new section of film into position immediately after making an exposure. This prevents making two pictures on the same section of film.

Keep the lens and inside of camera clean.

Never oil the shutter.

Instructions for making time exposures, indoors and outdoors, are included in this manual.

EASTMAN KODAK COMPANY,
ROCHESTER, N. Y.

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# Nikon

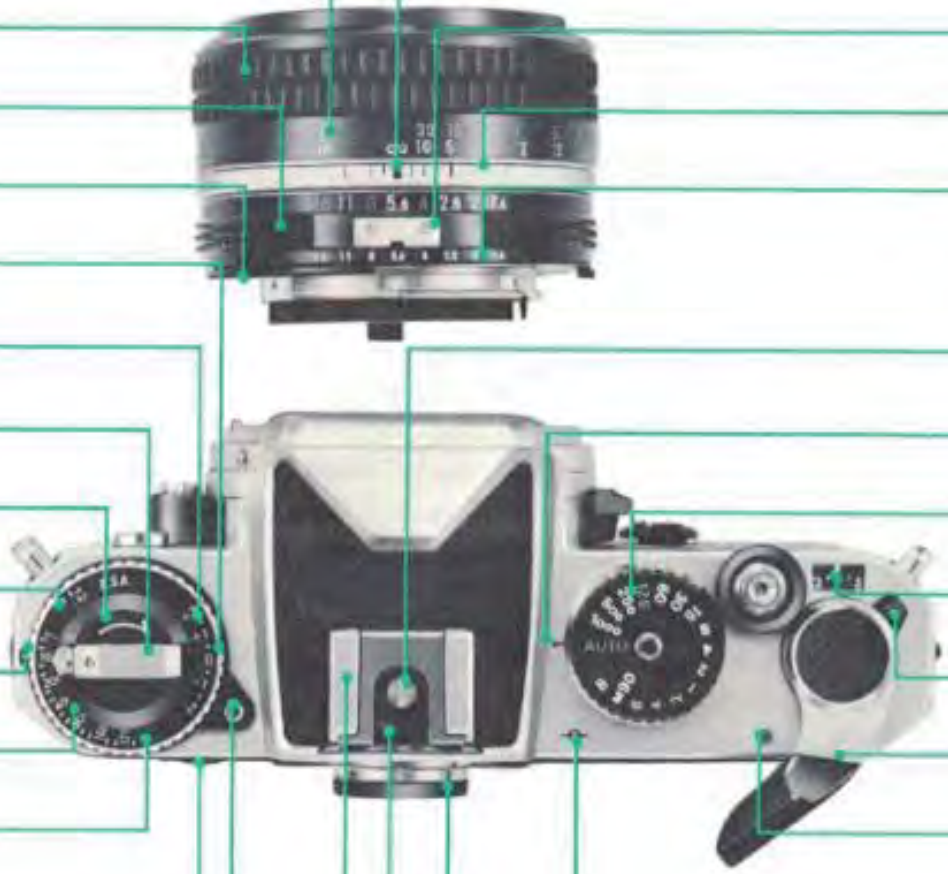
# FE

INSTRUCTION MANUAL

# NOMENCLATURE


Shutter-speed dial lock
Shutter release button
Shutter release fingerguard
Neckstrap eyelet
Depth-of-field preview lever
Self-timer/memory lock
Reflex mirror
Lens mounting flange
Lens aperture direct readout window
Meter coupling lever
Meter coupling lever release
Sync terminal (cover provided)
Lens mounting index
Lens release button
Focusing screen holder release

Motor drive shutter coupling
Motor drive coupling
Film rewind button
Tripod socket
Battery chamber lid
Motor drive electrical contacts
Memo holder



Distance scale
Focusing ring
Aperture ring
Meter coupling ridge
Exposure compensation index
Exposure compensation scale
Film rewind crank
Film rewind knob
Safety lock
Film-speed scale index
ASA film-speed scale/dial
Exposure compensation ring
Power check lever/lamp
ASA film-speed dial lock
Accessory shoe

Aperture/distance scale index
Meter coupling shoe
Depth-of-field indicators
Aperture-direct-readout scale
Hot-shoe contact
Shutter-speed index
Shutter-speed scale
Frame counter
Multi-exposure lever
Film-advance lever
Meter ON index
Film-plane indicator
Viewfinder eyepiece (w/ready-light)
Ready-light contact

# CONTENTS

# FOREWORD

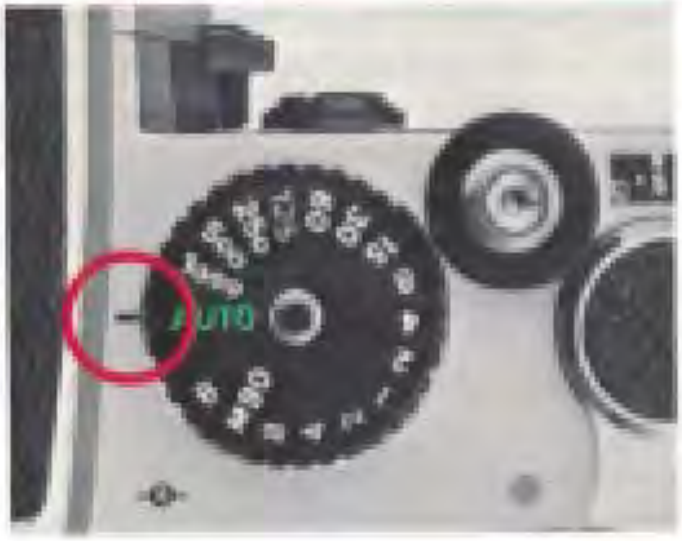
The Nikon FE is a compact 35mm single-lens reflex camera with a host of outstanding features. It offers aperture-priority automatic exposure control with shutter speeds from 1/1000 second down to 8 seconds, has interchangeable focusing screens, and accepts the optional MD-12 for motor-driven exposures up to 3.5 frames per second. In addition, the FE incorporates automatic flash speed setting when used in conjunction with the accessory Speedlight Unit SB-10. When the SB-10 is mounted on the camera's hot shoe and turned on, the shutter speed is automatically set to the proper synchronization speed of 1/90 second when the camera is set to "automatic." The FE will also accept virtually every accessory in the Nikon System—the most comprehensive ever created for photography. To get the most out of this camera, study the instructions in this manual carefully, and practice using the controls before loading the camera with film. Keep the manual on hand for ready reference until you have mastered operation. The few minutes you spend familiarizing yourself with the camera will guarantee you the best results and increase your pleasure in taking pictures many times over.

# OPERATION OF CAMERA CONTROLS

## Setting the Shutter Speed

The Nikon FE is set for automatic or manual shutter speed selection via the shutter-speed dial positioned to the right of the finder, with setting operation possible at any time either before or after the shutter is wound. The dial is provided with positions for automatic (AUTO), and manual speeds from 8 seconds to 1/1000 second. To set the dial for automatic shutter speed selection, simply rotate the dial clockwise until the green AUTO (automatic) setting clicks and locks into place aligned with the shutter-speed scale index at the base of the dial; the built-in locking mechanism ensures that the dial cannot be accidently shifted from the automatic position during shooting.

To set the dial for manual shutter speed selection used during "match-needle" exposure measurement, simply hold in the shutter-speed dial lock and rotate the dial counterclockwise off the "AUTO" position; when the dial is aligned with white settings from 2 to 1000, the actual shutter speed is a fractional value from 1/2 second to 1/1000 second, while the remaining settings indicate the actual values from 8 seconds to 1 second. The "M90" setting indicates a mechanical shutter speed of 1/90 second which operates independently of battery power. This is the only setting (except "B") which can be used when




the batteries are exhausted or none are loaded in the camera. The "M90" setting also serves as a known shutter speed when shooting with electronic flash. At the "B" setting, the shutter remains open as long as the shutter release button is depressed. "B" is also a mechanical shutter speed, so there is no battery drain when shooting time exposures. To conserve battery power when making really long time exposures, use a cable release and then push the film-advance lever back in flush with the camera body after opening the shutter. Note that the 125 setting is engraved in red; this indicates 1/125 second, the fastest shutter speed available for synchronization with electronic flash units. (Refer to page 37 for additional information on flash photography.)

Nikon

NIPPON KOGAKU K.K.



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# The Development of Digital Still Camera using I.3M-Pixel VT-CCD Image Sensor

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Abstract:
We have developed a 2/3-inch 1.3M-pixel full-frame readout VT-CCD (Vacancy Transfer CCD) image sensor for digital still cameras. We have also completed a portable SLR-type digital still camera using this CCD image sensor. We can obtain as much image quality and resolution as in conventional photoprint.

## 1. Introduction

In recent years, digital cameras have gained attention as image-data input devices in the fields of commercial photography, news reporting, medicine and printing along with the advent of the age of multimedia that comprehensively handles still images, videos, audio and character information, along with the higher functionality of personal computers and networks. So to support this multimedia generation, the single-lens reflex (SLR) type digital camera DS-505/515 was developed.

The concept of the DS-505/515 was to place importance on high quality and behavior and operability by which it can be used with the same feeling as a conventional single-lens reflex type camera.

For that reason, the DS-505/515 was developed as a new image sensor (VT-CCD) that simultaneously reads all 1.3 million pixels in a 2/3 inch size as a dedicated still image to attain image quality that can be compared to LS size prints that require high-image quality2).

The following is an overview of the digital camera DS-505/515 system, and a report on the main engineering and imaging elements.


Fig. 1 DS-505/515, HG-15

2. DS-505 System Configuration

The DS-505 is a single-shot model and the DS-515 is continuous shooting model. (DS-515 is capable of continuous shooting at 3 frames/second.) The following is a description using DS-505 as an example.

Fig. 2 shows the overall configuration of the camera system. Image data is interfaced with a personal computer using a PC card, MO device, and SCSI, as shown in the drawing.

Fig. 3 is a block diagram of internal signal processes in the digital camera DS-505.

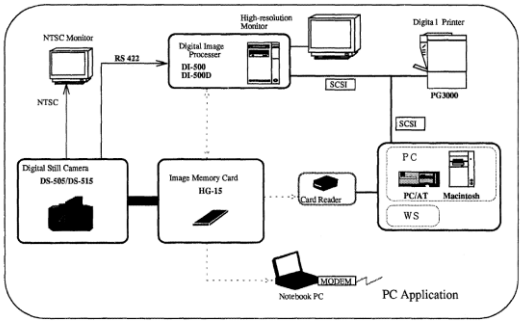


Fig. 2 Digital Still Camera System

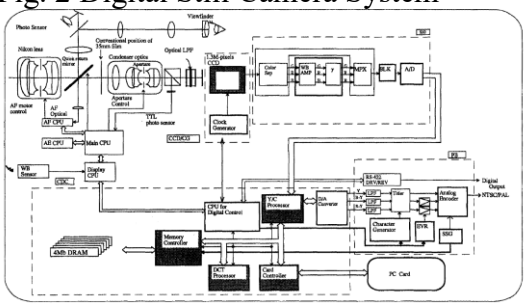

Fig. 3 Block Diagram of DS-505

3. Main Specifications (Features)

Table 1 shows the main specifications of the DS-505.

The following will describe the features of this digital still camera.

1) Attains high-image quality and high-resolution by mounting a I.3M-Pixel VT-CCD

2) Used with the same feel as a single-lens reflex (SLR) camera. (Adopts an optical reduction system, replacement lens, and others)

3) More compact because of the development of a signal-processing LSI.

4) Adopts a PC card (HG-15, 15 MB) that records at high speed.

4) VT-CCD

4-1) CCD Device

This time, a method image sensor for independently reading all 1.3 million pixels (VT method: Vacancy Transfer) in a 2/3 inch size was developed as to be dedicated to still images. This device simultaneously reads and transfers an image of a full frame that includes 1,280 (H) x 1,001 (V) effective pixels.

A G vertical-stripe R/B complete checkerboard method was attained as a result of simulating filter arrangements. Table 2 shows the element performance in this device.

| | |
|---|---|
| Transfer architecture | Vacancy Transfer(VT) |
| Optical format | 2/3 inch |
| Number of effective pixels | 1,280 (H) × 1,001 (V) |
| Number of total pixels | 1,364 (H) × 1,032 (V) |
| Aspect ratio | 5:4 |
| Pixel size | 6.8 (H) × 6.8 (V) $\mu m^2$ |
| Effective pixel size | 8.7 (H) × 6.96 (V) $mm^2$ |
| Optical black | (H):front 4pixel rear 72pixel<br>(V):front 4pixel rear 4pixel |
| Frame rate | 1/5.96sec |
| Package | 28pin DIP |
| Filter | G line stripe<br>R/B perfect checker |
| Sensitivity | 220mV<br>Green signal F5.6(1,200nt) |
| Saturation output voltage | 400mV |
| Shutter speed | 1/2 ～ 1/8,000sec |

Table 2. Specification and Performance

| | |
|---|---|
| Format | SLR Digital Still Camera |
| Lens mount | Nikon F mount |
| Focus models | Auto/manual |
| Exposure control | Programmed auto/aperture priority/ shutter priority/manual modes |
| Shutter control | Electronically controlled focal plane shutter<br>Manual : 1/2000 ~ 1/8 sec<br>Auto : 1/1000 ~ 1/2 sec<br>Flash Sync : 1/250 sec |
| Aperture | F=6.7 ~ 38 Set in the internal Condensor lens |
| Exposure compensation | 1/4EV step/±3EV max |
| Finder | Optical Finder/Frame coverage:virtually 100% of actual picture area Viewing magnification:0.72X |
| Continuous film advance | 3 frames/sec up to 7 frames(DS-515),1frame/sec(DS-505) when using Image Memory Card HG-15 |
| CCD | 2/3-inch, 1.3M-pixel (1,280×1,001) CCD |
| Effective ISO | ISO 800/1600 |
| White balance | Auto/manual(5-step)modes |
| File size | 1,280×1,000 pixels, 24-bits color |
| Storage medium | ATA Type I or II, Flash |
| Data compression | JPEG standard |
| Number of frames | Compression mode / Number of frames<br>Hi(Uncompressed) 5 frames<br>Fine 21 frames<br>Normal 43 frames<br>Basic 84 frames |
| Output | Video output : NTSC/PAL Digital output : RS-422 |
| Power source | Dedicated NiCd battery / External power supply |

Table l. Specification of DS-505

4-2) VT Method

Ordinary inter-line type CCDs read signal charges from all photodiodes to a vertical transfer path. It is not possible to transfer the charge without mixing.

There, by injecting an empty packet generated from a horizontal charge transfer path side and moving this empty packet in a direction reverse to the vertical charge transfer path, it is possible to read all pixels at the same time.

Fig. 4 is a view of the potential of a vertical transfer path that shows the drive method of the device. This shows that four transfer electrodes in order from nearest to the horizontal transfer path are one block; sequential vertical transfer pulses are charged and the empty packet moves sequentially in the reverse direction.

This injection operation of the empty packet is implemented in each horizontal period, and the empty packet is dispersed in 8-horizontal line increments in the vertical transfer route.

Fig. 5 shows a block diagram of the VT-CCD.

In order to attain this transfer method, a VT scanning circuit, a vertical-transfer pulse control circuit, and a charge-reading pulse charge circuit were disposed in an ordinary inter-line CCD.

The VT scanning circuit is composed of a shift register that generates a pulse for sequentially selecting a blocked vertical transfer electrode. Output from the scanning circuit is contacted to the vertical transfer pulse control circuit, and a vertical drive pulse is charged to the selected block electrode. The charge-read-out pulse charge circuit is a circuit that controls the read-out gate to transferring the signal charge accumulated in the photodiode to the accumulated packet in the vertical transfer path. To read-out all pixels simultaneously, it is acceptable to turn on all TG pulses simultaneously.

4-3) Others Features

As another feature of this device, it also capable of the following drive, in addition to simultaneous read-out of all pixels, described above.

1) Movie mode (Fig. 6-1)

Includes a motor mode for reading the signal charge for each four vertical lines. Also includes a function for interlacing pixels in a 1,280 x 250 pixel field every 1/30 seconds.

2) AE mode (Fig. 6-2)

Drive method for reading pixels in a 1,280 x 125 pixel field without mixing each color, using a drive method for reading at high speed of 1/60 seconds for each eight vertical lines.

3) AF mode (Fig. 6-3)

This is a drive method for reading pixels at the high speed of 1/60 seconds for each eight vertical lines similar to AE mode. However, to attain the information amount of the horizontal direction, this is a drive method for reading by calculating 2 pixels in the vertical direction.

It is possible to support the drive method described above so it is possible to implement pre-processes such as exporting images to an electronic

viewfinder or AE/AF and others, with the same speed as a conventional still camera.

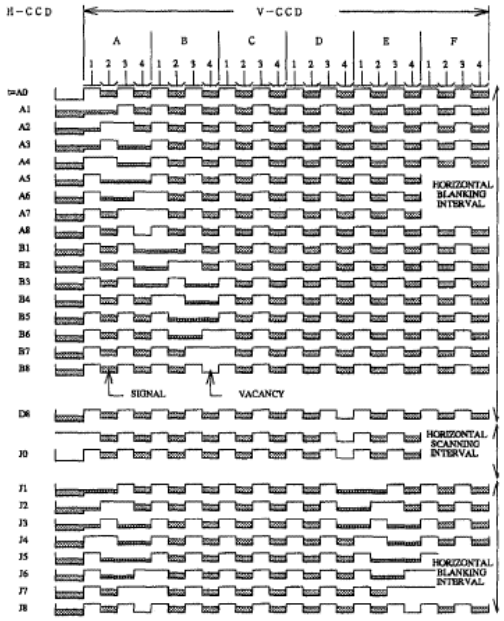


**Fig.4 Potential diagram of VT-method**

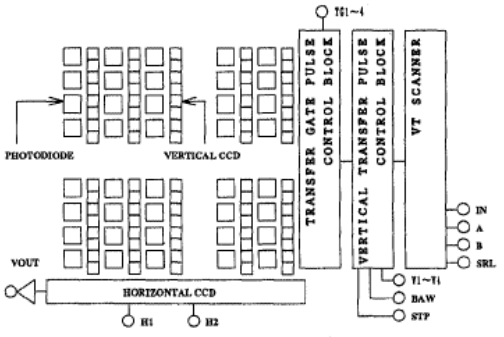


**Fig.5 Schematic diagram of this device**

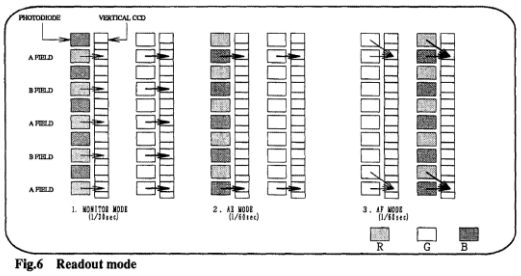


**Fig.6 Readout mode**

Optical Reduction System

Conventional single-lens reflex type digital still cameras could only record a portion of the image that can be seen from the finder, but with the DS-505/515, an optical reduction system was mounted to guide the image angle of the lends as it is to the CCD.

With this, the entire range in the finder visual field can be image-recorded, so imaging is possible with the same feeling as a single-lens reflex camera. 3)

6. Signal-processing LSI

Four types of signal processing LSI (YC processor, memory controller, DCT processor, card controller) shown in the block diagram of Fig. 2 were developed. 4)

Brightness/color-difference signal processing for VT-CCD signal output, JPEG-standard DCT compression and decompression, memory control, and card-interfacing of PC cards as recording media are possible with this LSI.

Also included are the low-power consumption features such as compactness, and support for 3.3 V drive and others. It is possible to constitute the most optimum circuit for the compact digital camera, and dramatically improve compatibility with PCs by adopting JPEG compression and PC card recording.

7. Recording Behavior and PC Cards

For the recording media, PC cards (ATA flash memory) which comply with PCMCIA have been adopted. When recording to ATA, compressed and uncompressed data is recorded at high speed to the card by buffering in sector units. For ATA, PC cards with a capacity of 15 M and that can record at the high speed of approximately 1 second/image is used.

8. Summary

It has become possible to obtain image quality comparable to L size (5 x 4 inches) prints by installing the 1.3 million-pixel VT CCD. Also, a size and weight equivalent to a single-lens reflex camera has been attained by making a majority of the electrical circuits ICs. These have gained favorable reviews in the commercial photography, and medical fields.

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IPU '97-15, CE' 97-7 (Mar, 1997)

# A4M-Pixel CMD Image Sensor

A4M-Pixel CMD Image Sensor

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A 4M-pixel Charge Modulation Device (CMD) image sensor with pixel size of 7.5 ×7.5 $\mu m^2$ has been developed. The sensor has three readout modes that are a full, a skip and a block modes. A4 M-Pixel image is obtained in the full modes, while an arbitrary window-of-interest can be read out in the block modes. The skip mode reads every $4^{th}$ pixel in both horizontal and vertical directions. The frame rate can be raised in the skip and the block modes. The sensor also has a capability of lowering the dark current generation during the integration time.

## 1. Introduction

In recent years, the demand for higher resolutions of electronic images has become extremely high. For that reason, a breakthrough has been required in problems relating to embedding in conventional, standard television format. The biggest of these problems, relating to ease-of-use for image quality and image-inputting devices, is the frame rate.

In this paper, the authors report on a 4 million-pixel CMD imaging element that they developed, with a focus on this viewpoint.[1)]

Several items that use CCD as high-resolution imaging elements that exceed high-vision (2-million pixels) have been reported.[2)] However, most of these imaging elements substantially support still images, and it can take several seconds to load the image of one frame. For that reason, there are a variety of restrictions in the demand for industrial and consumer use. For example, using the example of a digital still camera, the fact that it is not possible to attain framing or focusing which are indispensable camera functions in real-time are major disadvantages of these kinds of cameras with high-resolution imaging elements. Also, because the frame rate is low, it takes a long time to accumulate a signal charge so there is a problem in that image quality degrades because of a dark charge that is accumulated along with the signal charge. A method has also been adopted in some to cool the elements in order to suppress the generation of the dark charge, but this introduces a new problem of

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IPU '97-15, CE' 97-7 (Mar, 1997)

increased power consumption of the overall system.

Still further, a variety of exposure times are used in electronic still cameras which are different from TV cameras. As the exposure time increases, a dark charge for that amount is accumulated. This invites serious image degradation along with the accumulation of a dark current caused by the low frame rate.

1-1. Countermeasure for Solving the Frame-rate Problem in High-resolution Imaging Elements

The basic countermeasure for solving the problem described above which is caused by a low frame-rate is to raise the data rate of the signal. For that reason, there is a method for making the drive block itself high-speed, and a method for improving the effective data rate by using multiple signal output lines. However, in the case of the 4 million pixel imaging elements, for example, the clock frequency required to attain a frame-rate of 30 fps with the former method is 150 MHz or higher. In such a case, major difficulties are expected considering an increase in the signal band and additional processing circuits.

Also, with ordinary CCDs, the temperature of the element rises because of the increased power consumption in line with the higher clock speed; there is a high danger that that will cause image degradation caused by the dark current. Conversely, the latter method for reading out using multiple lines is often used with high-speed cameras, but there is a tendency for images to degrade when processing circuits becoming more complex, and variations in each output line and processing circuit return to the low-frequency side of video signals.

For that reason, the authors developed a new scanning method that solves the bugs in functionality and performance to circumvent a situation that directly faces new problems caused by making data rates high-speed as they are. For that reason, firstly, the authors organized the problems caused by a low frame-rate, namely the three points already mentioned. They are:

(1) Maintaining framing an overall image observation in real time;

(2) Maintaining focusing and detailed observation in real time; and

(3) Preventing image degradation cause by accumulation of a dark charge.

The authors undertook development with a view to solving each of these problems using the following methods.

(1) Thinned readout: Spatial resolution degrades, but functional requirements are matched and real-time is maintained.

(2) Any region readout: Viewability of the entire image angle is lost, but functional requirements are matched and real-time is maintained.

(3) Low-dark current drive: Alleviates pixel bias during exposure of the read-out of all pixels and prevents image degradation by reducing the dark current.

The following reports on the overall design and the results of evaluations of prototype imaging elements.

1-2. Design

When designing this image sensor, functions for freely switching the three read-out methods (all pixels, thinning/random range) were installed in the scanning circuit, in order to solve the problem of frame-rate. Also, a function for implementing low-dark current drive was installed to suppress the generation

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March 14, 1997 (Fri.) The Institute of Image Information and Television Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 37-42

IPU '97-15, CE' 97-7 (Mar, 1997)

of the dark charge when a charge is accumulated.

1-3. Sensor Configuration

Fig. 1 is a circuit diagram for the CMD imaging elements. CMD is a 4-terminal MOS device. Three terminals other than the gate are biased to DC.

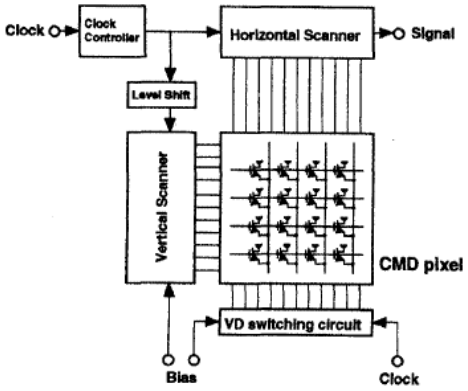


Fig.1 Block diagram of the CMD image sensor.

CMD behavior control is implemented by changing the gate potential; the CMD source current is handled as an output signal. Each row of CMD source terminals is commonly connected to the source line in the vertical direction. This source line is connected to the output signal line via a MOS switch driven by a horizontal scan circuit. The gate for CMDs in each line is commonly connected to the horizontal direction gate line. The CMD of each line is controlled for read-out behavior and reset behavior by a pulse charged to each gate line from the vertical scan circuit.

Pixel selection of CMD imaging elements as described above is implemented by an X-Y address method.

2. New Development Item 1 (Each Type of Read-out Method)

Fig. 2 shows the general concepts newly developed for Full mode, Skip mode, and Block mode with these imaging elements.

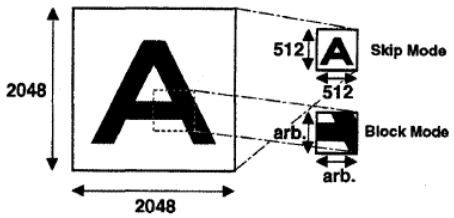


Fig.2 Schematic diagram of three read-out modes.

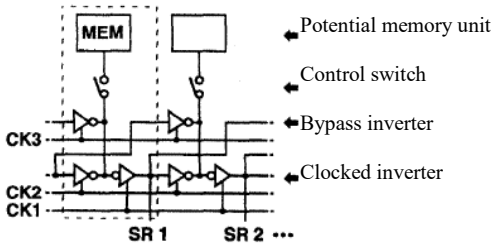


Fig.3 Configuration of the shift register.

Generally, a decoder is used for read-out of any pixel. However, with a decoder, no bit is equivalent in a circuit, so there is concern that streak-like FPN will be generated. Therefore, a circuit was developed with all bits having the same configuration. Fig. 3 is a conceptual view of the scanning circuit developed this time. The shaded portion is a unit of one level of the scanning circuit. This unit is composed of a potential memory unit for a read-out position setting in block mode, a control switch for switching the clocked inverter when not using the potential memory unit, and a bypass inverter for transferring a transfer pulse when in skip mode from a next level clocked inverter to a destination. Behavior of the scanning circuit to attain each scanning mode will now be described below.

2-1. Full Mode

Fig. 4 is a timing chart when in full mode drive. With full mode scanning, fix CK3 in Fig. 3 to low level, and turn off the control switch at the same time to

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March 14, 1997 (Fri.) The Institute of Image Information and Television Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 37-42

IPU '97-15, CE' 97-7 (Mar, 1997)

electrically separate the potential memory unit, and the bypass inverter from the clocked inverter. For that reason, in full mode, this has the same scan circuit configuration as conventional CMD imaging elements. The result is that the start pulse is transferred sequentially by CK 1 and CK 2 inside the clocked inverter, and carried to the final stage of the shift registers. Row and line selection signals appear in sequence of SR 1, SR 2 • • •; in full mode, it is possible to attain an image with the resolution of 4 million pixels.

2-2. Skip Mode

Fig. 5 shows the timing chart when in skip mode drive. It is possible to attain random thinning rates by changing the connection of the bypass inverter, but with these imaging elements, it was designed to thin three pixels of four pixels in both the horizontal and vertical directions. This resulted in being able to obtain all pixels obtained in the field angle of the imaging elements as a rough image thinned at 1/16. The frame-rate is 30 fps, and it is also possible to display video.

When scanning in skip mode, by tuning off the control switch, the potential memory unit is separated in the same way as in full mode. Also, fixing CK2 to low level stops operation of the initial inverter of the clocked inverters at two levels that compose single units of the shift registers. The result is that the shift pulse is transferred to the bypass inverter and the last level inverter of the clocked inverters at two levels by CK 1, and CK 3.

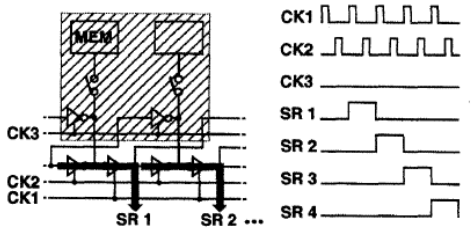


Fig.4 Timing diagram of the Full mode.

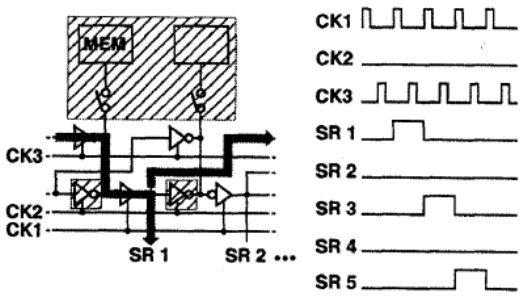


Fig.5 Timing diagram of the Skip mode.

2-3. Block Mode

Block mode is a scanning method for reading out all image information in an arbitrary, specified range. A two-stage process is required to implement block mode. These are a process for setting the read-starting position and a process for actually reading out an arbitrary range.

Fig. 6(a) is a timing charge for setting the read-starting position in block mode. In order to set the read-starting position, firstly, electrically separate the bypass inverter by fixing CK 3 to low level. Until the signal-reading position is set, the content of the clocked inverter that is two levels is sequentially transferred by the start pulse. When the transferred start pulse reaches the desired read-out-starting position, node information in clocked inverters at each level is transferred altogether to the potential memory unit a the corresponding position when all control switches are turned on. The result is that the low level is set for only the

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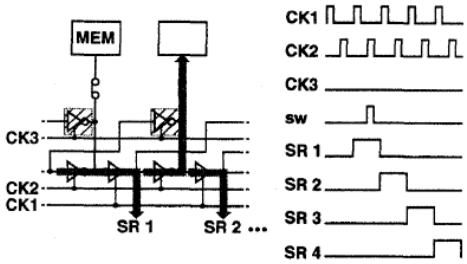
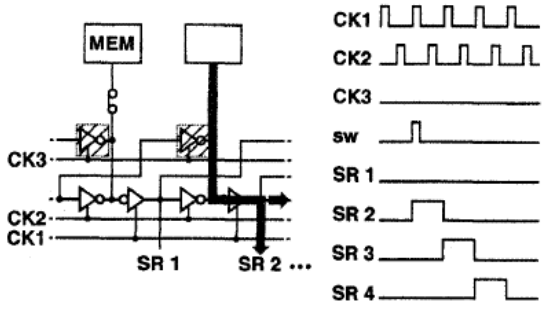
March 14, 1997 (Fri.) The Institute of Image Information and Television Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 37-42

IPU '97-15, CE' 97-7 (Mar, 1997)

potential memory unit at the position to start reading.




(a) Start address set-up




(b) Signal readout

Fig.6 Timing diagram of the Block mode.

Next, the scan circuit drive method for reading out signals in an arbitrary range will be described. Fig. 6(b) is a timing charge for reading gout signals in block mode. In the same way as setting the read-starting mode, electrically separate the bypass inverter by fixing CK 3 to low. Potential information that is retained in the potential memory unit is transferred into the shift registers when the control switch is turned on while driving CK 1, and CK 2. The result is that the selection signal appears at SR 2 in Fig. 3, and is sequentially transferred to a later stage by CK 1, and CK 2. The range to read can be randomly specified, but if the pixel count to read is not different from skip mode, the frame-rate will be 30 fps, and video display will be possible.

## 3. New Development Item 2 (Low-dark Current Drive)

Details of the mechanism that generates CMD dark current is being analyzed, but the authors have understood that dependency on the gate drain electrical field is one major factor[3)] . The low-dark current drive that was adopted for these imaging elements will be described after the conventional CMD drive is described. The low-dark current drive adopted for these imaging elements will be described after describing the conventional CMD drive below.

### 3-1. Low-dark Current Drive

Fig. 7(a) is a drive method for conventional CMD imaging elements. A positive DC bias is charged to a drain electrode, and is fixed to approximately a normal 3V. In this state, CMD behavior is controlled by changing the gate voltage VG. The charge accumulation status is maintained while a voltage; $V_{AC}$ is charged to the CMD gate electrode to accumulate a charge. The CMD is cut-off and the source current does not flow. Here, when a potential; VRD for reading the signal is charged to the gate electrode, the source current is started to be read. Also, an overflow potential; VOF for sweeping away an excess charge is supplied to non-selected pixels during the horizontal blanking period. Normally, a voltage of approximately -6V is charged to VAC in the potential accumulation state, so the potential difference; VGD between the gate and drain is a maximum of 9V.

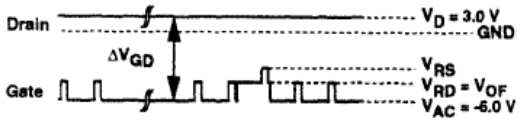
Fig. 7(b) is a drive method for the newly developed CMD imaging elements. By lowering the drain voltage; VD for the exposure time in full mode, generation of the dark charge is suppressed by

The Institute of Image Information and Television Engineers

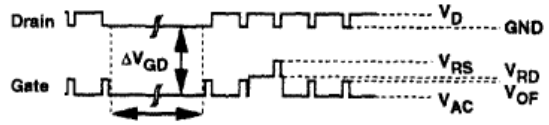
March 14, 1997 (Fri.) The Institute of Image Information and Television Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 37-42

IPU '97-15, CE' 97-7 (Mar, 1997)

mitigating the electrical field between the gate and drain. For that reason, VD is supplied via a VD switch. Therefore, when the VD switch is turned on, the terminal supplying VD is switched to GND. With these imaging elements, the potential difference ΔVGD between the gate and drain is mitigated from a maximum of 9V to 6 V.




(a) Conventional driving of the CMD image sensor




(b) New driving of the CMD image

## 4. Evaluation Results

### 4-1. Each Read-out Method (Full/Skip/Block)

Fig. 8(a) and Fig. 8(b) show imaging examples in a resolution chart. Fig. 8(a) is an imaging example of a resolution chart for the skip mode. Here, an entire image of a target object is obtained within an angle of view that can capture with an image area of these imaging elements. Pixels are thinned to 1/16 in line with the horizontal and vertical directions. Fig. 8(b) is an imaging example of a resolution chart for the block mode. Fig. 8(b) is a view of reading a region indicated by the white frame in Fig. 8(a). The drive frequency of these imaging elements is approximately 12 MHz; these imaging examples are displayed on an NTSC monitor. The frame-rate for both skip and block modes is 30 fps, and it is also possible to display video. Also, in full mode, resolution of 2,000 TVs is implemented for both horizontal and vertical directions.

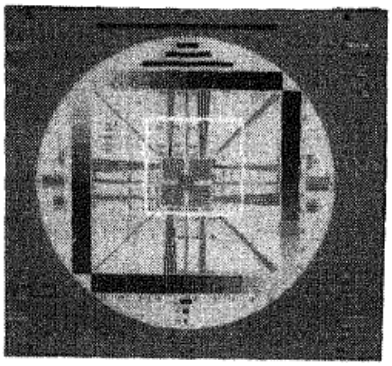
### 4-2. Low-dark Current Drive

Fig. 9 is a graph showing results when implementing low-dark current drive while accumulating a charge. The horizontal axis represents the time for accumulating a charge; the vertical axis represents the amount of increase of signal currents caused by accumulating a dark charge. The incline in the graph is equivalent to the rate of generation of the charge for each. As a result of implementing low-dark current drive with the prototype elements this time,
generation of a dark charge compared to the conventional method was suppressed 30%. With this, it is possible to reduce the amount accumulated during exposure of the dark-current charge accumulated in full mode.

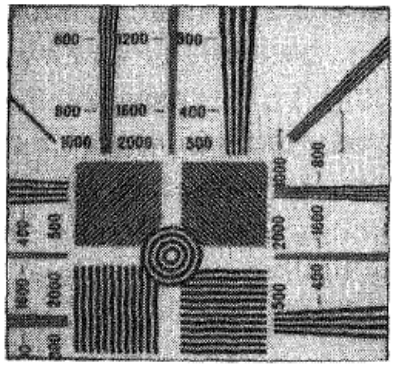
The Institute of Image Information and Television Engineers

March 14, 1997 (F ision Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 42

IPU '97-15, CE' 97-7 (Mar, 1997)



*(a) Skip mode.*



*(b) Block mode.*

Fig.8 Reproduced images

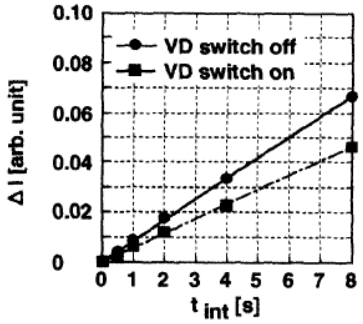



Fig.9 Dark current generation.

4-3. Element Characteristics

Table 1 shows the design characteristics and features of these imaging elements. Of the characteristics in the table, the saturation signal current and sensitivity were measured in skip mode (accumulation time $t_{int}$ = 1/60s). The saturation signal current was 24 μA, and the sensitivity was 440 nA/lx. Power consumption was measured in block mode and had low power consumption of 90 mW. This indicates a value substantially equivalent to skip mode. The dynamic range in full mode is determined by dark-current shot noise of the pixels. In full mode, the results of signal accumulation time of 0.4 s and 70 dB were obtained.

5. Summary

A 4 million-pixel CMD imaging element was developed. Fig. 10 shows a photo of the chip. Not only is drive frequency increased, but also a design was implemented for the purpose of solving the problems of frame rate in high-definition images without multi-line read-outs. Development of imaging elements that have three read-out methods was successful. The result was that by dual use of both skip mode and block mode, the overall rough image of high-definition images and a portion of the image can be confirmed in a video.

Table I Specifications and performance of the CMD image senser.

| | |
|---|---|
| Pixel size | 7.5 μm(H)× 7.5 μm(V) |
| Number of effective pixel | 2048(H)×2048(V) |
| Image area | 15.36 mm(H)×15.36 mm(V) |
| Chip size | 20.0 mm(H)×20.0 mm(V) |
| Output channel | Single |
| I/O pins | 35 pins |
| Readout mode | Full/Skip/Block |
| Saturation Signal | 24 μA |
| Sensitivity | 440 nA/lx ($t_{int}$=1/60 s) |
| Blooming level | -110 dB (V/10 exposure,Block mode) |
| Power dissipation | 90 mW (Block/Skip) |
| H limiting resolution | 2000 TV lines |
| V limiting resolution | 2000 TV lines |
| Dynamic Range | 70 dB (Full mode) |
| Frame rate (@12MHz) | 2 fps (Full mode) 30 fps (Skip mode) variable (Block mode) |

The Institute of Image Information and Television Engineers

March 14, 1997 (Fri.) The Institute of Image Information and Television Engineers Report ITE Technical Report Vol. 21. No. 21, PP. 7-42

IPU '97-15, CE' 97-7 (Mar, 1997)

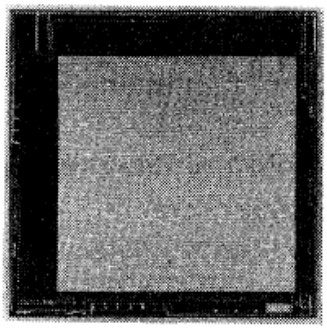


Fig. 10 CMD image sensor micrograph.

Also, to avoid a drop in image quality that accompanies the generation of a dark charge during exposure in full mode, a low-dark current drive was developed. By adopting this drive method, an amount of suppression of 30% of a dark charge compared to the same accumulation time was confirmed.

The functionality above was satisfied, and despite multiple pixels, low power consumption of 90 mW was attained.

A scanning system for observing in high resolution a large target object on an electronic still camera or a liquid-crystal panel that can confirm in real-time on a monitor focal adjustments and framing can be implemented without using a mechanical scanning mechanism, by utilizing these features using these imaging elements. These imaging elements can implement the complex image cropping processes like those conventionally implemented outside of the imaging elements and it is thought that this is extremely useful as an input device for electronic still cameras and scanning systems.

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2) S. G. Chamberlain et al., "Mega Pixel CCD Image Sensor Technology," *IEEE Proceedings IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, April 1995.

3) Kazuya MATSUMOTO, "CMD Image ch" Shizuoka Univer[illegible]ity pp.43-47, Nov., 1996

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Microcomponent Engineering Dept.
6666 Inatomi, Tatsuno-Cho, Kamiina-Gun, Nagano Prefecture, 399-04
Tel: 0266-41-4179 Fax: 0266-41-4868

US005668597A

# United States Patent [19]

Parulski et al.

[11] Patent Number: 5,668,597

[45] Date of Patent: Sep. 16, 1997

[54] **ELECTRONIC CAMERA WITH RAPID AUTOMATIC FOCUS OF AN IMAGE UPON A PROGRESSIVE SCAN IMAGE SENSOR**

[75] Inventors: **Kenneth A. Parulski**, Rochester, N.Y.; **Masaki Izumi**, Yokohama, Japan; **Seiichi Mizukoshi**, Chigasaki, Japan; **Nobuyuki Mori**, Setagaya-ku, Japan

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **367,404**

[22] Filed: **Dec. 30, 1994**

[51] **Int. Cl.**[6] ..... **H04N 5/232**

[52] **U.S. Cl.** ..... **348/350**; 348/315; 348/353

[58] **Field of Search** ..... 348/311, 312, 348/314, 315, 316, 317, 322, 323, 345, 349, 350, 362, 363, 364; 354/400, 402, 403; H04N 5/232

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| 0 421 243 A2 | 9/1990 | European Pat. Off. | H04N 5/232 |
| 62-094084 | 4/1987 | Japan | H04N 5/335 |
| 1303975 | 12/1989 | Japan | H04N 5/335 |

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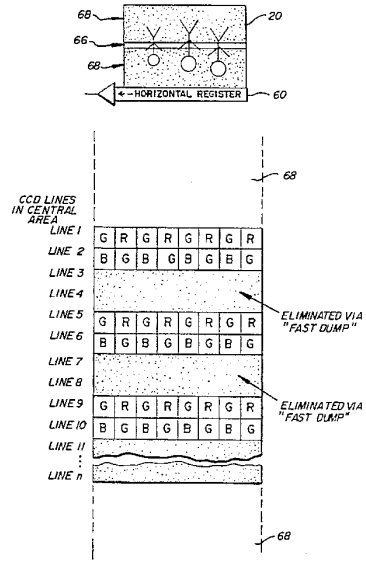
"KAI-0310 648(H)×484(V) Pixel Interline CCD Image Sensor Performance Specification", Eastman Kodak Company, Revised Apr. 26, 1994.

*Primary Examiner*—Thai Tran
*Assistant Examiner*—Ngoc-Yen Vu
*Attorney, Agent, or Firm*—David M. Woods

[57] **ABSTRACT**

A technique for automatically focusing the lens of an electronic still camera employs a progressive scan image sensor **20** with a fast dump structure **62**. The image sensor **20** itself is operated first in a "fast flush " mode to focus a lens **22**, and then in a normal readout mode to obtain the final still image. To focus the lens **22**, an image is integrated on the sensor **20**. The average contrast of a central region **66** of the image is used to determine how well the image is focused. The portion of the image surrounding a central focusing area **66** is rapidly read out and discarded, using "fast flush" clocking where the vertical and horizontal registers are continuously clocked and lines of image charge are dumped to the substrate through the fast dump structure **62**. In the central focusing area **66**, a pattern of lines are eliminated through the fast dump structure **62**, and the intervening lines are transferred out to generate a focus adjustment signal. The process is repeated numerous times as the lens focus is adjusted until the maximum average contrast is obtained. At this point, the entire sensor is cleared using "fast flush" clocking, and the final image is then captured and read out.

**19 Claims, 10 Drawing Sheets**



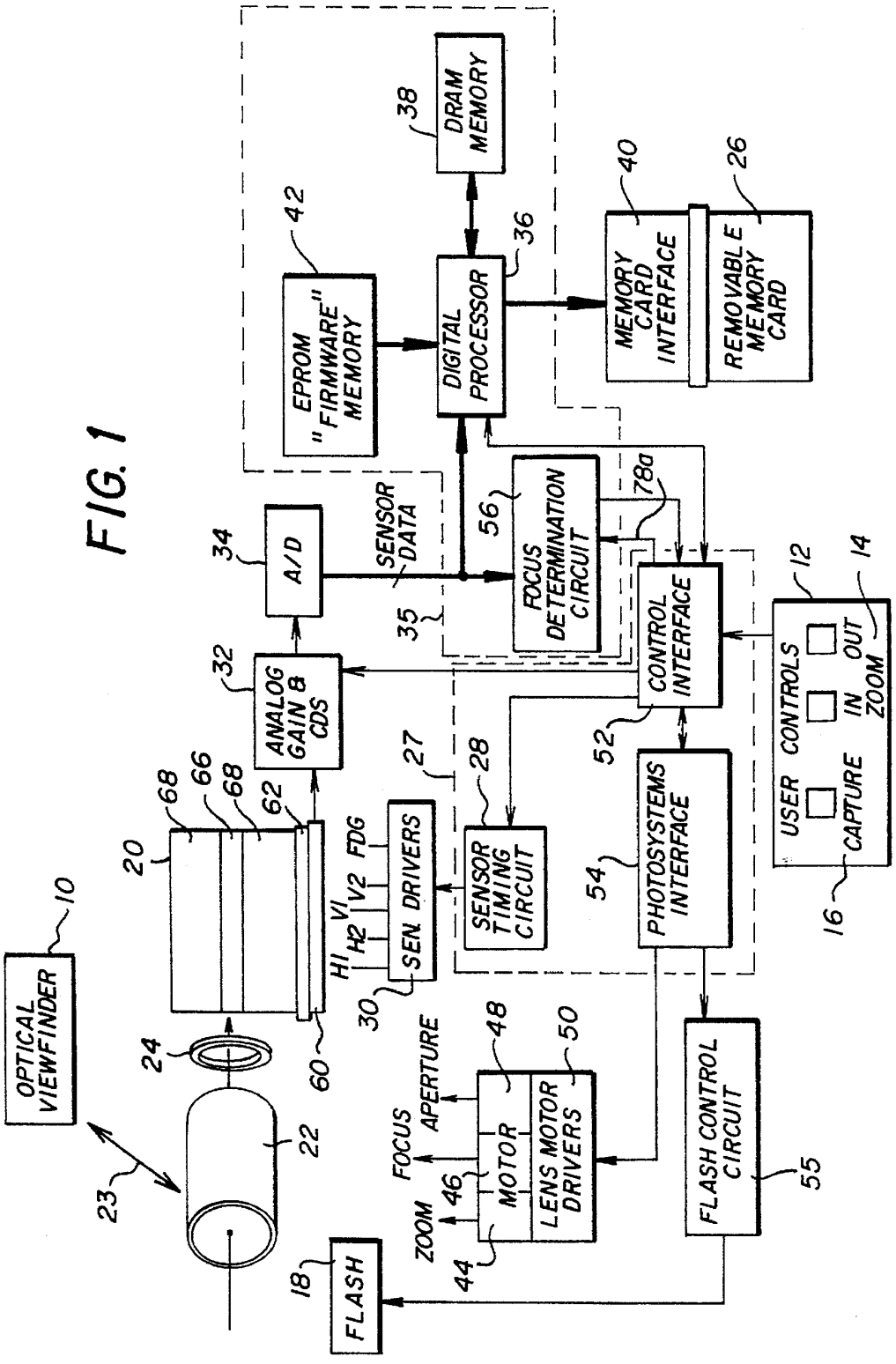

DRAM MEMORY
38
EPROM "FIRMWARE" MEMORY
42
DIGITAL PROCESSOR
36
MEMORY CARD INTERFACE
40
REMOVABLE MEMORY CARD
26
A/D
34
SENSOR DATA
FOCUS DETERMINATION CIRCUIT
56
78a
35
CONTROL INTERFACE
52
USER CONTROLS
IN
OUT
ZOOM
CAPTURE
12
14
16
ANALOG GAIN & CDS
32
SEN DRIVERS
30
SENSOR TIMING CIRCUIT
28
27
PHOTOSYSTEMS INTERFACE
54
OPTICAL VIEWFINDER
10
20
68
66
68
62
FDG
V2
V1
H2
H1
60
24
22
23
APERTURE
FOCUS
ZOOM
48
50
46
44
MOTOR
LENS MOTOR DRIVERS
FLASH
18
FLASH CONTROL CIRCUIT
55

FIG. 1

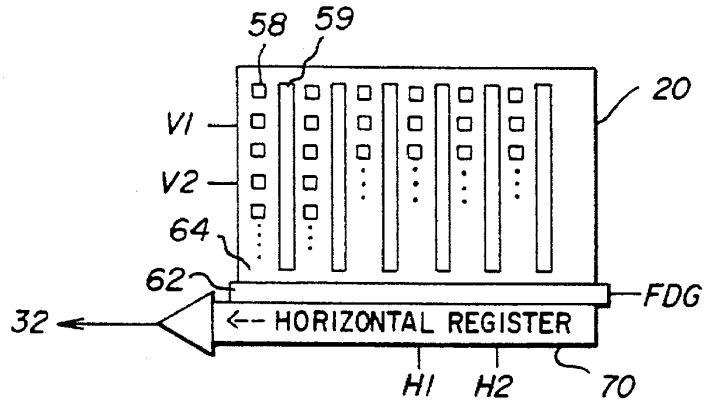
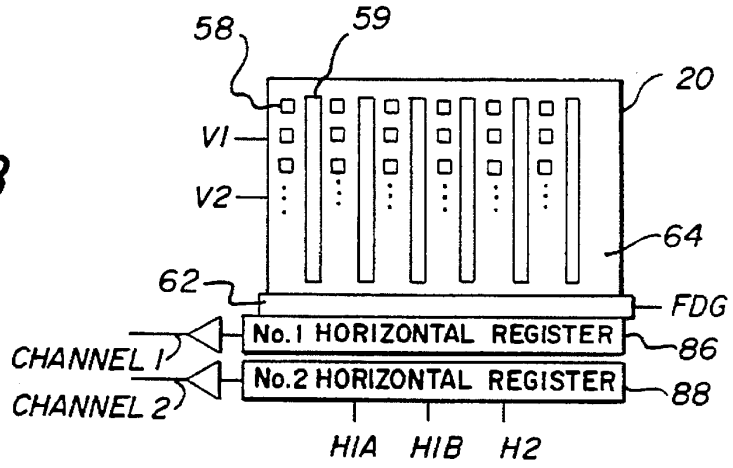



FIG. 2A

FIG. 2B




CCD LINES

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LINE 1 | G | R | G | R | G | R | G | R |
| LINE 2 | B | G | B | G | B | G | B | G |
| LINE 3 | G | R | G | R | G | R | G | R |
| LINE 4 | B | G | B | G | B | G | B | G |
| LINE 5 | G | R | G | R | G | R | G | R |
| LINE 6 | B | G | B | G | B | G | B | G |
| LINE 7 | G | R | G | R | G | R | G | R |
| LINE 8 | B | G | B | G | B | G | B | G |

FIG. 3

FIG. 4

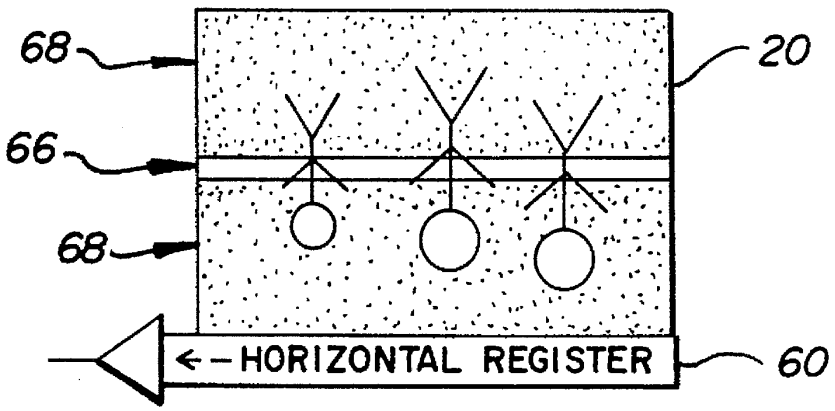
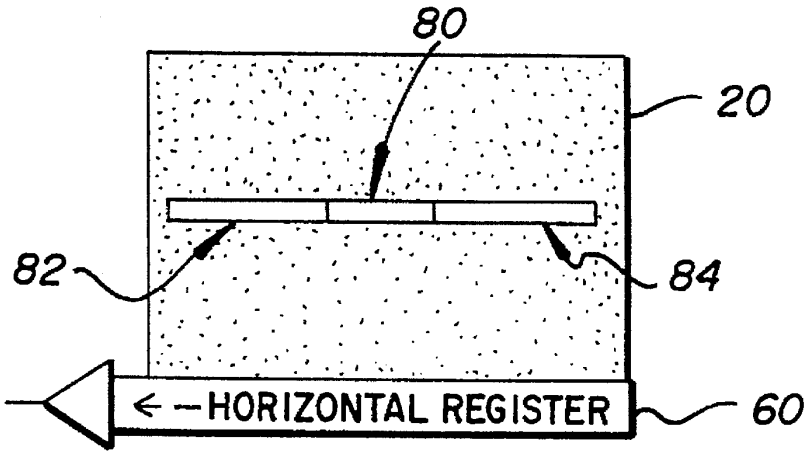

68
66
68
20
HORIZONTAL REGISTER
60

FIG. 5


80
20
82
84
HORIZONTAL REGISTER
60

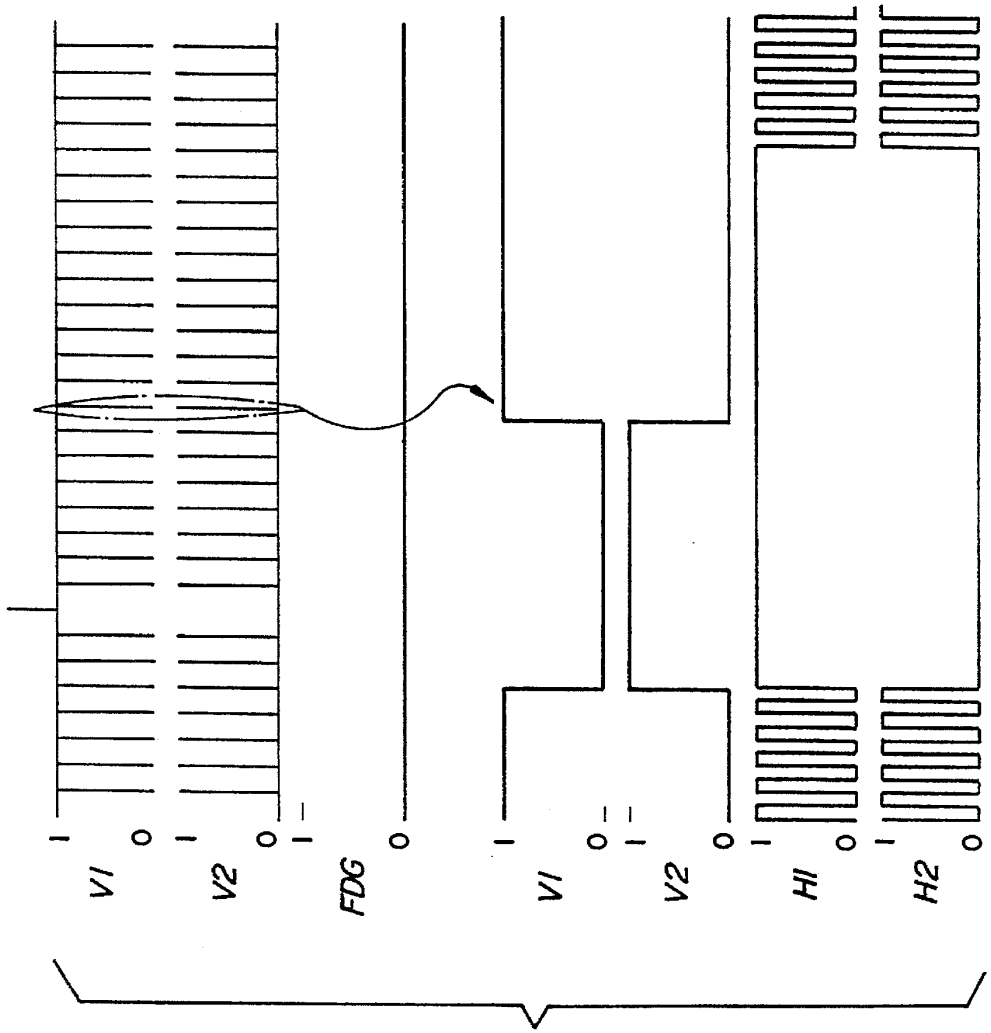



FIG.6

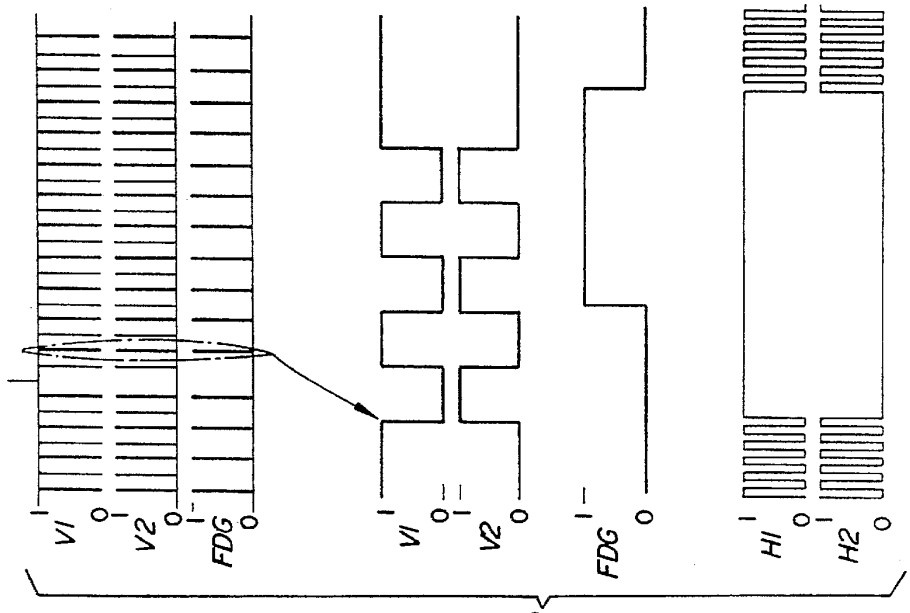



FIG.7B

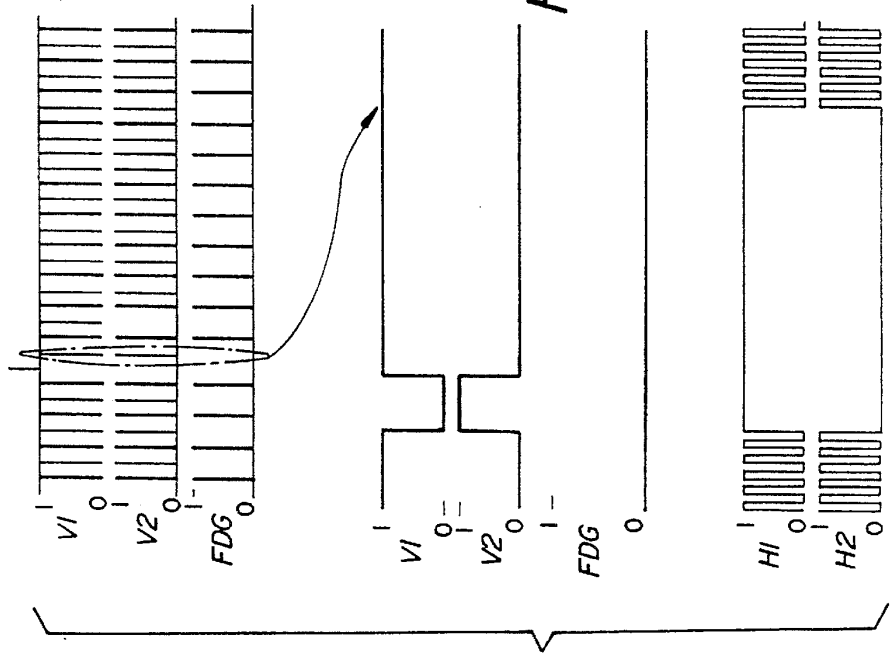



FIG.7A

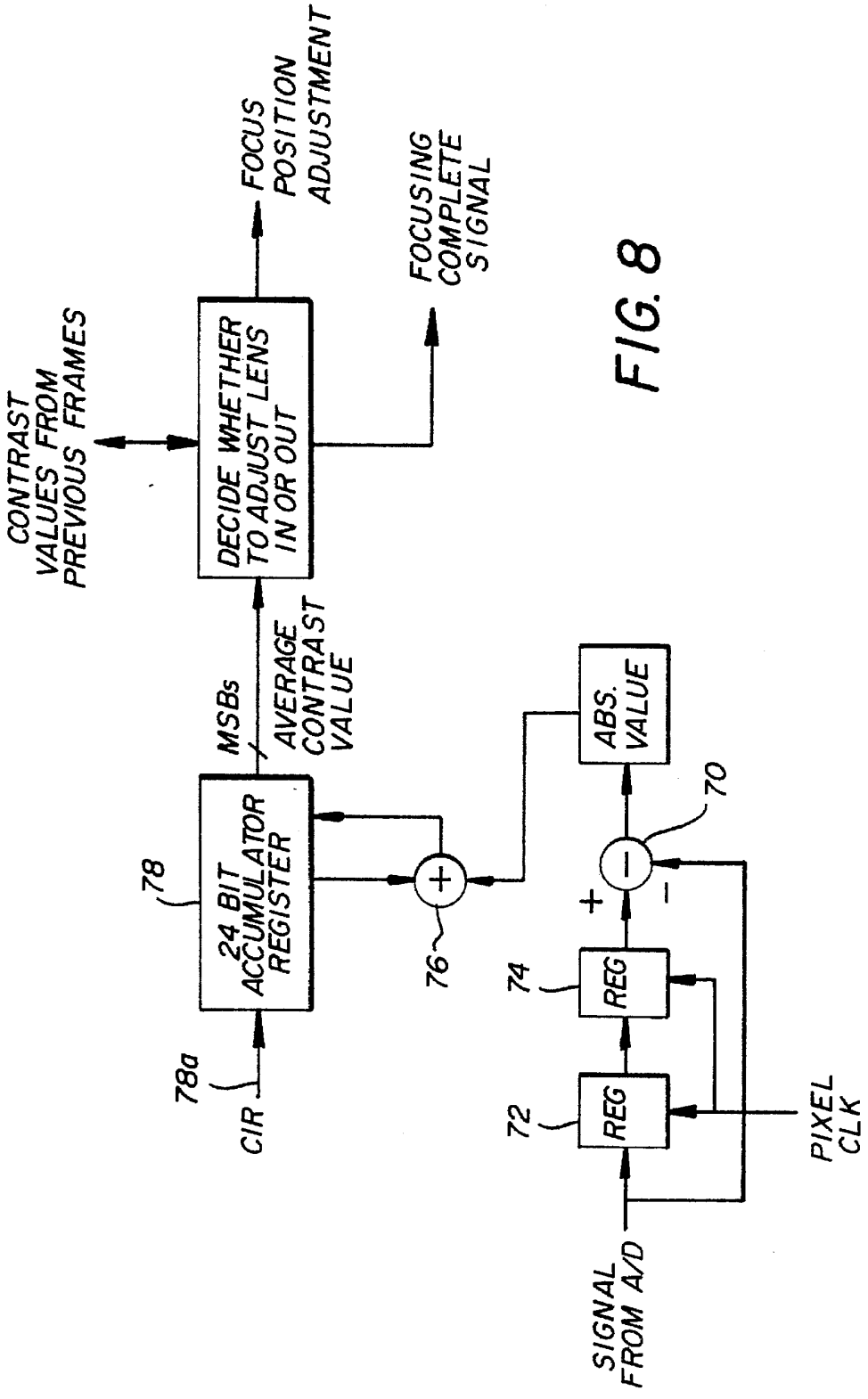

FOCUS POSITION ADJUSTMENT
FOCUSING COMPLETE SIGNAL
CONTRAST VALUES FROM PREVIOUS FRAMES
DECIDE WHETHER TO ADJUST LENS IN OR OUT
MSBs
AVERAGE CONTRAST VALUE
24 BIT ACCUMULATOR REGISTER
78
78a
CIR
76
ABS. VALUE
70
74
REG
72
REG
PIXEL CLK
SIGNAL FROM A/D

FIG. 8

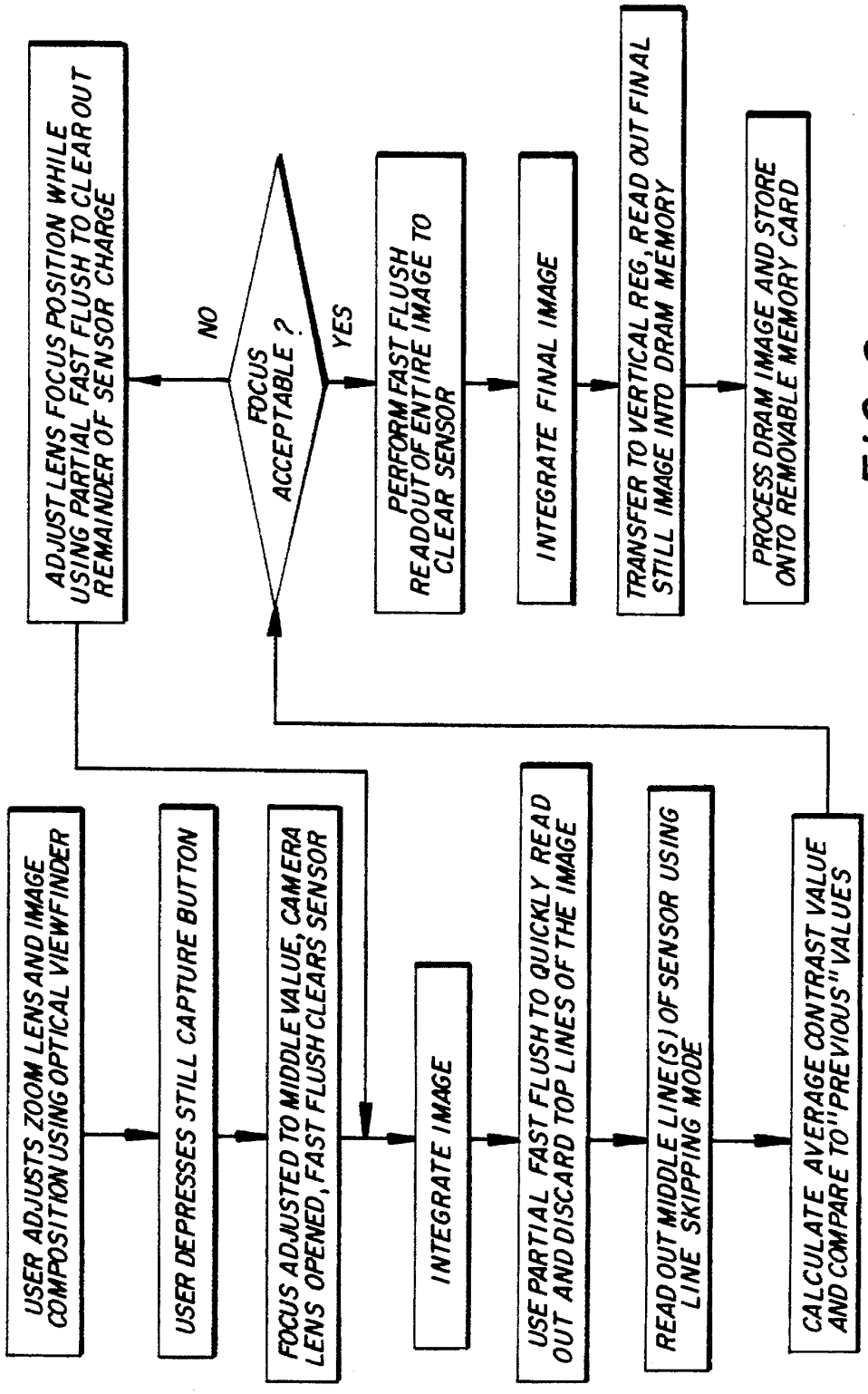

USER ADJUSTS ZOOM LENS AND IMAGE COMPOSITION USING OPTICAL VIEWFINDER
USER DEPRESSES STILL CAPTURE BUTTON
FOCUS ADJUSTED TO MIDDLE VALUE, CAMERA LENS OPENED, FAST FLUSH CLEARS SENSOR
INTEGRATE IMAGE
USE PARTIAL FAST FLUSH TO QUICKLY READ OUT AND DISCARD TOP LINES OF THE IMAGE
READ OUT MIDDLE LINE(S) OF SENSOR USING LINE SKIPPING MODE
CALCULATE AVERAGE CONTRAST VALUE AND COMPARE TO "PREVIOUS" VALUES
FOCUS ACCEPTABLE ?
NO
YES
ADJUST LENS FOCUS POSITION WHILE USING PARTIAL FAST FLUSH TO CLEAR OUT REMAINDER OF SENSOR CHARGE
PERFORM FAST FLUSH READOUT OF ENTIRE IMAGE TO CLEAR SENSOR
INTEGRATE FINAL IMAGE
TRANSFER TO VERTICAL REG, READ OUT FINAL STILL IMAGE INTO DRAM MEMORY
PROCESS DRAM IMAGE AND STORE ONTO REMOVABLE MEMORY CARD

FIG. 9

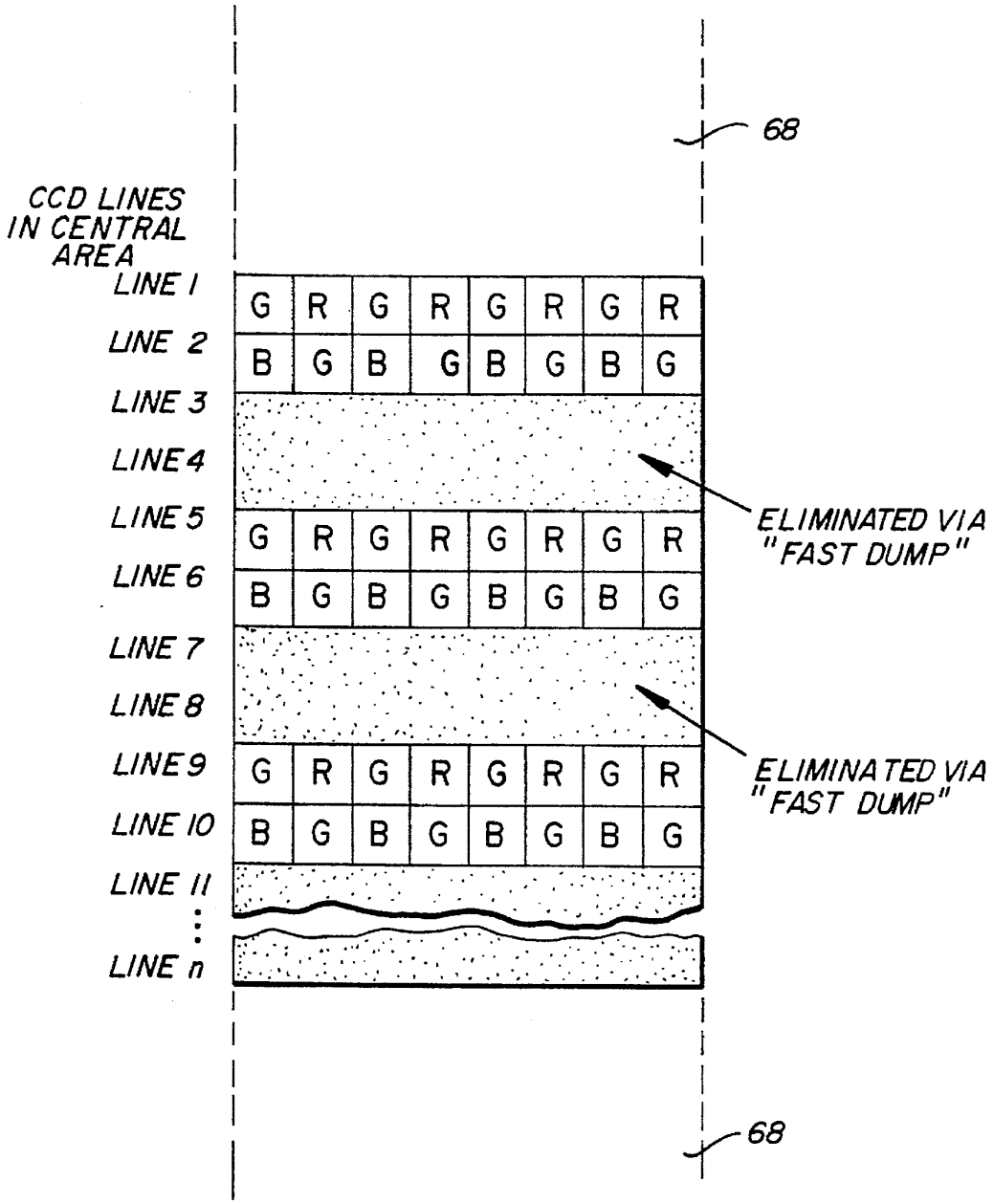
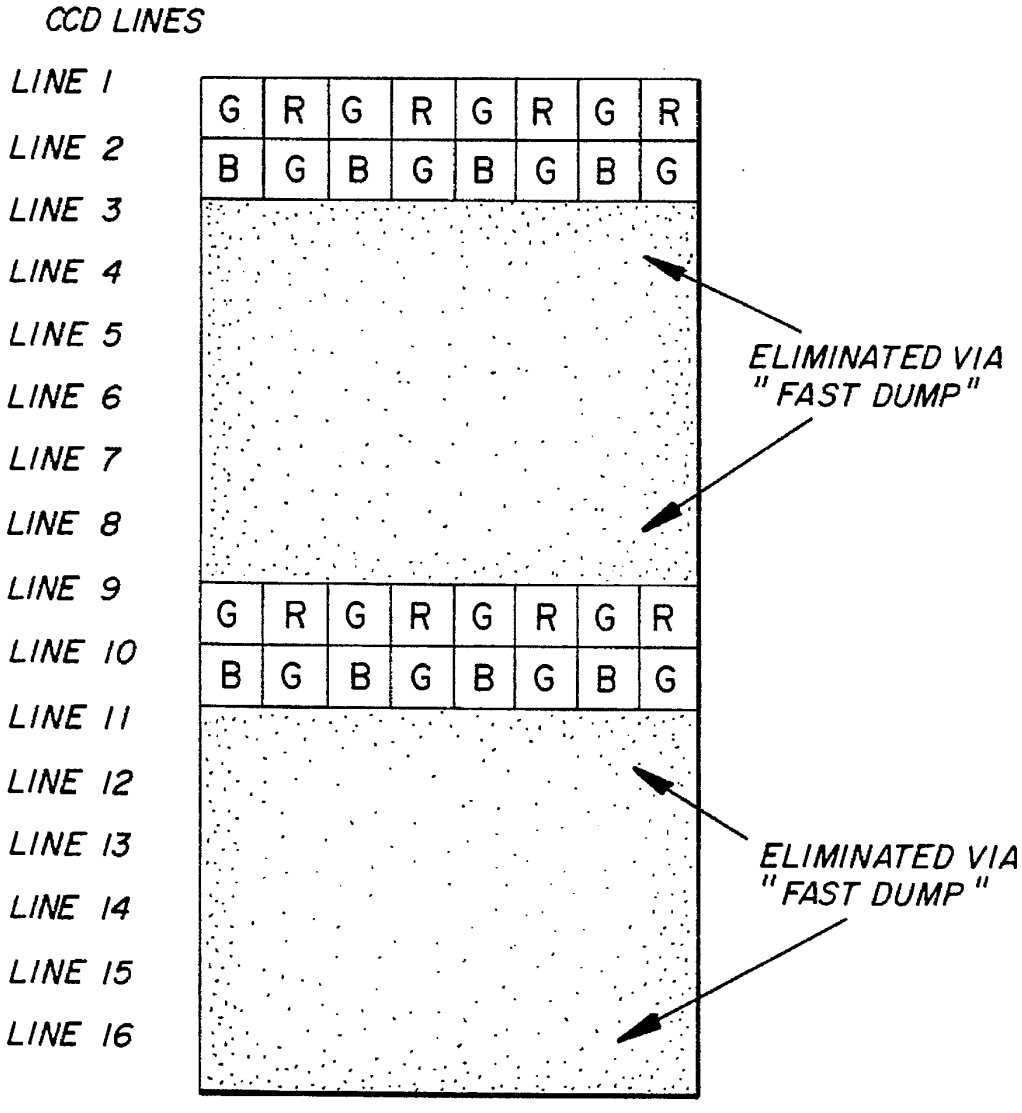

68
CCD LINES IN CENTRAL AREA
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE n
G R G R G R G R
B G B G B G B G
ELIMINATED VIA "FAST DUMP"
ELIMINATED VIA "FAST DUMP"
68

FIG. 10

FIG. 11


CCD LINES
LINE 1
LINE 2
LINE 3
LINE 4
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LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE 12
LINE 13
LINE 14
LINE 15
LINE 16
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
ELIMINATED VIA "FAST DUMP"
ELIMINATED VIA "FAST DUMP"

FIG. 12A

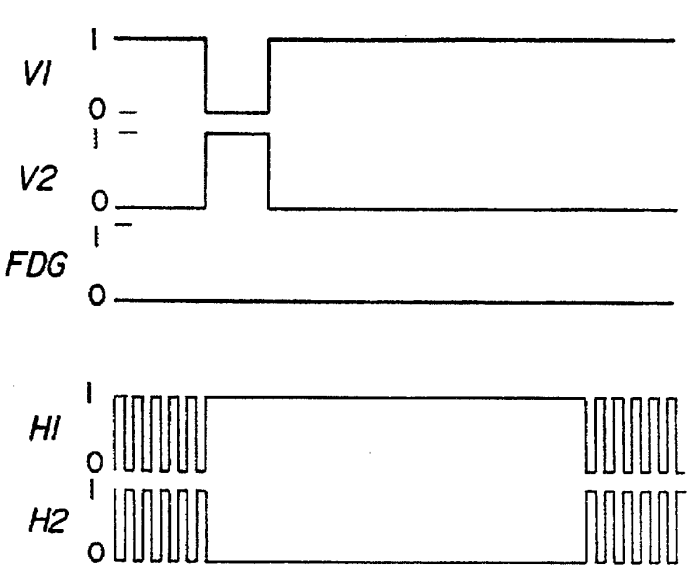
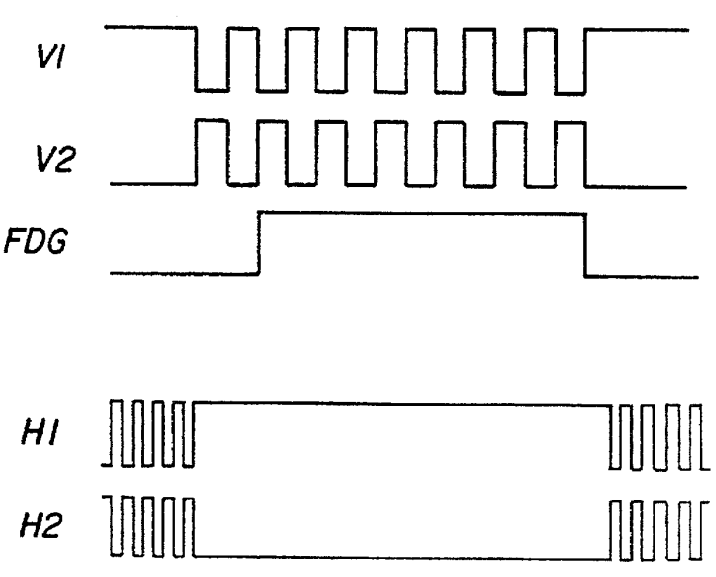



FIG. 12B



# ELECTRONIC CAMERA WITH RAPID AUTOMATIC FOCUS OF AN IMAGE UPON A PROGRESSIVE SCAN IMAGE SENSOR

## FIELD OF THE INVENTION

The invention pertains to apparatus for automatically focusing an image upon an electronic image sensor and, more particularly, for rapidly focusing an image upon a progressive scan image sensor based upon signals from a partial area of the sensor.

## BACKGROUND OF THE INVENTION

An image sensor for an electronic camera ordinarily contains a two-dimensional array of light sensitive photosites. In an interline transfer sensor, the image charge is transferred from the photosites to light-protected vertical registers, through which the image charge is moved to a horizontal readout register. On the other hand, in a full frame image sensor the image charge is incremented line-by-line through the photosites themselves to a horizontal readout register, from which the image signal is obtained. Since the full frame image sensor does not contain a separate light-protected storage area, a shutter is normally used to block the light and prevent vertical smearing when reading out the image.

An example of an electronic still camera is the model DCS 200c camera, marketed by Eastman Kodak Company, Rochester, N.Y. This camera uses a high resolution full frame image sensor in an electronic camera back which attaches to a conventional 35 mm film camera body. The camera body includes a normal focal plane shutter for blocking image light. In this type of electronic camera, a separate focus sensor is used in the camera body to automatically focus the camera lens. This extra sensor increases the camera cost. It may also result in a less than optimally focused image on the sensor, if the tolerances of the camera lens focusing mechanism, and the tolerances of the focus detector, are not tightly controlled. Therefore, by using the high resolution image sensor itself to focus the camera lens, the camera cost may be reduced, and the camera focusing accuracy may be increased.

Focusing a camera lens by using the sensor output signal is an iterative process which requires capturing a sequence of images while varying the focus, until a focus-related parameter of the image, such as the "average contrast", is maximized. Prior art camcorders typically use NTSC format interline image sensors, which do not require a mechanical shutter, to perform this type of automatic lens focusing. In these camcorders, the same image that is recorded is also analyzed to provide the focus information. Focusing is done by spatially bandpass filtering a subsection of the video image read out from the sensor. The lens focus position is adjusted to obtain the highest average magnitude output signal (highest average contrast) from the bandpass filter. Note that the camcorder's image sensor is ordinarily read out at the video field rate (1/60 second) so that the same sensor operating mode is used to provide both the focus information and the final images. In such camcorders, many images may need to be read out before the lens is properly focused. Since the image readout time is relatively rapid (approximately 1/60 second), acceptable focus can typically be achieved in less than a second.

Focus time can be further improved by application of the technique shown in U.S. Pat. No. 5,051,833 (Tsuji). This patent describes an electronic still camera in which focus is based on a rectangular subset of the pixels on an interline charge coupled device (CCD) sensor. During the focusing operation, the image lines within the rectangle are read out at the regular NTSC video rates, while the lines outside the rectangle are read out more rapidly to a charge drain on the CCD sensor. Tsuji thus describes a focusing mode which takes less time for reading out an image for the purpose of focusing than is taken for reading out an image for normal image capture. This focusing mode is employed with an interline transfer sensor, which has light-protected storage areas (vertical registers) and consequently does not require a mechanical shutter. Because the focusing image frames are not usable as captured images, this technique is not useful with camcorders. Moreover, focusing time can remain a problem if rapid utilization of the camera is desired or if longer readout times are required, such as for definitions higher than NTSC resolution.



Progressive scan image sensors having a noninterlaced architecture, such as the Kodak model KAI-0310CM imager, have been developed for high quality color electronic cameras. This sensor has approximately 480 active lines, and approximately 640 active pixels per line. A progressive scan sensor provides a higher quality still image than an interlaced sensor, since all lines are captured during the same interval of time. Unlike an interlace sensor, the progressive scan sensor allows the entire image to be read out in a single scan, albeit through light protected vertical registers as in the interline sensor. Mechanical shuttering, therefore, is unnecessary for exposure control (and to prevent vertical smear) as the function can be performed electronically.

For a high quality still mode, the progressive scan sensor can be read out at slower than video rates without sacrificing performance, since real-time operation is not required. If, however, the image is read out in the same period of time as from an interlaced image sensor, readout timing from a progressive scan image sensor normally requires a clock rate of approximately twice that used with the interlaced image sensor. Such timing would be required, for instance, for an electronic viewfinder or for the rapid acquisition of image data, such as for autofocus determination. For example, an NTSC format interlaced image sensor with 480 lines and 640 pixels per line requires a clock rate of approximately 12 MHz to read out the 640 lines in the 52.4 mSec NTSC standard active line time, which provides a field rate of 1/60 second. Since a progressive scan sensor, like the model KAI-310 imager, must read out twice as many lines per field, it must use a clock rate of about 24 mHz to read out all 480 lines in 1/60 second. This higher clock rate requires more expensive clock drivers, analog processing, and A/D conversion than interlaced sensors require. Such high speed, and thus high cost, components are required for autofocus processing within the focusing area even though, as in Tsuji, the lines above and below the focusing area are not used.

This leads to the anomalous situation that a non-imaging part of the system, the autofocus processing, requires the higher clock rate, and thus the higher cost parts—clock drivers, analog processing, A/D converters, etc.—than the high resolution imaging part itself. What is needed is a technique for reading out the image sensor data within the focusing area in a manner that decreases the required clock rate while enabling rapid focus of the lens of an electronic camera.

## SUMMARY OF THE INVENTION

In arriving at the invention, it was first realized that quick dumping of some parts of the image, even within the

focusing area itself, could solve the clocking problem and still leave enough information in the remaining part of the focusing area that the remaining lines of the image could be used for focus evaluation. The problems noted above are then solved according to the invention by basing focus evaluation on a subset of the image lines within the focusing area of the image. More particularly, an electronic camera having an automatically focused lens that is operable to focus an image based on image data electronically obtained by the camera from a partial area of the whole image includes an image sensor comprising a two-dimensional array of photosites arranged in lines and columns to provide image charge, the sensor having the capacity to eliminate some lines of image charge and to transfer other lines of image charge. The camera further includes a timing and control section for controlling the sensor so as to eliminate a pattern of lines of image charge from the partial area utilized for autofocus and to transfer the intervening lines of image charge within the partial area, and a processor for generating a focus adjustment signal based on the intervening lines of image charge transferred from the partial area.

Unlike the application of conventional camcorder automatic focusing techniques to interline sensors, which would take several seconds with a progressive scan architecture to bring the lens into focus, the advantage of the invention is that the entire focusing sequence occurs rapidly, taking only a fraction of a second. Furthermore, high speed requirements are avoided by dropping lines of image charge within the partial area that is used for autofocus evaluation.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, wherein

FIG. **1** is a block diagram of an electronic camera incorporating the invention in connection with a progressive scan image sensor;

FIGS. **2**A and **2**B are diagrams of progressive scan image sensors useful with the camera of FIG. **1**;

FIG. **3** is a diagram of the Bayer color filter geometry for the sensor used with the camera of FIG. **1**;

FIG. **4** is a diagram of the imaging portion of a sensor showing a central focusing area;

FIG. **5** is a diagram of the imaging portion of a sensor showing a central focusing area divided into regions;

FIG. **6** shows the line timing for the still imaging mode of operation;

FIGS. **7**A and **7**B show the line timing for the autofocus mode of operation;

FIG. **8** is a block diagram of a focus determination circuit used in the camera of FIG. **1**;

FIG. **9** is a flowchart showing the sequence of operations of the camera of FIG. **1**;

FIG. **10** shows a first embodiment of a line-skipping pattern, especially for the central focusing area shown in FIG. **4**;

FIG. **11** shows a second embodiment of a line-skipping pattern for the central focusing area; and

FIGS. **12**A and **12**B shows the line timing for the pattern shown in FIG. **11**.

## DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

A block diagram of a camera using an automatic focus apparatus incorporated into a progressive scan architecture according to the invention is shown in FIG. **1**. The camera includes an optical viewfinder **10** and a user control section **12** having a number of user control buttons, including zoom buttons **14** and a capture button **16**. To take a still picture, the user turns on the camera (using a power switch (not shown), which may be automatically enabled when the user depresses the zoom buttons **14** or partially depresses the capture button **16**). The user composes the picture by depressing the "zoom in" or "zoom out" buttons **14**, and by adjusting the position of the camera, while observing the viewfinder image. When the user is satisfied with the composition, the user depresses the capture button **16**. The camera then captures a single still image, firing a flash **18** if necessary when the ambient illumination level is low. The still image is focused upon an image sensor **20** by a motor driven zoom lens **22**, which is interconnected with the viewfinder **10** by a mechanical coupling **23**. The intensity of the image light upon the sensor **20** is regulated by a motor driven mechanical aperture **24** while exposure time is regulated electronically by appropriate clocking of the sensor **20**. The still image from the image sensor **20** is processed and digitally stored on a removable memory card **26**.

Control of the sensor **20** is provided by a timing and control section **27**, which specifically includes a sensor timing circuit **28**. The sensor timing circuit **28** provides the signals to enable sensor drivers **30**, which provides horizontal clocks (H1, H2) and vertical clocks (V1, V2), as well as a signal FDG for activating a drain structure on the sensor **20**. The output of the image sensor **20** is amplified and processed in an analog gain and sampling (correlated double sampling (CDS)) circuit **32**, and converted to digital form in A/D converter **34**. The A/D output signal is provided to a processor section **35**, which includes a digital processor **36** which temporarily stores the still images in a DRAM memory **38**. The digital processor **36** then perform image processing on the still images, and finally stores the processed images on the removable memory card **26** via a memory card interface circuit **40**, which may use the PCMCIA 2.0 standard interface. An EPROM memory **42** is used to store the firmware which operates the digital processor **36**.

The motor driven zoom lens **22** includes a zoom motor **44**, a focus motor **46**, and an aperture motor **48** (all controlled by lens motor drivers **50**). The timing and control section **27** further includes a control interface **52** connected to the lens motor drivers **50** and to a flash control circuit **55** via a photosystem interface block **54**, which controls the operation of the zoom lens **22** and the flash **18**. The lens zoom position is controlled by the photosystem interface block **54** based on the position input from the zoom control buttons **14**. The focus is set by the control interface **52** using a focus adjustment signal output by a focus determination circuit **56** within the processor section **35**. The focus determination circuit **56** processes data from the A/D converter **34** according to a focusing algorithm (which will be described in connection with FIG. **8**) applied to a selected partial area of the image sensor **20** as the sensor is operated in the focus mode. An iterative algorithm in the control interface **52** adjusts the lens focus position, depending on the output of the focus determination circuit **56**, until the focus determination process provides a maximum contrast signal. Although the digital processor **36** and the control interface **52** are shown as two separate blocks, in some implementations the same processor could be used to perform both of these functions. Other of the recited functions, such as focus determination, could also be functionally part of one of the processors.

The sensor **20** is a progressive scan interline image sensor having a noninterlaced architecture, as shown in more detail

in FIG. 2A. The sensor comprises a two-dimensional array of photosites **58**, e.g. photodiodes, arranged in rows (lines) and columns, a plurality of vertical registers **59** adjacent photosite columns for transferring rows (lines) of image charge from the photosites **58** to a horizontal register **60** for readout, and a charge drain (specifically, a fast dump structure **62**) interposed between the output of the vertical registers **59** and the horizontal register **60** for eliminating complete rows (lines) of image charge at a time from the image sensor **20** by discharge to a sensor substrate **64**. A preferred image sensor is the Kodak model KAI-0310CM CCD image sensor, which has approximately 480 active lines with approximately 640 active pixels per line and an image aspect ratio of 4:3. This sensor is described in a Performance Specification document available from Eastman Kodak Company, Rochester, N.Y. Each pixel is 9 microns "square", since both the vertical and horizontal distances between the centers of adjacent pixels are 9 microns. The sensor uses a color filter array pattern known as the "Bayer checkerboard" pattern, described in U.S. Pat. No. 3,971,065, which is shown in FIG. **3**. Such a color filter array is characterized by a mosaic pattern in which the filter colors alternate in both line and column directions.

The sensor **20** uses a progressive scan readout method, which allows the entire image to be read out in a single scan. In this operating mode, all of the pixels on the sensor are transferred to the horizontal register **60**, which delivers the image signals to the analog gain and CDS circuit **32** (see FIG. **1**). More specifically, referring to FIG. **2**A, the accumulated or integrated charge for the photodiodes comprising the photosites **58** is transported from the photosites to light protected vertical (parallel) registers **59** by applying a large positive voltage to the phase-one vertical clock (V1). This reads out every row, or line, into the vertical registers **59**. The charge is then transported from the vertical registers **59** to the horizontal register **60** by two-phase clocking of the vertical clocks (V1, V2). Between the vertical and horizontal registers is the fast dump structure **62**, which is further described in the Performance Specification document for the KAI-310 sensor. By setting a suitable positive potential on a fast dump gate line FDG, charge from the row (line) of pixel values currently adjacent to the fast dump structure **62** is transferred from the CCD channel directly into the sensor substrate **64** rather than to the horizontal register **60**. This dump, or line clear, is accomplished during the vertical-to-horizontal transfer time. When properly controlled by the sensor timing circuit **28**, the fast dump structure **62** allows lines of charge to be eliminated. (A conventional use of the gate **62** is to eliminate stray charge in the vertical registers **59** during especially long integration times, and just before transfer of image charge to the vertical registers **59**. The gate **62** may also be used to eliminate unwanted non-image lines above and below the **20** image.)

FIG. **4** shows a representative portion of the image sensor **20** which provides the data used to focus the image in the focusing operating mode. Only a small number of lines in a central focusing area **66** of the image are used to provide the focus determination input data. For the progressive scan sensor, the other lines in the outer area **68** are quickly read from the image by continuously holding the fast dump structure **62** at a high positive potential, as the vertical clocks are cycled high and low to transfer lines of charge to the substrate via the fast dump drain. Since the image charge for the non-used lines are quickly flushed from the sensor, this operation is referred to as a "fast flush" and the focus mode is thus described as a fast flush focus mode. The time required to read out the image in the fast flush focus mode is well under 10 mSec. Although it may take **10** iterative cycles for proper focus in some cases, acceptable focus can still be achieved in a fraction of a second. Moreover, as will be described, dropping lines within the central focusing area **66** allows even more "images" to be captured per unit time (i.e., more iterative cycles or image "updates"). If more image updates can be obtained in a given period of time, then autofocus can be achieved more rapidly for the same size central focusing area **66** as would be used in the prior art. Alternatively, if the existing update rate is satisfactory, the central focusing area **66** can be enlarged in the vertical direction without decreasing the update rate obtained in the prior art. A larger central focusing area **66** may be useful in focusing on a more appropriate area of the sensor **20**.

The timing and control section **27** operates the electronic camera shown in FIG. **1** in two modes, including a first imaging mode wherein all rows of signal charge corresponding to each line are progressively read out through the horizontal register **60** during a single scan, and a second autofocus mode wherein some of the rows of signal charge corresponding to some lines are eliminated through the fast dump structure **62** prior to readout. As applied to the embodiment of FIG. **1**, the first mode corresponds to a high quality still imaging mode while the second mode corresponds to a focusing mode for providing central lines of image data to the focus determination circuit **56**. In the autofocus mode, the timing and control section **27** controls the fast dump structure **62** to A) eliminate all lines of image charge in the outer area **68** (FIG. **4**) outside the central focusing area **66**, and B) eliminate at least one line of image charge from the image sensor **20** for every one or more lines of image charge that are transferred to the horizontal register **60** for readout from the central focusing area **66**.

The sensor timing circuit **28** is controlled by the control interface **52** to provide the clock signals V1, V2, H1, H2, and the gate signal FDG according to the two modes of operation. The timing signals for the first mode are shown in FIG. **6**; those for the second mode are shown in FIGS. **7**A and **7**B. The two-phase cycling of signals V1 and V2 control the transfer of lines of image charge from the vertical registers **59** to the horizontal register **60**. The two-phase cycling of signals H1 and H2 control the transfer of pixels from the horizontal register **60** to subsequent circuits in the camera. The level of the signal FDG determines whether the image charge is dumped to the substrate **64** or transferred to the horizontal register **60**. When the sensor **20** is clocked using the first timing mode shown in FIG. **6**, all lines of the sensor are clocked out, one after the other, through the horizontal register **60**, processed in subsequent camera circuitry, and stored in the removable memory **26**. This timing mode provides a high quality progressive scan still image, but may take 1/30 second or longer to read out the still image. Such timing, however, is acceptable for still mode usage, and, as mentioned before, does not require unusually high speed components.

To provide focusing data to the focus determination circuit **56**, a lower resolution image was found to be suitable. The update rate must be sufficient to provide good focus detection. An update rate of 60 fields/sec is appropriate. Moreover, the sensor **20** includes the aforementioned array of color filters arranged in a particular color pattern (e.g., the checkerboard Bayer pattern of FIG. **3**), and the lines of image charge that are transferred to the horizontal register **60** should preserve that particular color pattern in the pattern of lines that are generated, if only for ease of subsequent processing. To provide this kind of focusing image, a pattern of lines in the central focusing area **66** of the sensor **20** is

eliminated in the autofocus mode, and the intervening lines are transferred to the horizontal register **60**, using the timing shown in FIG. **7B**. The line-skipping pattern for the central focusing area **66** is shown in FIG. **10**. The first two lines (**1** and **2**) are read out as in the imaging mode. These provide a green-red and a blue-green line. The next two lines (**3** and **4**)a are eliminated by turning on the fast dump structure **62** during the time that these lines are transferred past the fast dump structure **62**. Next, lines **5** and **6** are read out normally, and then lines **7** and **8** are eliminated through the fast dump structure **62**. This process proceeds through the central area **66** and generates an output image signal having the Bayer-type color filter repeating pattern, so that the signals can be processed using algorithms designed for the Bayer pattern. More specifically as to waveforms, in the area **68** surrounding the central focusing area **66**, the vertical clocks are cycled continuously with the fast dump gate FDG held high. This dumps all lines of image charge for the outer area **68** into the sensor substrate **64**. FIGS. **7A** and **7B** shows the clock waveforms for the vertical and horizontal clocks V1, V2, H1, H2 and the fast dump gate FDG for the central focusing area **66**. For each saved pair of lines (i.e., lines **1** and **2**, **5** and **6**, etc.) that is read out as in the imaging mode, another pair of lines (i.e., lines **3** and **4**, **7** and **8**, etc.) is eliminated by turning on the fast dump structure **62** during the time that this line pair is transferred past the fast dump structure **62**. The first line of each saved pair is transferred to the horizontal register **60** and read out according to the timing diagram shown in FIG. **7A**. The second line of each saved pair is transferred to the horizontal register **60**, and the succeeding pair of two lines are dumped through the fast dump structure **62**, according to the timing diagram shown in FIG. **7B**. The continuation of the sequence of this readout timing achieves readout of the central focusing area **66**. This results in a line-skipping sequence of dumping alternate line pairs, and saving intervening line pairs.

A second embodiment of line skipping in the central area **66** is shown in FIG. **11**. Basically, six lines are dumped for each two lines that are read out, thus preserving the Bayer-type pattern in the readout signal while gaining further advantage in processing time. To provide this kind of focusing image, the area **68** outside the central area **66** continues to be read out by continuously cycling the vertical clocks with the fast dump gate FDG held high. Within the central area **66**, the timing is shown in the waveforms of FIGS. **12A** and **12B**. The first two lines (**1** and **2**) are read out as in the imaging mode. These provide a green-red and a blue-green line. The next six lines (**3–8**) are eliminated by turning on the fast dump structure **62** during the time that these are transferred past the fast dump structure **62**—and so on in sequence (save two lines, dump six lines, save two, dump six, etc.) with **20** the remainder of the lines. As was explained in relation to FIGS. **7A** and **7B**, the first line of each saved pair is transferred according to the timing of FIG. **12A**, and the second line of each saved pair, as well as the six lines that are dumped, are processed according to the timing of FIG. **12B**.

Although the color filter array pattern has been preserved by saving pairs of lines, and then dumping integral numbers of pairs of lines, the pattern may also be preserved by saving single lines and dumping an appropriate number of lines, e.g., save one line and dump seven lines. Moreover, the invention should not be considered limited to a specific color filter array pattern or to any particular line-skipping sequence. Indeed, it is not strictly necessary to preserve the color filter array pattern in order to obtain image data useful for autofocus determination. Nor must lines be dumped in pairs, or in multiples of pairs. The advantage of the invention as broadly understood, namely to reduce the amount of data that must be handled from the central focusing area **66**, can be obtained by dumping any number or pattern of lines irrespective of the color filter array geometry.

FIG. **8** shows the focus determination circuit. This circuit measures the "average contrast" (high frequency detail) of a portion of the image. The high frequency detail is obtained by a subtractor **70**, which subtracts the value of the current input pixel output by the A/D converter **34** from the value of the A/D output delayed by two pixels, via two registers **72** and **74**. The two register delay is used instead of a single register, since the horizontal color filter pattern along the line repeats every two pixels. This ensures that similarly colored pixels are subtracted. The output of the subtractor is zero when the values of the two pixels are identical. The magnitude of the subtractor output increases as the difference between pixel values increases. This subtractor output will be large near vertically oriented edges if the camera lens is well focused, but smaller near these same edges if the camera lens is not well focused. The absolute value of the subtractor output is combined in a summer **76** with an accumulated value from an accumulator register **78**. This accumulated value is the average contrast value. A single average contrast value may be computed, for example, for the central area **66** shown in FIG. **4**. In this instance, an accumulator clock input **78***a* (provided by the control interface processor **52**) would be enabled for all pixels in the central area **66** shown in FIG. **4**, and disabled for any pixels outside this area. In any event, the accumulated average contrast value is the focus adjustment signal that is used by the control interface **52** and the photosystems interface **54** in the adjustment of the lens **22**. Alternately, the circuit in FIG. **8** could be modified to include multiple accumulators to store the average contrast for multiple regions in the image. For example, the average contrast could be computed for a center region **80**, a left central region **82** and the right central region **84** as shown in FIG. **5**.

FIG. **9** shows the operating sequence of the camera. The user adjusts the zoom setting and points the camera to compose the image, and then presses the still capture button **16**. The camera focus is adjusted to a mid-range position, and the sensor **20** is cleared of any charge using the fast dump structure **62** for all lines on the entire sensor. An image, to be used for focusing the camera lens, is then integrated for a period of time, for example 10 mSec, during the focusing mode. During this mode, a top portion of the image is rapidly read out and discarded, using "fast flush" clocking where the vertical and horizontal registers are continuously clocked and the fast dump gate FDG remains high. The vertical clock sequence is then set to a line skipping operation (e.g., read two lines, dump two lines, read two, dump two, etc.), while the small number of remaining (not dumped) lines in the central area **66** of the image are clocked out. The average absolute value output (average contrast) of a horizontal spatial bandpass filter processing these image lines is used to determine how well the image is focused. This average contrast value is stored by the control interface **52**, and the lens focus is adjusted while the remainder of the image charge is cleared out using fast flush timing. The process of integrating and reading out the focus image is then repeated for a second focusing cycle. If the average contrast increases, the lens focus position is stepped again in the same direction. If the average contrast decreases, the focus position is moved in the opposite direction. These focusing cycles are repeated numerous times as the lens focus is adjusted until it provides the

maximum average contrast. The entire focusing sequence occurs rapidly, taking only a fraction of a second. Once the average contrast has reached a maximum value, the focus is acceptable. At this point, the entire sensor **20** is cleared, using the fast dump structure **62**. The final image is then integrated for a period of time and then transferred to the vertical registers **59**, which terminates the exposure. The final image is finally read out from the horizontal register **60**.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention. For instance, FIG. **2B** shows a progressive scan sensor with two readout registers **86** and **88** (which corresponds to the Performance Specification document for the KAI-0310CM image sensor; the preferred embodiment of FIG. **2A** simply uses but one register). The purpose is to double the system speed by having two complete processing channels (analog processing, A/D, etc.); the fast dump structure **62** of such a sensor would be operated as described in connection with foregoing figures to eliminate lines of charge in the central focusing area **66**. Furthermore, although the Bayer pattern was described, other mosaic-type filter patterns could be used to advantage, for example, complementary patterns involving cyan, magenta, and yellow filters. While the preferred embodiment maintains the Bayer (mosaic) geometry for the benefit of subsequent algorithms, this is not strictly necessary. The line-skipping focusing mode could alternate between saved and dumped lines of charge, with the subsequent processing being accordingly adapted to the particular color progression that is output.

PARTS LIST

**10** optical viewfinder
**12** control section
**14** zoom buttons
**16** capture button
**18** flash
**20** image sensor
**22** zoom lens
**23** mechanical coupling
**24** mechanical aperture
**26** memory card
**27** timing and control section
**28** sensor timing circuit
**30** sensor drivers
**32** analog gain and CDS circuit
**34** A/D converter
**35** processor section
**36** digital processor
**38** DRAM memory
**40** interface
**42** EPROM memory
**44** zoom motor
**46** focus motor
**48** variable aperture
**50** lens motor drivers
**52** control interface
**54** photosystems interface
**55** flash control circuit
**56** focus determination circuit
**58** photosites
**59** vertical registers
**60** horizontal register
**62** fast dump structure
**64** sensor substrate
**66** central focusing area
**68** outer area
**70** subtractor
**72, 74** registers
**76** summer
**78** accumulator register
**80** center region
**82** left central region
**84** right central region
**86** first readout register
**88** second readout register

We claim:

**1.** An electronic camera having an automatically focused lens that is operable to focus an image based on image data electronically obtained by the camera from a partial area of the whole image, said camera comprising:

an image sensor comprising a two-dimensional array of photosites arranged in lines and columns to provide image charge, the sensor having the capacity to eliminate some lines of image charge and to transfer other lines of image charge;

a timing and control section for controlling the sensor so as to eliminate a pattern of lines of image charge from the partial area utilized for autofocus so as to leave an array of intervening lines, and to transfer the intervening lines of image charge within the partial area; and

a processor for generating a focus adjustment signal based on the intervening lines of image charge transferred from the partial area.

**2.** An electronic camera as claimed in claim **1** wherein the timing and control section controls the image sensor so as to eliminate all lines of image charge from the remaining area outside the partial area.

**3.** An electronic camera as claimed in claim **1** wherein the timing and control section generates a pattern of eliminated lines within the partial area by eliminating two or more consecutive lines of image charge within the partial area for every two lines of image charge that are transferred from the partial area.

**4.** An electronic camera as claimed in claim **3** wherein two lines are eliminated for every two lines that are transferred.

**5.** An electronic camera as claimed in claim **3** wherein six lines are eliminated for every two lines that are transferred.

**6.** An electronic camera as claimed in claim **1** wherein the partial area is a central area of the whole image.

**7.** An electronic camera having an automatically focused lens, the lens operable to focus an image based on image data electronically obtained by the camera, the camera comprising:

an image sensor comprising a two-dimensional array of photosites arranged in lines and columns, a plurality of vertical registers adjacent photosite columns for transferring lines of image charge from the photosites to a horizontal register for readout as image data, and a charge drain interposed between the output of the vertical registers and the horizontal register for eliminating complete lines of image charge at a time from the image sensor;

a timing and control section for controlling the charge drain so as to eliminate at least one line of image charge from a central area of the image sensor for every one or more consecutive lines of image charge that are transferred from the central area to the horizontal register for readout, thereby generating a pattern of transferred lines suitable for focus determination; and

a processor generating a focus adjustment signal based on the transferred lines from the central area.

8. An electronic camera as claimed in claim 7 wherein said timing and control section provides a pattern of lines within the central area by eliminating two or more consecutive lines of image charge for every two lines of image charge that are transferred to the horizontal register.

9. An electronic camera as claimed in claim 8 wherein two lines are eliminated for every two lines that are transferred.

10. An electronic camera as claimed in claim 8 wherein six lines are eliminated for every two lines that are transferred.

11. An electronic camera as claimed in claim 7 wherein the image sensor is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines of image charge that are transferred to the horizontal register preserve the particular color pattern in the pattern of lines that are generated for readout.

12. An electronic camera as claimed in claim 11 wherein the array of color filters is arranged in the following mosaic pattern of red, green, and blue filters

R G R G

G B G B

R G R G

G B G B

and wherein the lines of image charge that are transferred to the horizontal register for readout preserve the same mosaic pattern.

13. An electronic camera having an automatically focused lens, the lens operable to focus an image data electronically obtained by the camera, the camera comprising:

a progressive scan image sensor capable of producing an entire image in a single scan in response to clocking signals, said image sensor comprising a two-dimensional array of photosites arranged in lines and columns, a plurality of vertical registers adjacent photosite columns for transferring lines of image charge from the photosites to a horizontal register for readout, and a fast dump structure interposed between the output of the vertical registers and the horizontal register for dumping complete lines of image charge at a time from the image sensor;

a timing and control section for producing clocking signals to read out the entire array of photosites in a single scan, said timing and control section further enabling the fast dump structure to dump at least one line of image charge from a central area of the image sensor utilized for autofocus for every one or more lines of image charge that are transferred from the central area to the horizontal register for readout, thereby generating a pattern of lines suitable for focus determination; and



a processor for generating a focus adjustment signal based on the transferred lines from the central area.

14. An electronic camera as claimed in claim 13 wherein said timing and control section provides a pattern of lines within the central area, and wherein said camera is operable in two modes, including a first mode in which the entire array of photosites are read out in a single scan, and a second mode in which said pattern of lines is generated by dumping two or more consecutive lines of image charges through the fast dump structure for every two lines of image charge transferred to the horizontal register to provide the focus adjustment signal.

15. An electronic camera as claimed in claim 14 wherein two lines are eliminated for every two lines that are transferred.

16. An electronic camera as claimed in claim 14 wherein six lines are eliminated for every two lines that are transferred.

17. An electronic camera as claimed in claim 13 wherein the image sensor is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines transferred to the horizontal register to provide the focus adjustment signal comprise a pattern that replicates the particular color pattern of the array of color filters.

18. An electronic camera as claimed in claim 17 wherein the array of color filters is arranged in the following mosaic pattern of red, green, and blue filters

R G R G

G B G B

R G R G

G B G B

and wherein the lines of image charge that are transferred to the horizontal register for readout preserve the same mosaic pattern.

19. An electronic camera having an automatically focused lens that images light upon an image sensor comprising a two-dimensional array of photosites arranged in lines and columns, the lens operable to focus an image based upon lines of image data integrated from a central area of the image sensor under control of a timing and control section, the improvement wherein

the timing and control section generates an intermittent pattern of lines within the central area utilized for autofocus by dumping some lines and transferring other lines, the transferred lines being used in the focus of the lens.

* * * * *

US005523786A

# United States Patent [19]

Parulski

[11] Patent Number: 5,523,786

[45] Date of Patent: Jun. 4, 1996

[54] **COLOR SEQUENTIAL CAMERA IN WHICH CHROMINANCE COMPONENTS ARE CAPTURED AT A LOWER TEMPORAL RATE THAN LUMINANCE COMPONENTS**

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[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **171,731**

[22] Filed: **Dec. 22, 1993**

[51] **Int. Cl.**[6] ..... **H04N 9/07**; H04N 5/225

[52] **U.S. Cl.** ..... **348/269**; 348/70; 348/237; 348/221; 348/364

[58] **Field of Search** ..... 348/65, 68, 70, 348/71, 234, 237, 268, 269, 272, 757, 780, 221, 362, 363, 364, 224, 229; 128/6; H04N 5/225, 9/04, 9/07

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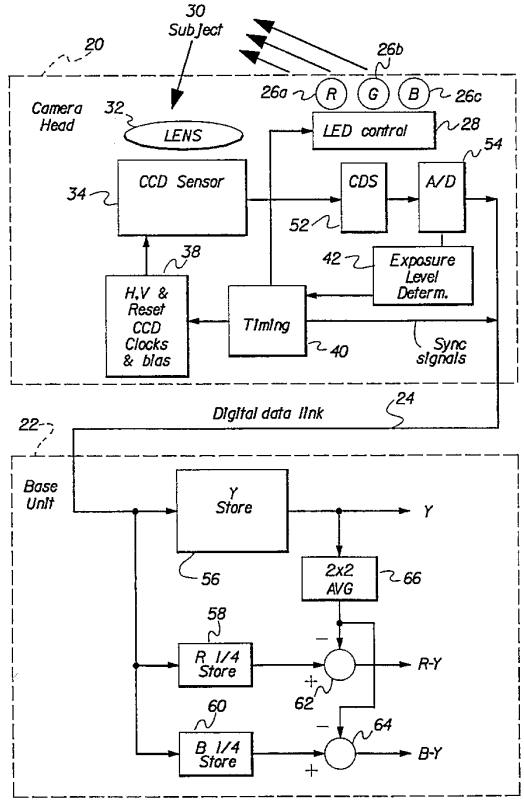
*Primary Examiner*—Safet Metjahic
*Assistant Examiner*—Cheryl Cohen
*Attorney, Agent, or Firm*—David M. Woods

[57] **ABSTRACT**

A color sequential electronic camera includes an RGB light source in which the R and G sources are activated in combination to provide a luminance light beam, and the R and B sources separately to provide separate chrominance light beams. Image light reflected by a subject is captured by an image sensor, which generates a color sequential signal comprising a sequence of luminance and chrominance image components. By activating the light sources such that chrominance light beams alternate between luminance light beams, the chrominance image components are captured at a lower temporal rate than the luminance image components. Furthermore, by binning the sensor photosites together for the chrominance image, the chrominance components are captured at a lower spatial resolution than the luminance image components.

**41 Claims, 10 Drawing Sheets**



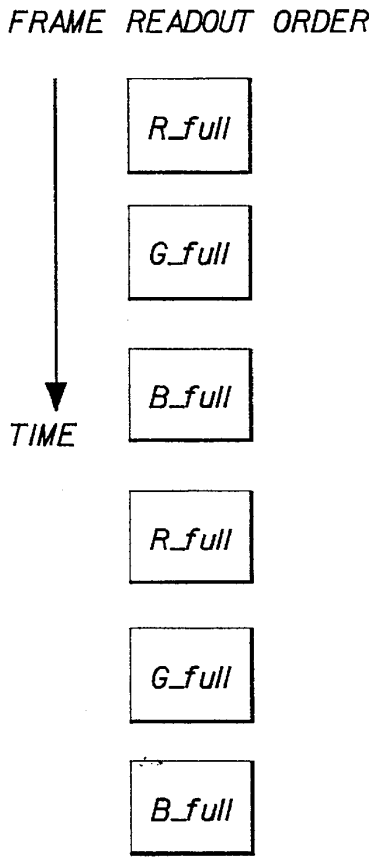



FIG. 1
(PRIOR ART)

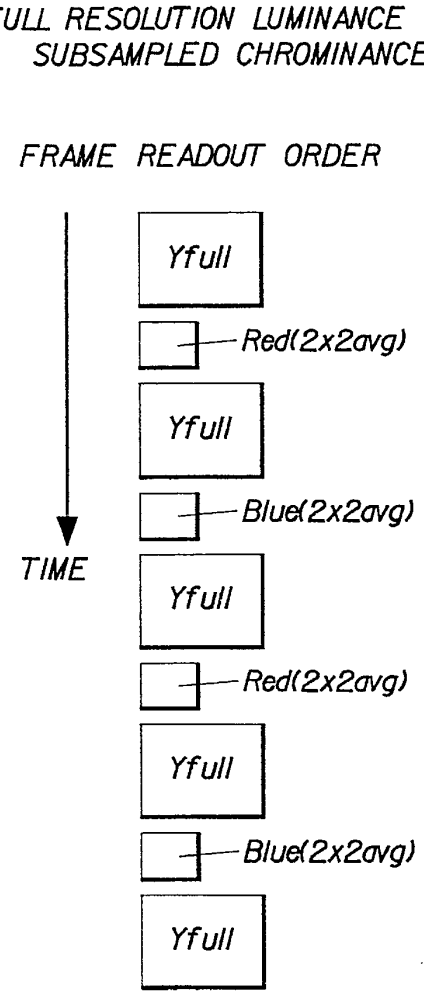



FIG. 2

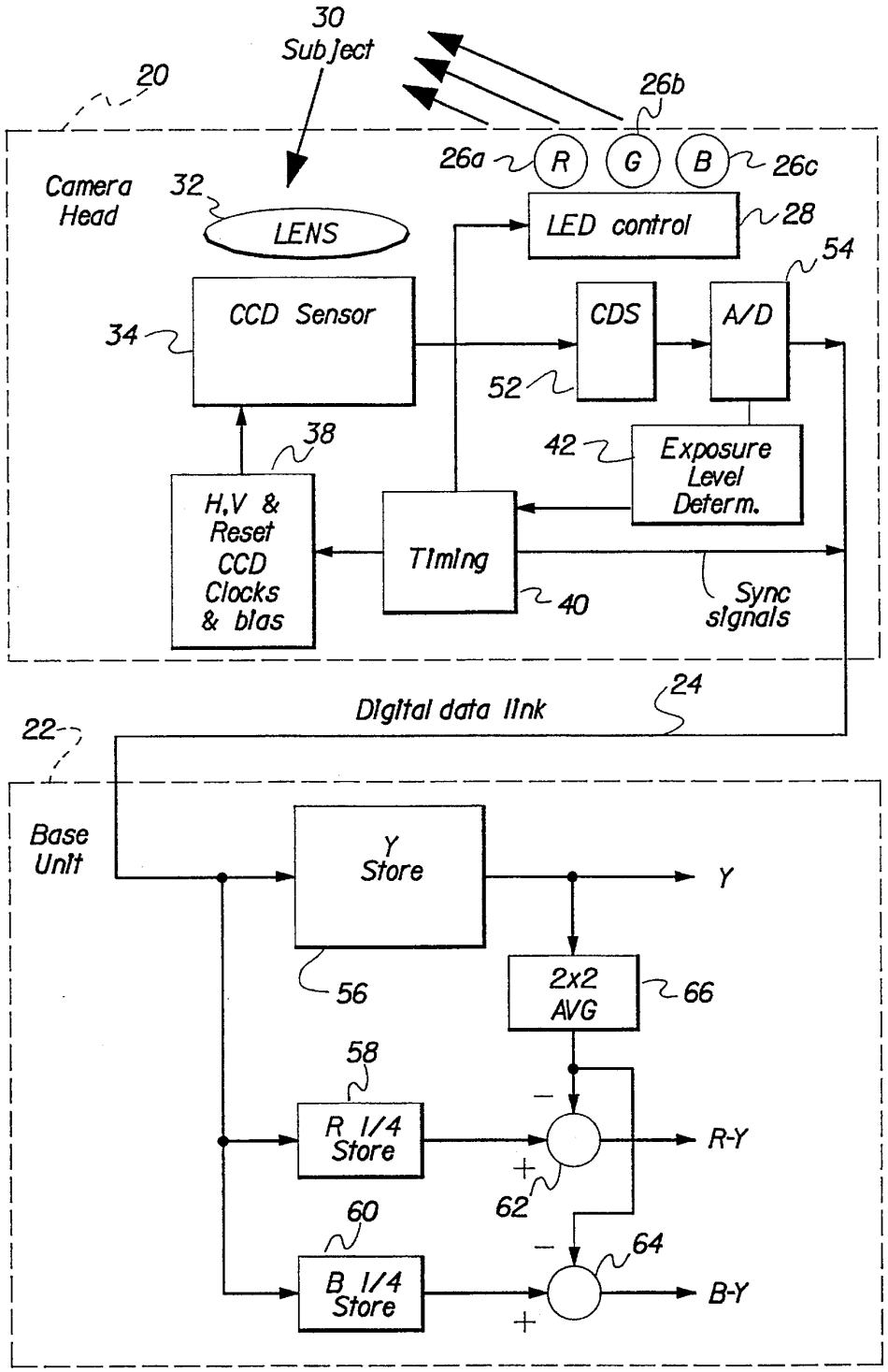

30
Subject
20
26b
26a
R
G
B
26c
Camera Head
32
LENS
LED control
28
54
CCD Sensor
34
CDS
A/D
52
38
42
Exposure Level Determ.
H,V & Reset CCD Clocks & bias
Timing
40
Sync signals
Digital data link
24
22
Base Unit
Y Store
Y
56
2x2 AVG
66
58
R 1/4 Store
R-Y
62
60
64
B 1/4 Store
B-Y

FIG. 3

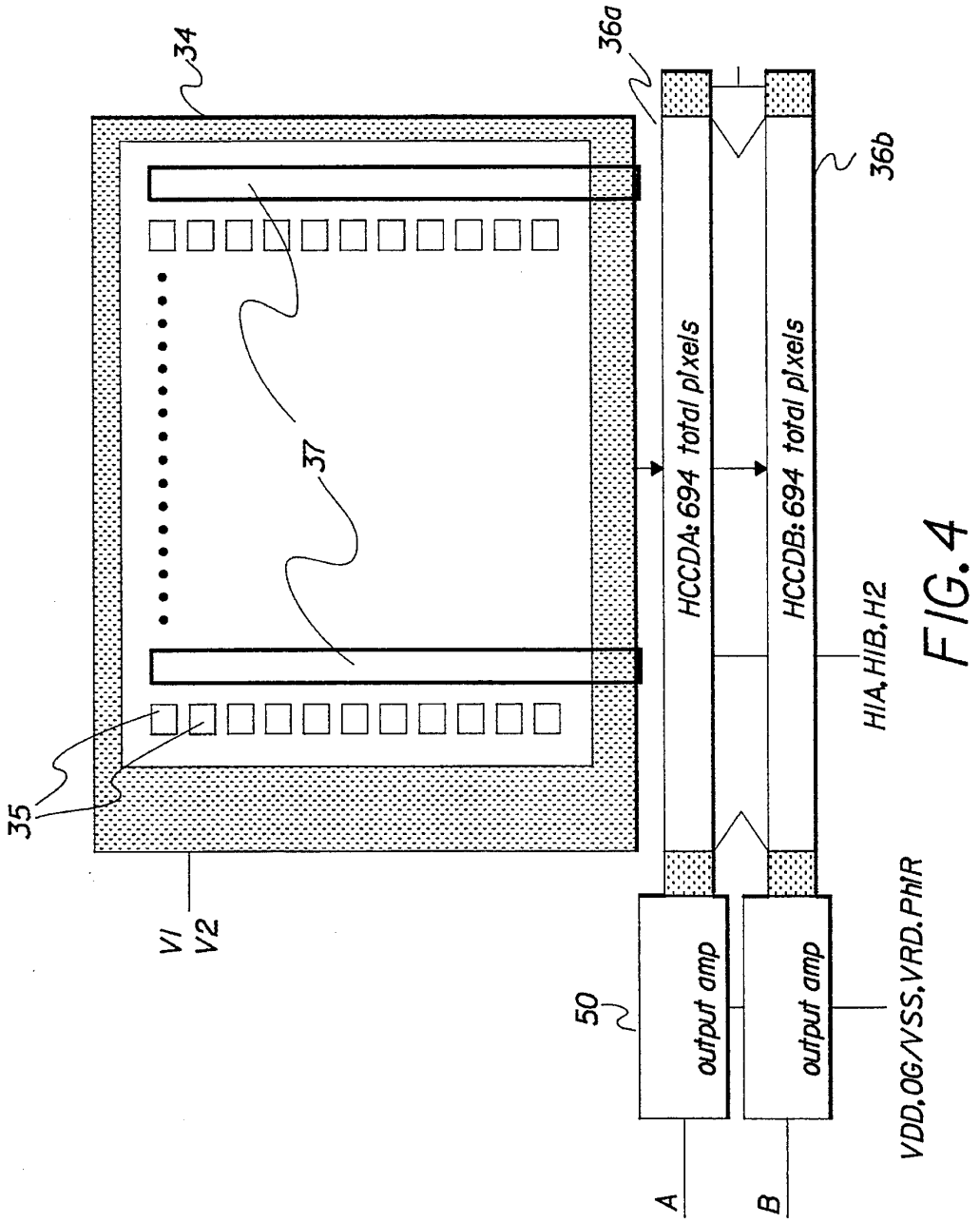
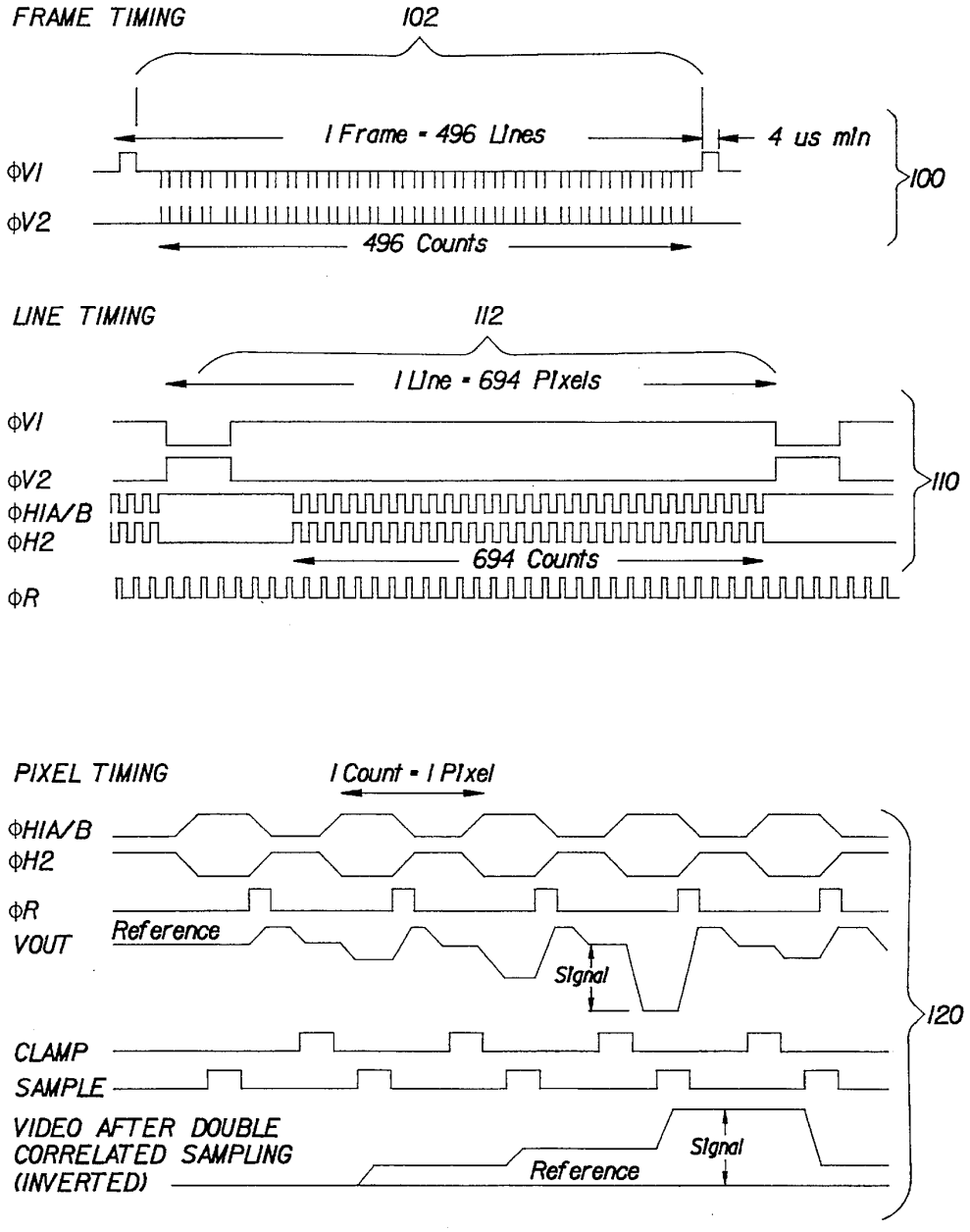
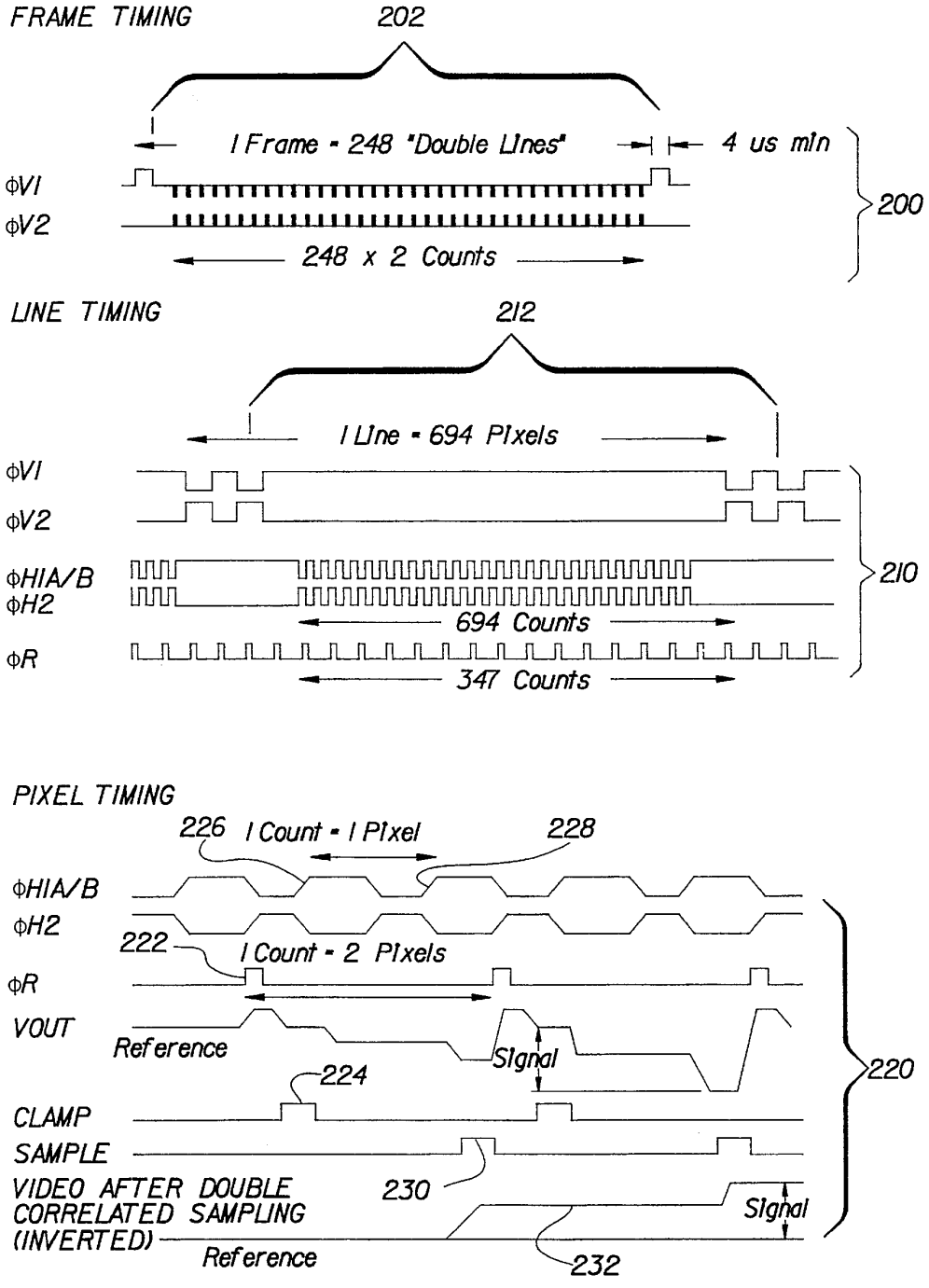

34
36a
36b
37
35
HCCDA: 694 total pixels
HCCDB: 694 total pixels
H1A, H1B, H2
V1
V2
50
output amp
output amp
A
B
VDD, OG/VSS, VRD. PhIR

FIG. 4




Timing Diagram - Normal Single Register Readout

FIG. 5




Timing Diagram - 2:1 Vertical and Horizontal "Binning"

FIG. 6

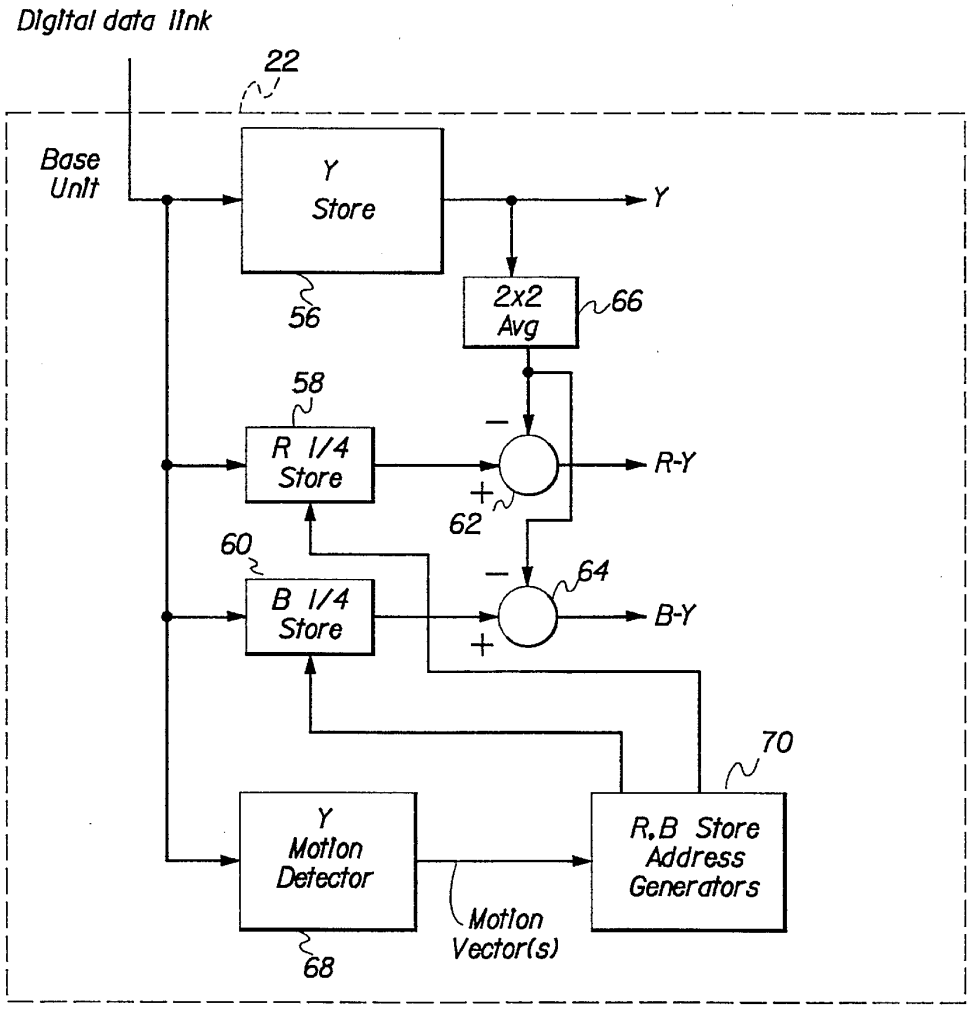

Digital data link
22
Base Unit
Y Store
56
Y
2x2 Avg
66
58
R 1/4 Store
R-Y
62
60
B 1/4 Store
64
B-Y
70
Y Motion Detector
68
Motion Vector(s)
R,B Store Address Generators

FIG.7

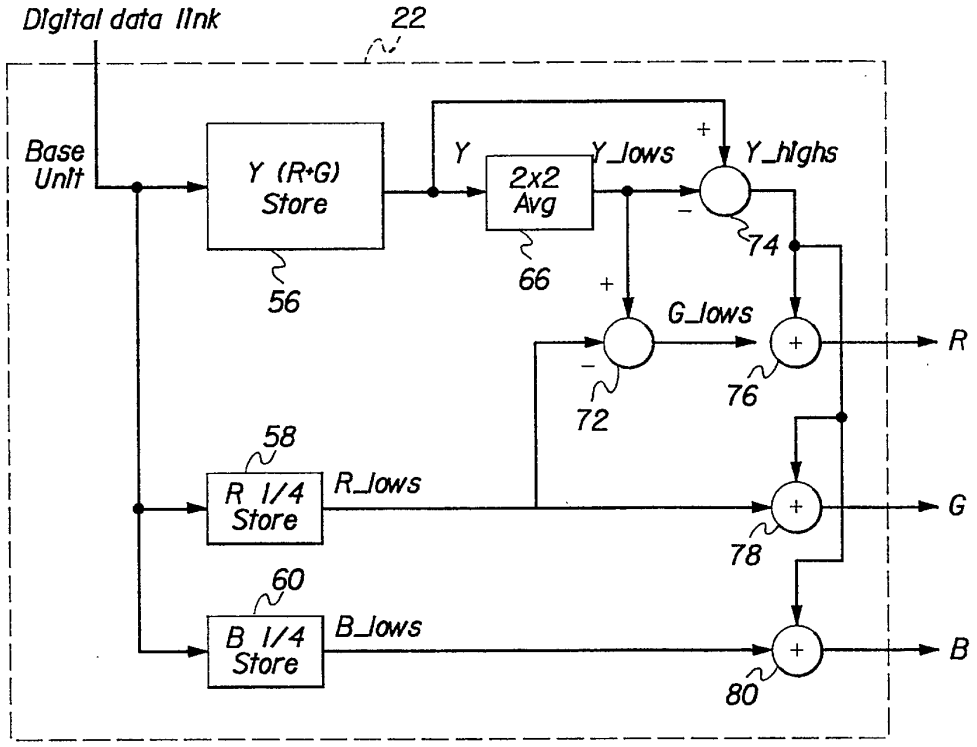

Digital data link
22
Base Unit
Y (R+G) Store
56
Y
2x2 Avg
66
Y_lows
Y_highs
74
G_lows
72
76
R
58
R 1/4 Store
R_lows
G
78
60
B 1/4 Store
B_lows
B
80

FIG. 8

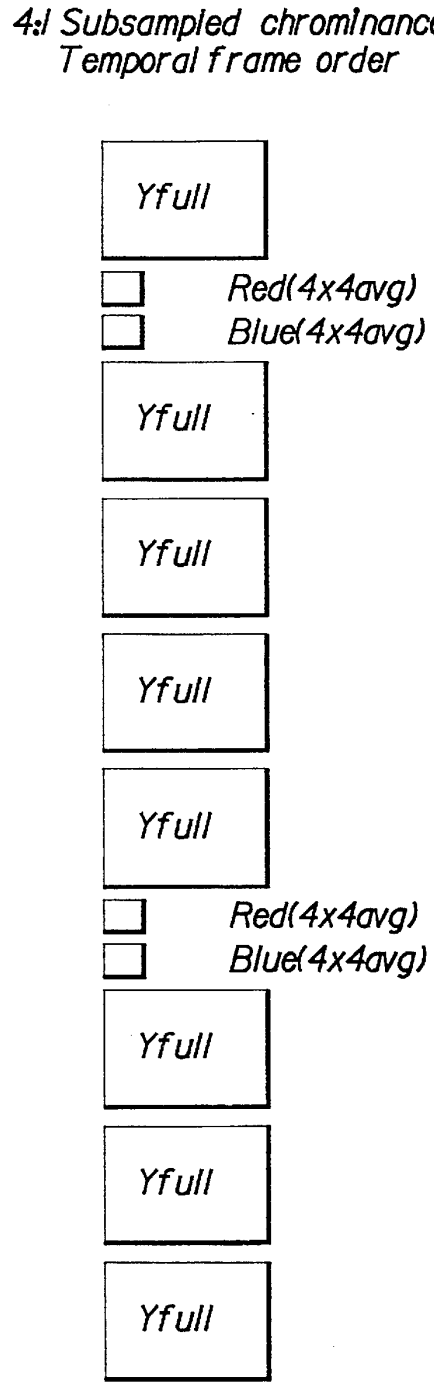

4:1 Subsampled chrominance
Temporal frame order
Yfull
Red(4x4avg)
Blue(4x4avg)
Yfull
Yfull
Yfull
Yfull
Red(4x4avg)
Blue(4x4avg)
Yfull
Yfull
Yfull

FIG. 9

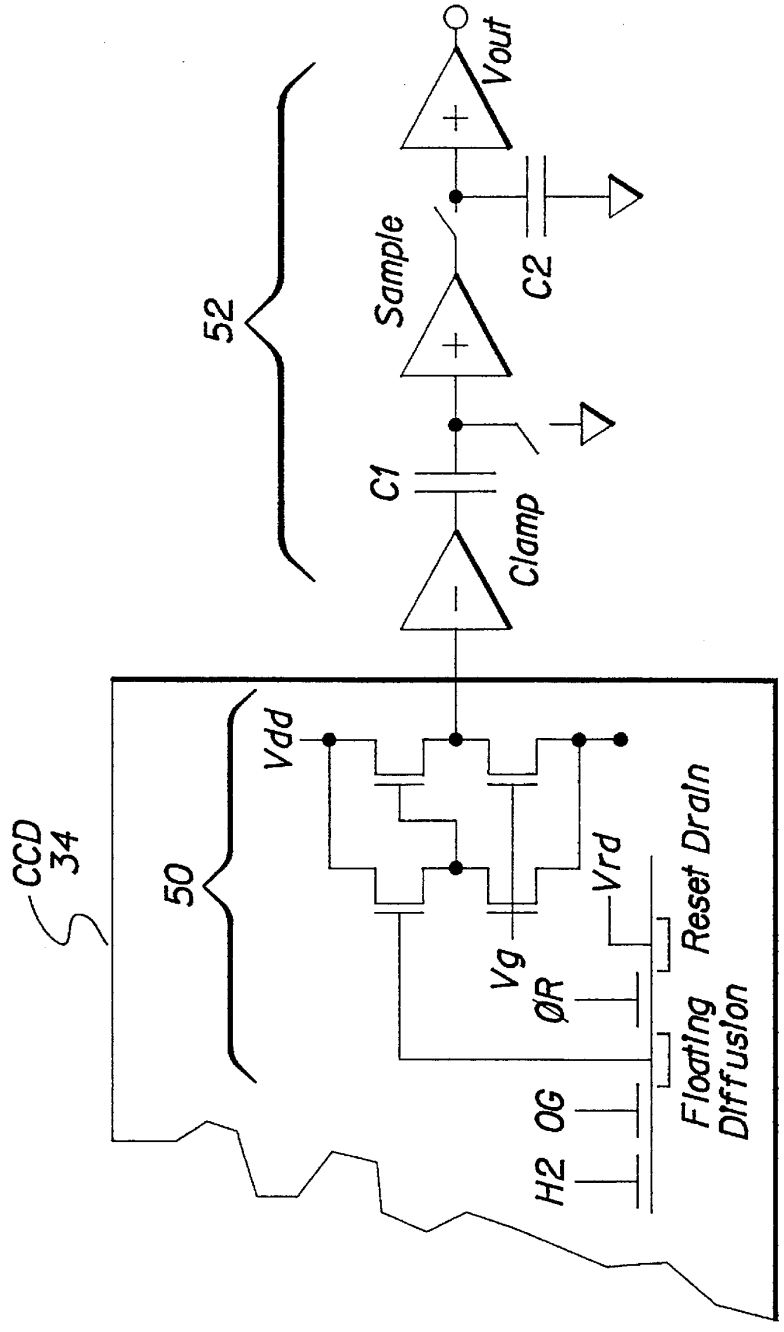

CCD
34
50
52
Vdd
Vg
ØR
Vrd
Reset Drain
Floating
Diffusion
ØG
H2
Clamp
C1
Sample
C2
Vout

FIG. 10

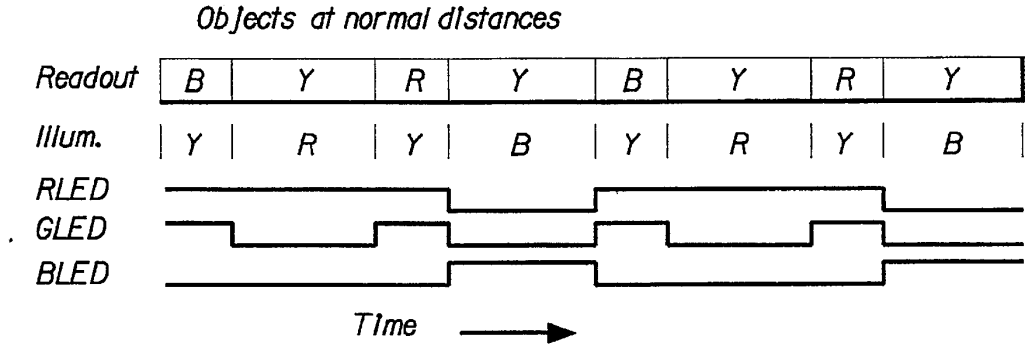



FIG. IIA

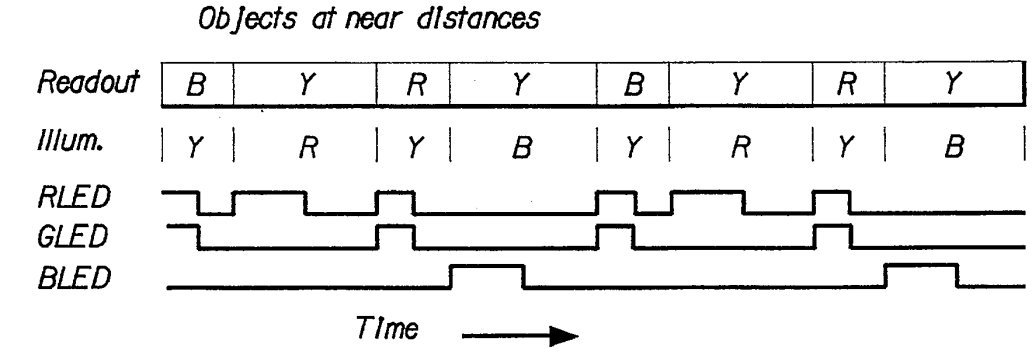



FIG. IIB

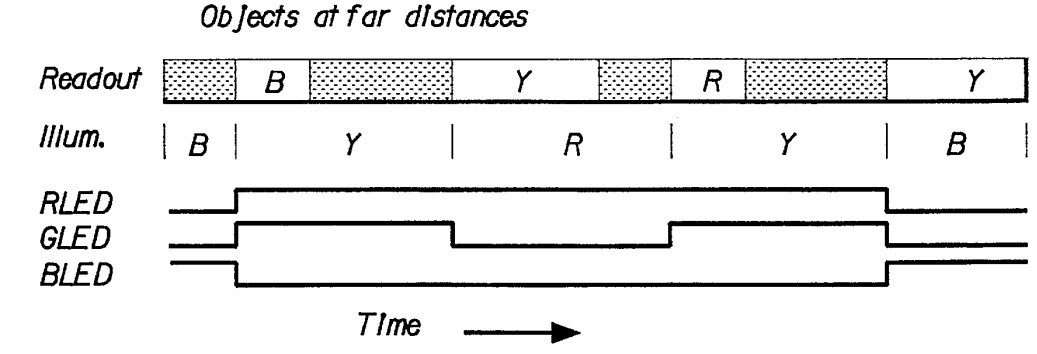



FIG. IIC

# COLOR SEQUENTIAL CAMERA IN WHICH CHROMINANCE COMPONENTS ARE CAPTURED AT A LOWER TEMPORAL RATE THAN LUMINANCE COMPONENTS

## FIELD OF INVENTION

This invention relates to electronic cameras using solid state image sensors, and, in particular to color sequential electronic cameras.

## BACKGROUND OF THE INVENTION

In some applications, such as medical imaging, a low power color sequential camera head, using a monochrome sensor, provides a digital output signal over a low bit rate digital link to a remote base unit. A typical application is an endoscope for examining body cavities, wherein the camera head is at the end of a probe, and the base unit includes a monitor for viewing images captured by the camera head. The camera head sequentially illuminates the scene with red, green, and blue light, and then sequentially digitizes the red, green, and blue color images output from the monochrome sensor. In addition, to minimize power, the pixel rate of the digital output signal should be as low as possible, while still maintaining good image resolution and good motion portrayal. Ordinarily, the RGB images all use the full sensor resolution. The monochrome sensor is read out in an interlaced mode at 60 fields per second, so that there are 20 red, 20 green, and 20 blue fields per second.

A known type of field sequential color television system, for use in a known type of endoscope, is shown in U.S. Pat. No. 4,845,553. The light of three primary colors (red, green, and blue) is sequentially irradiated onto an object such as an organism, and the reflected light of each of the individual colors is received by a charge-coupled device (CCD), where it is converted into an electrical image signal. After the thus-obtained picture signals are stored in memories in succession, they are converted into color television signals by a processor and displayed on a color monitor. In particular, as shown in the '553 patent, the memory capacity is reduced by sub-sampling the full resolution output of the CCD for the red and blue light, while maintaining the green light at its full resolution output.

In U.S. Pat. No. 4,685,451, red and blue light is similarly sub-sampled, but within the same timing. This is done by utilizing a single sensor having cyan and yellow color filters. Full resolution green is obtained for odd fields by illuminating the sensor with green light (cyan and yellow photosites both being sensitive to green light), and red and blue are obtained at lesser resolution for even fields by illuminating the sensor with white (or magenta) light (cyan and yellow photosites being separately sensitive to blue and red light, respectively). The light may be input into the endoscope sheath by means of fibers, or, as described in U.S. Pat. No. 4,074,306, a package enclosing a plurality of solid state light emitting chips can be mounted in the sheath of the endoscope.

In the known systems as described, including ones that use sub-sampling to reduce resolution and storage, the pixel data rate nonetheless must be maintained at relatively high rates, such as 12 MHz or thereabouts. Moreover, subsampling can reduce image quality by introducing color aliasing artifacts. To provide an improved camera, what is needed is a lower pixel rate, to decrease power consumption, yet a higher field rate, to improve motion rendition—without producing color artifacts.



## SUMMARY OF THE INVENTION

Since the human visual system is more sensitive to luminance wavelengths than to chrominance wavelengths, an object of the invention is to improve motion rendition with an electronic camera that is more sensitive to luminance temporal resolution than to chrominance temporal resolution.

A further object of the invention is to utilize the lower chrominance resolution to provide an electronic camera with a lower pixel rate.

A further object of the invention is to increase the signal level of dimly illuminated objects by decreasing the temporal update rate, so as to increase the exposure time, and by increasing the binning factor, so as to sum more pixels together.

Accordingly, the invention provides for an electronic color sequential camera including a plurality of light sources arranged to sequentially illuminate a subject; means for activating a) two or more of said light sources to generate a luminance light beam and b) selected ones of said light sources to generate at least first and second chrominance light beams, the luminance and chrominance light beams being generated in a predetermined sequence; and an image sensor arranged to receive the luminance and chrominance light beams reflected from the subject and to generate therefrom a color sequential signal comprising a sequence of luminance and chrominance image components, whereby the camera is more sensitive to luminance temporal resolution than to chrominance temporal resolution.

As further detailed, the invention includes the emission of a sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams. The image sensor then generates a color sequential signal comprising a sequence of luminance image components separated by an alternating sequence of chrominance image components, whereby the chrominance image components are captured at a lower temporal rate than the luminance image components, and the pixel rate is consequently lowered.

Furthermore, the image sensor may comprise an array of photosites arranged in rows and columns, such that the luminance image component is obtained from substantially all the photosites and the chrominance image components are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values, whereby the chrominance image components are captured at a lower spatial resolution than the luminance image components, and the pixel rate is further lowered. Furthermore, the binning operation increases the signal level of the chrominance components, which allows lower power light sources to be used, thus further reducing the power.

The advantage of the invention, as heretofore described, is that luminance emissions are customized to the human visual system, while reduced chrominance resolution is appropriate, since the human visual system is more sensitive to luminance spatial resolution than to chrominance spatial resolution. This results in an electronic color sequential camera with better temporal resolution, and therefore better motion portrayal, with fewer colored edge artifacts and with a lower camera head data rate.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the temporal frame readout order and spatial resolution for a prior art system;

FIG. **2** shows the temporal frame readout order and spatial resolution for a system according to the invention;

FIG. **3** shows a block diagram of a camera head and a base unit according to the invention;

FIG. **4** is a diagram of the image sensor used in the camera head shown in FIG. **3**;

FIG. **5** shows timing waveforms for "normal" operation of the sensor shown in FIG. **4**;

FIG. **6** shows timing waveforms for 2×2 binning operation of the sensor shown in FIG. **4**;

FIG. **7** shows a second embodiment of the invention having a base unit using the luminance motion vector to shift the stored chrominance components;

FIG. **8** shows a third embodiment of the invention having a base unit with simple processing to provide RGB output signals;

FIG. **9** shows a fourth embodiment of the invention using 4:1 temporal and spatial chrominance subsampling;

FIG. **10** shows a correlated double sampling circuit used in camera head of FIG. **3**; and

FIGS. **11**A, B and C show readout and illumination waveforms for different levels of exposure.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention is based in part on the recognition that it is possible to turn on more than one color emitter during the sensor illumination period. This allows the camera to capture luminance frames, which are ordinarily defined as the weighted sum of red, green, and blue light. For television cameras capturing normal pictorial scenes, luminance is typically composed of approximately 60% green, 30% red, and 10% blue light. For medical applications inside body cavities, however, other weightings of red, green and blue may provide better images, because the reflectance of typical objects is higher for red and lower for blue, relative to normal pictorial scenes. Therefore, the combination of red and green light is used to provide luminance in practice of the invention. Two other color sequential frames are used to provide chrominance resolution, by illuminating only one color emitter per frame integration time, for example red or blue. Psychophysical studies have shown that not only is luminance spatial resolution more visually important than chrominance spatial resolution, but luminance temporal resolution is also more visually important than chrominance temporal resolution. Therefore, for a given pixel data rate, the perceived temporal resolution is increased and image quality can be optimized by using luminance frames instead of green frames. Furthermore, by reducing the spatial resolution as well as the number of the red and blue frames, relative to the luminance frames, the camera head output data rate can be decreased while providing improved image quality.

A simplified diagram of the difference between the present invention and the prior art is shown in FIGS. **1** and **2**. In the prior art, shown in FIG. **1**, the resolution and number of red, green, and blue frames (or alternately red, green, and blue fields, for interlaced video formats) is equal. The temporal frame readout sequence of the invention, shown in FIG. **2**, indicates that there are twice as many luminance frames as red or blue frames. Furthermore, the luminance frames have higher spatial resolution (×2 more lines and ×2 more pixels per line) compared to the red or blue frames.



A block diagram of an electronic color sequential camera according to the invention is shown in FIG. **3** in the form of a camera head **20** connected to a base unit **22** by a digital data link **24**. Although this invention is not limited to a specific application, a color sequential camera head **20** of the type described herein may be used in a medical application in the elongated insertion portion of an endoscope. The insertion portion (not shown as such, but which includes the digital data link **24**) is inserted into a body cavity of an organism, and the camera head **20** generates images that are transmitted back to the base unit **22** for observation by an attending physician (on a monitor, not shown).

In the camera head **20**, red, green, and blue light emitting devices (LEDs) **26***a*, **26***b*, **26***c* are activated by an LED control device **28** to emit red, green, and blue light beams outward from the camera head **20** toward a subject **30**. The subject **30**, being in a confined space, is illuminated only by the red, green and blue light beams. Red, green and blue light reflected from the subject **30** is then collected by a lens **32** and directed to an image sensor **34**. An exemplary sensor useful with the invention is the Kodak KAI-310 CCD image sensor shown in FIG. **4**. This sensor is an interline transfer CCD device having photodiodes **35** connected to vertical readout registers **37** (shown in part in FIG. **4**). The CCD has a progressive scan (non-interlaced) architecture, such that every pixel is transferred into the vertical registers **37** during each frame readout time. This sensor has 484 active lines and 648 active photosites per line, and a pair of read out registers **36***a*, **36***b*. In this embodiment, only readout register **36***a* is used, to provide a single register video output signal, although the CCD is capable of providing dual output signals. The CCD contains additional black (light-shielded) photosites vertically and horizontally, so that a total of 496 vertical clock cycles, with 694 horizontal clocks per vertical cycle, are used to transfer each image frame.

In accordance with the invention, the luminance light beam is generated by activating both the red and green emitting devices **26***a* and **26***b* during the sensor integration period for the luminance image component. Then the red and blue emitting devices **26***a* and **26***c* are activated sequentially to generate red and blue chrominance light beams during the sensor integration period for the chrominance image components. Note that by turning on both red and green LEDs, the signal level of the luminance image component is substantially increased, so that the signal-to-noise ratio is improved. The blue LED **26***b* is not turned on for the luminance image component to reduce the power consumption since the efficiency of available blue LEDs is poor.

The clock and bias circuit **38** of the sensor **34** is clocked by a timing circuit **40**, which is capable of clocking out all of the pixels of the sensor, or binning (summing) together the pixels into a lower resolution image, for example one with 242 lines and 324 pixels per line. FIGS. **5** and **6** provide the timing diagrams for the normal and the 2×2 binning operation, respectively. In the binning operation, the photosite charge is summed first vertically and then horizontally, to create pixel values which include the signal charge from four neighboring photosites. In the normal timing, signal charge is transferred from the photosites **35** to the vertical readout registers **37** during transfer pulse times 102 of frame timing **100**. Lines are transferred one by one into the horizontal register **36**, utilizing the line timing waveforms **110** shown in FIG. **5**, and pixels are transferred out of the register **36**, utilizing the pixel timing waveforms **120** shown in FIG. **5**.

To sum or "bin" the charge vertically, two lines are transferred into the horizontal readout register **36***a* by

cycling V1 and V2 high and low twice per line, as shown in the waveform portion **212** of the "line timing" portion **210** of FIG. **6**, rather than once per line, as shown in the waveform portion **112** of the "line timing" portion **110** of FIG. **5**. To sum or "bin" the charge horizontally, the floating diffusion output is reset after every second pixel is read out, so that the charge from two horizontal pixels is summed on the output diffusion of an output amplifier **50** on the image sensor **34** (see FIG. **4**). Since each of these two horizontal pixels contains the charge from two vertically adjacent lines, the output signal level is nominally four times the signal level for the "normal" (no binning) operation, using the timing waveforms shown in FIG. **5**.

With respect to pixel timing for "binning" the charge horizontally, as shown in the "pixel timing" portion **220** of FIG. **6**, the output sequence is to first reset the floating diffusion output by cycling ΦR high and low at time **222**, which sets the output diffusion of the output amplifier **50** to a nominal voltage controlled by the reset drain voltage VRD. The next step is to clamp to this reset level by cycling the CLAMP signal controlling a correlated double sampling circuit **52** (shown in FIG. **10**) high and low at time **224**. The charge from the two adjacent horizontal pixels is transferred onto the floating diffusion output on the rising edge of ΦH1, at times **226** and **228** respectively. After the second horizontal pixel charge is transferred to the output diffusion, the voltage of the output diffusion is sampled with the SAMPLE signal at time **230**. This sampled value 232 is equal to the "binned" sum of 2 vertical and 2 horizontal pixels.

The timing circuit **40** also controls the light emitting devices **26***a*, **26***b*, **26***c* via the LED control device **28**, and provides sync signals to the digital data link **24**. The output of the output amplifier **50** on the image sensor **34** is processed by the correlated double sampling (CDS) circuit **52**, shown also in FIG. **10**, and an analog/digital (A/D) converter **54**. The A/D output is provided to an exposure level determination circuit **42** and is also sent: over the digital data link **24** to the base unit **22**. In the base unit **22**, the color sequential digital image frames are stored in separate luminance (Y), red (R) and blue (B) frame stores **56**, **58**, **60**. Since the R and B frames have only ½ as many lines and ½ as many pixels as the Y frame, smaller digital memories can be used to store these frames. The last Y, R, and B frames received from the camera head **20** are used to create a normal NTSC scanning format (525 total lines, 60 field/sec) color image. This is accomplished by forming luminance (Y) and color difference (R-Y and B-Y) signals in subtractors 62 and 64 by subtracting a 2×2 pixel average of the Y stored image generated by the averaging circuit **66** from the R and B images. These signals can be combined (in a subsequent circuit, not shown) to form a composite NTSC or an S-Video signal, or matrixed to form an RGB component NTSC image. Such processing is conventional, and well known in the art.

The exposure determination circuit **42** in FIG. **3** operates in conjunction with the timing circuit **40** and the LED control device **28** to provide the proper exposure. In an endoscope application, the light level reflected from objects depends on the distance between the object and the light sources **26***a*, **26***b*, **26***c* in the camera head **20**. The illumination level decreases dramatically as the distance between the light sources and the object increases. Therefore, the sensor exposure should be controlled, in order to provide acceptable images over the range of distances expected to be encountered. The exposure level determination circuit **42** determines the exposure level of a particular frame by calculating, for example, the average digital code level of the pixels of that frame. Alternately, the peak code level can be measured. The circuit then compares the level with a reference level, to determine whether the average or peak signal level is within a range of acceptable levels. If the level is outside the desired range, the exposure level is adjusted during the next capture of the same type (i.e., luminance, red, or blue) of frame.

FIG. **11**A shows the readout sequence of image sensor **34**, and the signals for controlling the red **26***a*, green **26***b*, and blue **26***c* LEDs for objects at normal distances. The R LED, G LED, and B LED signals are high when the respective LEDs are turned on, and low when the LEDs are turned off. Note that the readout color sequence lags the illumination color sequence by one frame period. For example, the red frame exposure is completed by turning on the red LED **26***a*, while a luminance frame is read out of the sensor. Next, the red frame is read out, while both the red and green LEDs **26***a*, **26***b* are turned on, to provide a luminance frame exposure. Next, the luminance frame is read out, while the blue LED **26***c* is turned on, to provide a blue frame exposure, and so on. Note also that the readout time for the luminance frames is approximately twice as long as for the red or blue frames. This happens because 2×2 "binning" is used to read out the red and blue signals. Because 2 lines are summed in the horizontal readout register **36***a*, as shown in time interval **212** of FIG. **6**, there are only 248 horizontal line readout periods using the 2×2 binning, as shown in frame timing waveforms **200**. In the normal readout mode used to read out the luminance frame, there are 496 line readout periods, as shown in frame timing waveforms **100**.

In FIG. **11**A, the illumination period is equal to the readout period. This provides proper exposure for objects at normal distances. However, for near objects, the amount of light reflected from the object is large, if the illumination period equals the readout period. Therefore, the illumination period is decreased, as shown in FIG. **11**B. In FIG. **11**B, the LEDs are illuminated for only a portion of the sensor readout period. This has the further advantage of decreasing the power consumption of the camera head.

Objects at far distances reflect very little light, since the illumination level is inversely proportional to the square of the distance between the light source and the object. In some prior art systems, electrical gain is used to amplify the signal level in such conditions. However, this also amplifies any sensor noise, so that the result is a noisy image. In other prior art systems, the illumination level is increased by increasing the current to the illumination source. Unfortunately, this greatly increases the power consumption and the temperature of the camera head. The present invention increases the sensor exposure for distant objects by decreasing the frame rate. This provides a longer exposure time for each frame, as shown in FIG. **11**C. Note that each frame illumination period is now twice as long as shown in FIG. **11**A. Therefore, the signal levels from the sensor are increased by a factor of two. This is accomplished by providing a "dormant" period between each frame readout, during which the appropriate LEDs are illuminated. The "dormant" period causes a decrease in the frame rate, but this causes little image degradation since the relative motion of far objects is much less than for near objects. The increased exposure level results in a noticeable increase in quality, because of the improved image signal-to-noise ratio.

For far objects which provide extremely low light levels, the signal levels can be further increased by using 2×2 "binning" of the luminance frames, and 4×4 "binning" of the red and blue frames. This provides an additional ×4 increase in the signal level, although it decreases the amount of image

detail. The overall quality of the image is improved, because the reduction in noise is much more noticeable than the reduction in image sharpness. In addition to adjusting the LED illumination periods, frame rate, and the amount of binning, the exposure level determination circuit **42**, can adjust the electrical gain of the amplifiers in the CDS circuit **52**, as is commonly done in the prior art.

FIG. **7** shows a second embodiment of a base unit **22** which includes a Y motion detector **68** to detect the amount of luminance motion from one frame to the next. The Y motion detector **68** could determine the average motion of the entire luminance frame (for example due to camera shake) or the motions of small blocks (for example 16×16 pixel blocks) within the luminance frame, and generate luminance motion vector(s). The luminance motion vector(s) are used to adjust the timing of address generators **70** used to read out the R and B stored data, so as to shift these image planes properly in the same direction as the luminance motion.

An applicable method for determining motion vectors is described in U.S. patent application 08/118,897, entitled "Method for processing color image records subject to misregistration", filed Sep. 9, 1993, in the name of Hintz et al. and assigned to Eastman Kodak Company. Hintz shows a method for correlating two subsections of an image, one subsection from a red image record and the second subsection from a green image record. The result of the correlation process performed on the two subsections provides an integer pixel shift value, which indicates the horizontal and vertical misregistration between the two image planes. This same method can be used to calculate the motion vector between two luminance images taken at two different periods of time. In this case, the result of the correlation process performed on the two luminance frames provides a pixel shift value, which indicates the horizontal and vertical motion between the two luminance images. This pixel shift value is a "motion vector", which indicates the magnitude and direction of the image motion that occurred between the two luminance frames. By shifting the red and blue planes in the direction of the motion vector, any color misregistration due to motion occurring between the color sequential red or blue frames and the luminance frames can be reduced.

The magnitude of the shift depends on the relative times at which the red, blue, and luminance frames were captured. For example, if there are 20 luminance frames per second, and 10 frames each for red and blue, then for the luminance frame which immediately follows a red frame, the red record should be shifted by ½ times the magnitude of the luminance motion vector, and the blue record should be shifted by ⅗ times the magnitude of the luminance motion vector.

If the motion is substantially uniform for the entire image, as would be the case if the motion was caused by camera motion, a single motion vector could correct the entire image. This is typically the case for medical endoscope applications. If, however, the motion is substantially different in different parts of the image, different motion vectors can be computed in different subsections of the image, and used to "warp" the stored red and blue frames to reduce color misregistration errors. U.S. patent application 07/712,865 "Cross correlation image sensor alignment system", filed Jun. 10, 1991 in the name of Parker, et al., and assigned to Eastman Kodak Company, describes a misregistration correction circuit that can shift different parts of an image by different amounts, using in this case the location motion vectors as the correction signal inputs.

Many other motion estimation methods can be used. Possible methods are described in an article by J. K. Aggarwal and N. Nandhakumar, entitled "On the computation of motion from sequences of images" which appeared in the Proceedings of the IEEE, volume 76, on pages 917–935 in August 1988, and in an article entitled "Review of motion analysis techniques", which appeared in the Proceedings of the IEEE, volume 136, part 1, on pages 397–404 in December 1989.

FIG. **8** shows a third embodiment of the base unit **22** with simple processing to provide RGB output signals. The luminance store **56** output (R+G, from turning on both the red and green LEDs) is averaged in groups of 2×2 pixels in the averaging circuit **66** to form a Y_lows signal. The R store **58** output is subtracted from Y_lows in a subtractor **72** to form G_lows. The Y_highs signal (luminance detail) is formed by subtracting Y_lows from the stored Y signal in a subtractor **74**. This "luminance detail" Y_ highs signal is added in adders **76**, **78**, **80** to the RGB lows signals to form high resolution RGB signals. The motion detection approach shown in FIG. **7** could be used with this RGB processing as well.

FIG. **9** shows a fourth embodiment of the invention using 4:1 temporal and spatial chrominance subsampling. The R and B signals are now binned (averaged) by 4:1 in each direction, to provide a 121×162 pixel image. There are four full resolution Y images for each R or B image, and the R and B images are temporally adjacent.

As is evident from the foregoing description, certain aspects of the invention are not limited to the particular details of the examples illustrated, and it is therefore contemplated that other modifications and applications will occur to those skilled in the art. It is accordingly intended that the claims shall cover all such modifications and applications as do not depart from the true spirit and scope of the invention.

PARTS LIST

**20** CAMERA HEAD
**22** BASE UNIT
**24** DIGITAL DATA LINK
**26***a* RED LIGHT EMITTING DEVICE
**26***b* GREEN LIGHT EMITTING DEVICE
**26***c* BLUE LIGHT EMITTING DEVICE
**28** LED CONTROL DEVICE
**30** SUBJECT
**32** LENS
**34** IMAGE SENSOR
**35** PHOTODIODES
**36***a* READ OUT REGISTERS
**36***b* READ OUT REGISTERS
**37** VERTICAL READOUT REGISTERS
**38** CLOCK AND BIAS CIRCUIT
**40** TIMING CIRCUIT
**42** EXPOSURE LEVEL DETERMINATION CIRCUIT
**50** OUTPUT AMPLIFIER
**52** CDS CIRCUIT
**54** A/D CONVERTER
**56** Y FRAME STORE
**58** R FRAME STORE
**60** B FRAME STORE
**62** SUBTRACTOR
**64** SUBTRACTOR

**66** AVERAGING CIRCUIT
**68** Y MOTION DETECTOR
**70** ADDRESS GENERATORS
**72** SUBTRACTOR
**74** SUBTRACTOR
**76** ADDER
**78** ADDER
**80** ADDER
**100** FRAME TIMING
**102** TRANSFER PULSE TIMES
**110** LINE TIMING PORTION
**112** WAVEFORM PORTION
**120** PIXEL TIMING WAVEFORM
**200** FRAME TIMING WAVEFORM
**202** TRANSFER PULSE TIMES
**210** LINE TIMING PORTION
**212** WAVEFORM PORTION
**220** PIXEL TIMING PORTION
**222** TIME
**224** TIME
**226** TIME
**228** TIME
**230** TIME
**232** SAMPLED VALUE

What is claimed is:

**1**. An electronic color sequential camera, comprising:

a plurality of light sources arranged to sequentially illuminate a subject;

means for activating a) two or more of said light sources within the same time to generate a luminance light beam and b) selected ones of said light sources independently to generate at least first and second chrominance light beams, the luminance and chrominance light beams being generated in a predetermined sequence; and

an image sensor arranged to receive the luminance and chrominance light beams reflected from the subject and to generate therefrom a color sequential signal comprising a sequence of luminance and chrominance image components.

**2**. A camera as claimed in claim **1** wherein said light sources include red, green, and blue light emitting devices, and wherein the luminance light beam is a combination of red and green emissions from said red and green devices and the first and second chrominance light beams are red and blue emissions, respectively, from said red and blue devices.

**3**. A camera as claimed in claim **2** wherein said luminance light is a weighted combination of the red and green emissions.

**4**. A camera as claimed in claim **1** further comprising a plurality of memory units coupled to said image sensor for separately storing the luminance and chrominance image components.

**5**. A camera as claimed in claim **4** wherein said predetermined sequence of light beams includes a sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams, and said image sensor generates a color sequential signal comprising a sequence of luminance image components separated by an alternating sequence of chrominance image components, whereby the chrominance image components are captured at a lower temporal rate than the luminance image components.



**6**. A camera as claimed in claim **4** wherein said image sensor comprises an array of photosites arranged in rows and columns, and said luminance image component is obtained from substantially all the photosites and the chrominance image components are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values, whereby the chrominance image components are captured at a lower spatial resolution than the luminance image components.

**7**. A camera as claimed in claim **4** or **5** further comprising means for reading each chrominance image component from said memory unit a plurality of times while spatially shifting the chrominance image components to compensate for motion of the luminance image component.

**8**. A camera as claimed in claim **1** or **2** wherein a correct exposure level for the subject is obtained by varying an illumination period of at least one of said luminance and chrominance light beams.

**9**. A camera as claimed in claim **8** wherein the luminance and chrominance image components represent frames read out from said image sensor, and the correct exposure level for the subject is obtained by further varying a frame readout period of the sensor.

**10**. An electronic color sequential camera, comprising:

a plurality of light sources arranged to sequentially illuminate a subject;

means for activating said light sources to generate a luminance light beam and at least first and second chrominance light beams, the luminance and chrominance light beams being generated in a predetermined sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams; and

an image sensor arranged to receive the luminance and chrominance light beams reflected from the subject and to generate therefrom a color sequential signal comprising a sequence of luminance image components separated by an alternating sequence of chrominance image components, whereby the chrominance image components are captured at a lower temporal rate than the luminance image components.

**11**. A camera as claimed in claim **10** wherein said light sources include red, green, and blue light emitting devices, and wherein the luminance light beam is a combination of red and green emissions from said red and green devices and the first and second chrominance light beams are red and blue emissions, respectively, from said red and blue devices.

**12**. A camera as claimed in claim **11** wherein said luminance light is a weighted combination of the red and green emissions.

**13**. A camera as claimed in claim **10** further comprising a plurality of memory units coupled to said image sensor for separately storing the luminance and chrominance image components.

**14**. A camera as claimed in claim **10** wherein said image sensor comprises an array of photosites arranged in rows and columns, and said luminance image component is obtained from substantially all the photosites and the chrominance image components are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values, whereby the chrominance image components are captured at a lower spatial resolution than the luminance image components.

**15**. A camera as claimed in claim **10** or **14** further comprising means for reading each chrominance image component from said memory unit a plurality of times while spatially shifting the chrominance image components to compensate for motion of the luminance image component.

16. A camera as claimed in claim 10 or 11 wherein a correct exposure level for the subject is obtained by varying an illumination period of at least one of said luminance and chrominance light beams.

17. A camera as claimed in claim 16 wherein the luminance and chrominance image components represent frames read out from said image sensor, and the correct exposure level for the subject is obtained by further varying a frame readout period of the sensor.

18. An electronic color sequential camera, comprising:

a plurality of light sources arranged to sequentially illuminate a subject;

means for activating at least two of said light sources within the same time to generate a luminance light beam and selected ones of said light sources independently to generate at least first and second chrominance light beams, the luminance and chrominance light beams being generated in a predetermined sequence; and

an image sensor arranged to receive the luminance and chrominance light beams reflected from the subject and to generate therefrom a color sequential signal comprising a sequence of luminance and chrominance image components, said image sensor comprising an array of photosites arranged in rows and columns from which said luminance image component is obtained from substantially all the photosites and the chrominance image components are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values, whereby the chrominance image components are captured at a lower spatial resolution than the luminance image components.

19. A camera as claimed in claim 18 wherein said light sources include red, green, and blue light emitting devices, and wherein the luminance light beam is a combination of red and green emissions from said red and green devices and the first and second chrominance light beams are red and blue emissions, respectively, from said red and blue devices.

20. A camera as claimed in claim 18 wherein said luminance light is a weighted combination of the red and green emissions.

21. A camera as claimed in claim 18 further comprising a plurality of memory units coupled to said image sensor for separately storing the luminance and chrominance image components.

22. A camera as claimed in claim 18 wherein said predetermined sequence of light beams includes a sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams, and said image sensor generates a color sequential signal comprising a sequence of luminance image components separated by an alternating sequence of chrominance image components, whereby the chrominance image components are captured at a lower temporal rate than the luminance image components.

23. A camera as claimed in claim 21 further comprising means for reading each chrominance image component from said memory unit a plurality of times while spatially shifting the chrominance image components to compensate for motion of the luminance image component.

24. A camera as claimed in claim 18 or 19 wherein a correct exposure level for the subject is obtained by varying an illumination period of at least one of said luminance and chrominance light beams.

25. A camera as claimed in claim 24 wherein the luminance and chrominance image components represent frames read out from said image sensor, and the correct exposure level for the subject is obtained by further varying a frame readout period of the sensor.

26. A color sequential video camera, comprising:

a plurality of light sources arranged to sequentially illuminate a subject;

means for activating a) two or more of said light sources within the same time to generate a luminance light beam and b) selected ones of said light sources independently to generate at least first and second chrominance light beams, the luminance and chrominance light beams being generated in a predetermined sequence;

an image sensor arranged to receive the luminance and chrominance light beams reflected from the subject and to generate therefrom a sequence of luminance and chrominance image signals; and

a plurality of memory units coupled to said image sensor for separately storing the luminance and chrominance image signals.

27. A camera as claimed in claim 26 wherein said predetermined sequence of light beams includes a sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams, whereby said image sensor generates a sequence of luminance signals derived from the luminance beams separated by an alternating sequence of chrominance image signals derived from either the first or second chrominance beams.

28. A camera as claimed in claim 26 wherein said image sensor is an array of photosites arranged in rows and columns, and wherein said luminance signal is obtained from substantially all the photosites and the chrominance image signals are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values.

29. A color sequential video imaging system, comprising:

a plurality of differently-colored light sources for illuminating a subject;

an optical section for collecting light from said sources reflected from the subject;

a solid state image sensor positioned for receiving the reflected light collected by said optical section; and

a timing section for driving two or more of said light sources within the same time to provide luminance-weighted light and for independently driving selected ones of said light sources to provide at least first and second chrominance-weighted lights, said timing section further driving said image sensor to provide a luminance image signal and first and second chrominance image signals in correspondence to the incidence of luminance and chrominance light upon said sensor.

30. A color sequential video imaging system, comprising:

a plurality of light sources for sequentially illuminating a subject with a plurality of differently-colored light beams;

an optical section for collecting light reflected from the subject;

a solid state image sensor positioned for receiving the reflected light collected by said optical section and for generating a sequence of image signals; and

a timing section for driving two or more of said light sources within the same time to provide a luminance-weighted light beam and for independently driving selected ones of said light sources to provide at least first and second chrominance-weighted light beams,

said timing section further driving said image sensor to provide a luminance image signal and first and second chrominance image signals in correspondence to the incidence of the luminance and chrominance light beams upon said sensor.

**31**. A color sequential video camera, comprising:

a plurality of light sources arranged to sequentially illuminate a subject;

an image sensor arranged to receive light reflected from the subject and to generate therefrom a sequence of image signals; and

means for sequentially energizing a) two or more of said light sources within the same time to generate a luminance-weighted beam of light, and b) selected ones of said light sources independently to generate at least first and second chrominance beams of light, whereby said image sensor correspondingly generates a sequence of luminance and chrominance image signals.

**32**. A camera as claimed in claim **31** wherein said sequentially energizing means generates a sequence of luminance-weighted beams of light separated by an alternating sequence of either first or second chrominance beams of light, whereby said image sensor generates a sequence of luminance signals separated by an alternating sequence of chrominance image signals derived from either the first or second chrominance beams of light.

**33**. A camera as claimed in claim **32** wherein said light sources are red, green, and blue light sources, and wherein said sequentially energizing means generates the luminance-weighted beam from a combination of at least red and green beams and the chrominance beams from red or blue beams.

**34**. An electronic color sequential camera, comprising:

a plurality of color light sources arranged to sequentially illuminate a subject;

means for activating said light sources to generate a plurality of light beams in a predetermined sequence;

an image sensor arranged to receive the light beams reflected from the subject and to generate therefrom a color sequential signal comprising a sequence of image frame components;

an exposure level determination section for determining an illumination level of the light beams reflected from the subject; and

a timing section for reading out the image frame components from said image sensor during a predetermined readout period according to a predetermined frame rate for normal illumination levels, wherein said timing section reduces the frame rate responsive to said exposure level determination section for low illumination levels such that, for low illumination levels, the period during which the light sources are illuminating the sensor is made longer than the readout period.

**35**. A camera as claimed in claim **34** wherein said light sources include red, green, and blue light emitting devices, and wherein a luminance light beam is generated from a combination of red and green emissions from said red and green devices and first and second chrominance light beams are generated from red and blue emissions, respectively, from said red and blue devices.

**36**. A camera as claimed in claim **35** wherein said luminance light is a weighted combination of the red and green emissions.

**37**. A camera as claimed in claim **35** further comprising a plurality of memory units coupled to said image sensor for separately storing the luminance and chrominance image components.

**38**. A camera as claimed in claim **37** wherein said predetermined sequence of light beams includes a sequence of luminance light beams separated by an alternating sequence of either first or second chrominance light beams, and said image sensor generates a color sequential signal comprising a sequence of luminance image components separated by an alternating sequence of chrominance image components, whereby the chrominance image components are captured at a lower temporal rate than the luminance image components.

**39**. A camera as claimed in claim **38** wherein said image sensor comprises an array of photosites arranged in rows and columns, and said luminance image component is obtained from substantially all the photosites and the chrominance image components are obtained by binning together selected rows and/or columns of photosites to produce a lesser number of pixel values, whereby the chrominance image components are captured at a lower spatial resolution than the luminance image components.

**40**. A camera as claimed in claim **37** or **38** further comprising means for reading each chrominance image component from said memory unit a plurality of times while spatially shifting the chrominance image components to compensate for motion of the luminance image component.

**41**. An electronic color camera comprising:

an image sensor arranged to receive light reflected from a subject and to generate therefrom a color signal comprising color components;

an exposure level determination section for determining an illumination level of the light reflected from the subject; and

a timing section for reading out the signal comprising color components from said image sensor during a predetermined readout period according to a predetermined frame rate for normal illumination levels, wherein said timing section reduces the frame rate responsive to said exposure level determination section for low illumination levels such that, for low illumination levels, the period during which the light is illuminating the sensor is made longer than the readout period.

* * * * *

US005440343A

# United States Patent [19]

Parulski et al.

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[45] Date of Patent: Aug. 8, 1995

[54] **MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS**

[75] Inventors: **Kenneth A. Parulski; Eric G. Stevens,** both of Rochester; **Robert H. Hibbard,** Fairport, all of N.Y.

[73] Assignee: **Eastman Kodak Company,** Rochester, N.Y.

[21] Appl. No.: **203,237**

[22] Filed: **Feb. 28, 1994**

[51] **Int. Cl.**[6] ..... **H04N 5/335**

[52] **U.S. Cl.** ..... **348/316;** 348/322; 348/220

[58] **Field of Search** ..... 348/207, 220, 294, 316, 348/317, 311, 314, 315, 322, 323, 297; H04N 5/335

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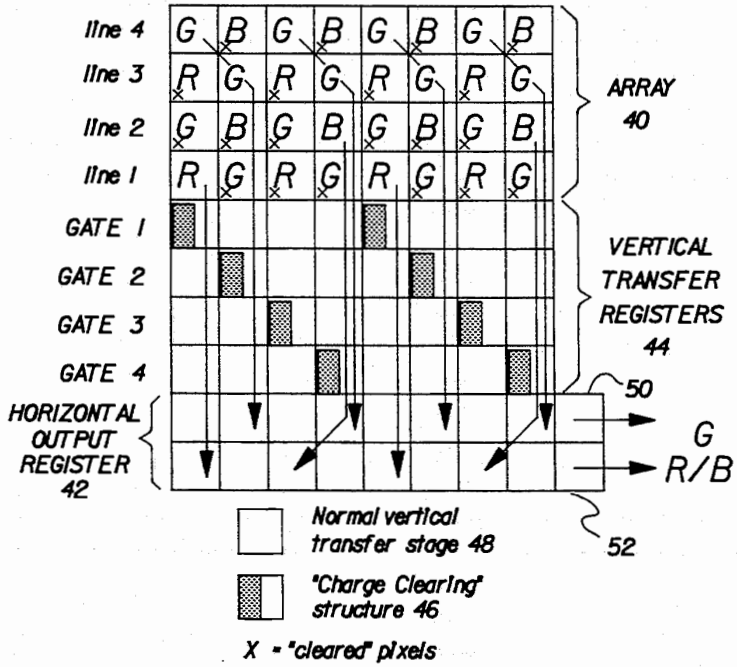
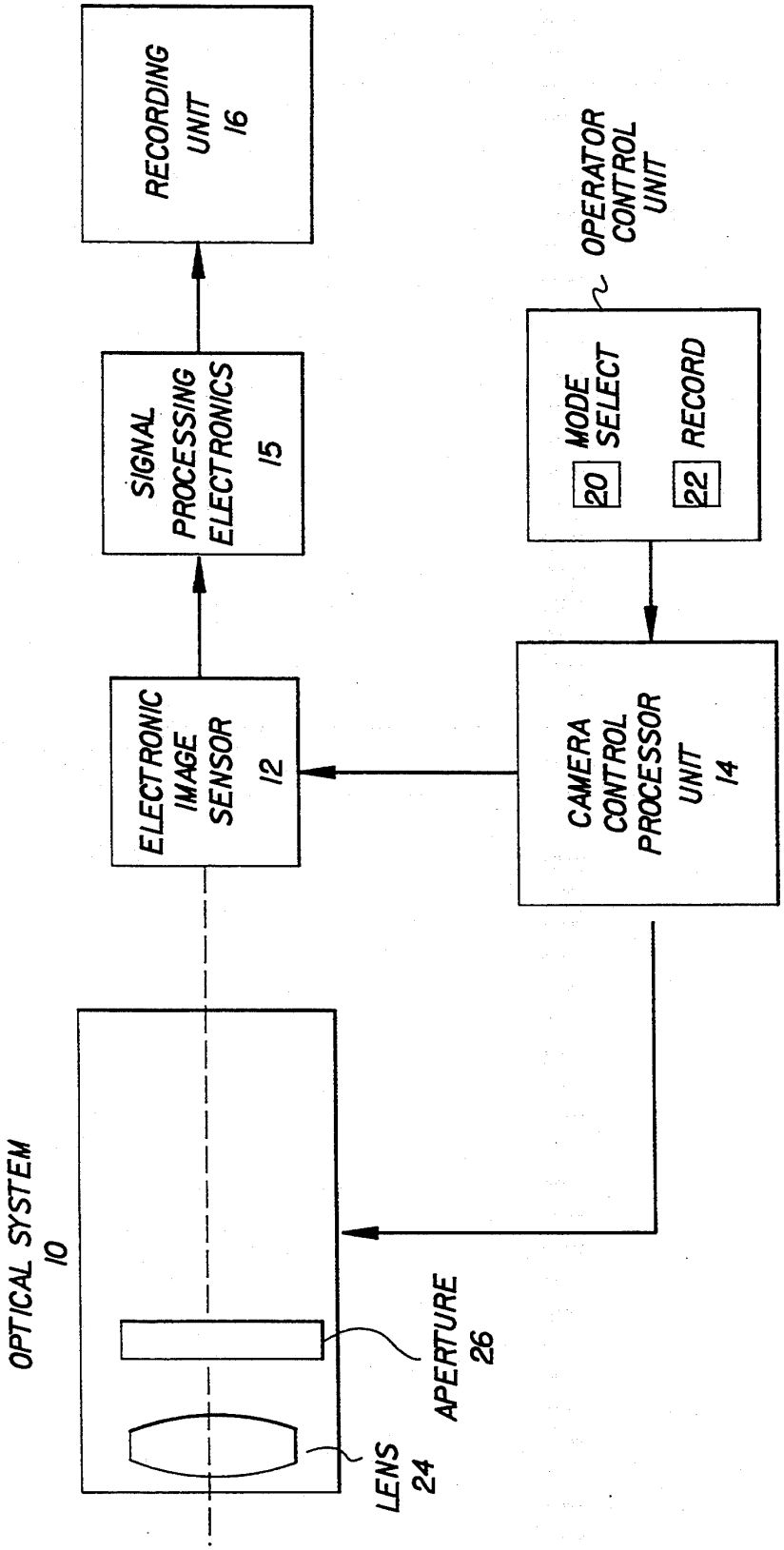
*Primary Examiner*—Michael T. Razavi
*Assistant Examiner*—Tuan V. Ho
*Attorney, Agent, or Firm*—David M. Woods

[57] **ABSTRACT**

An electronic imaging system is provided that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate. The electronic imaging system utilizes an electronic image sensor that incorporates column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from multiple vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

**12 Claims, 10 Drawing Sheets**

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SIGNAL PROCESSING ELECTRONICS 15
ELECTRONIC IMAGE SENSOR 12
OPTICAL SYSTEM 10
LENS 24
APERTURE 26
OPERATOR CONTROL UNIT
MODE SELECT 20
RECORD 22
CAMERA CONTROL PROCESSOR UNIT 14

FIG. 1

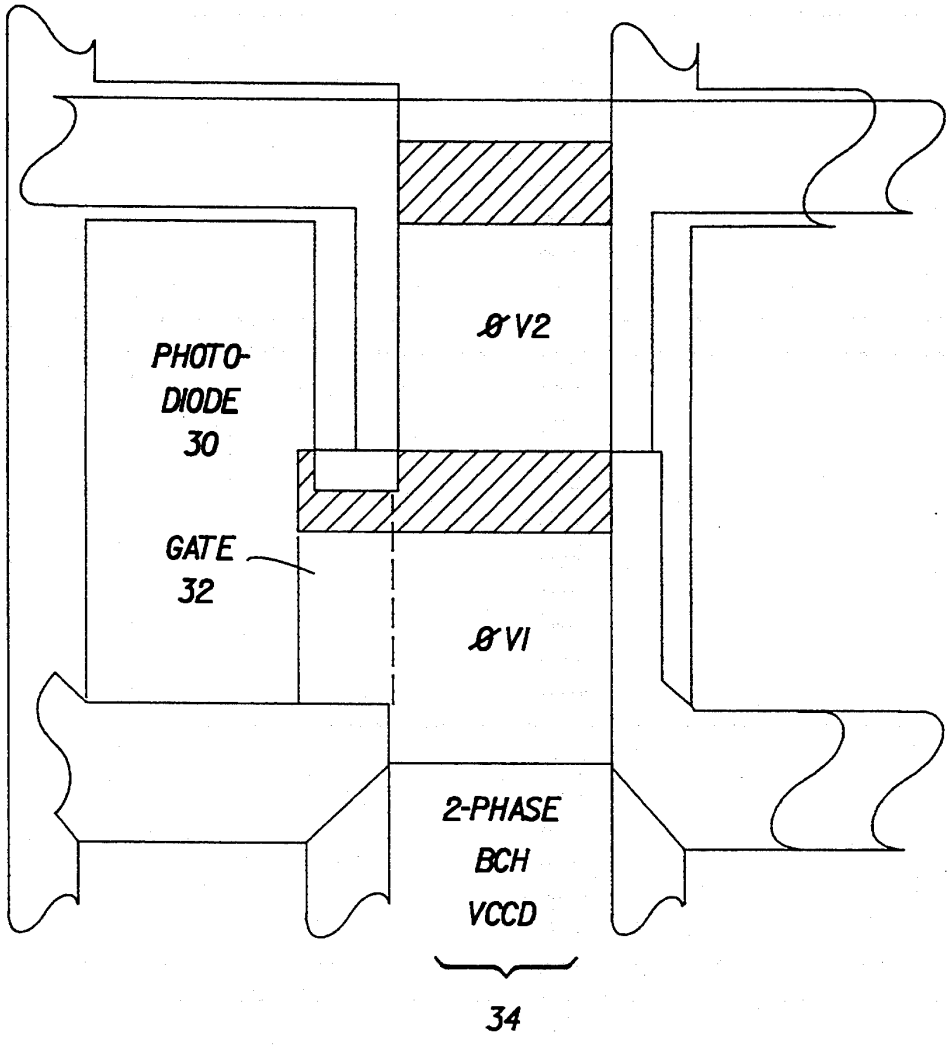


FIG. 2

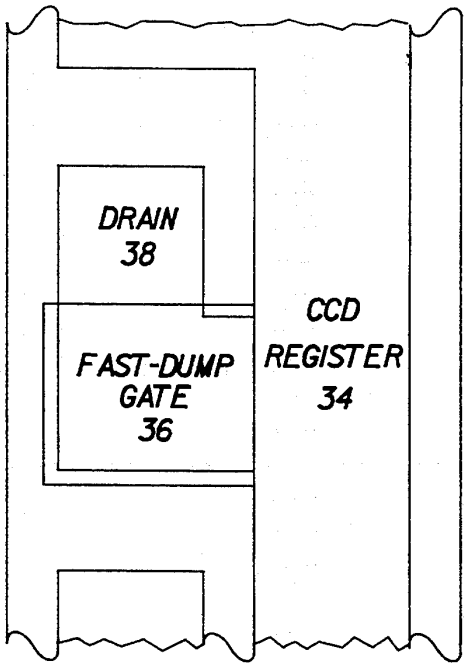
DRAIN
38
FAST-DUMP
GATE
36
CCD
REGISTER
34

FIG. 3

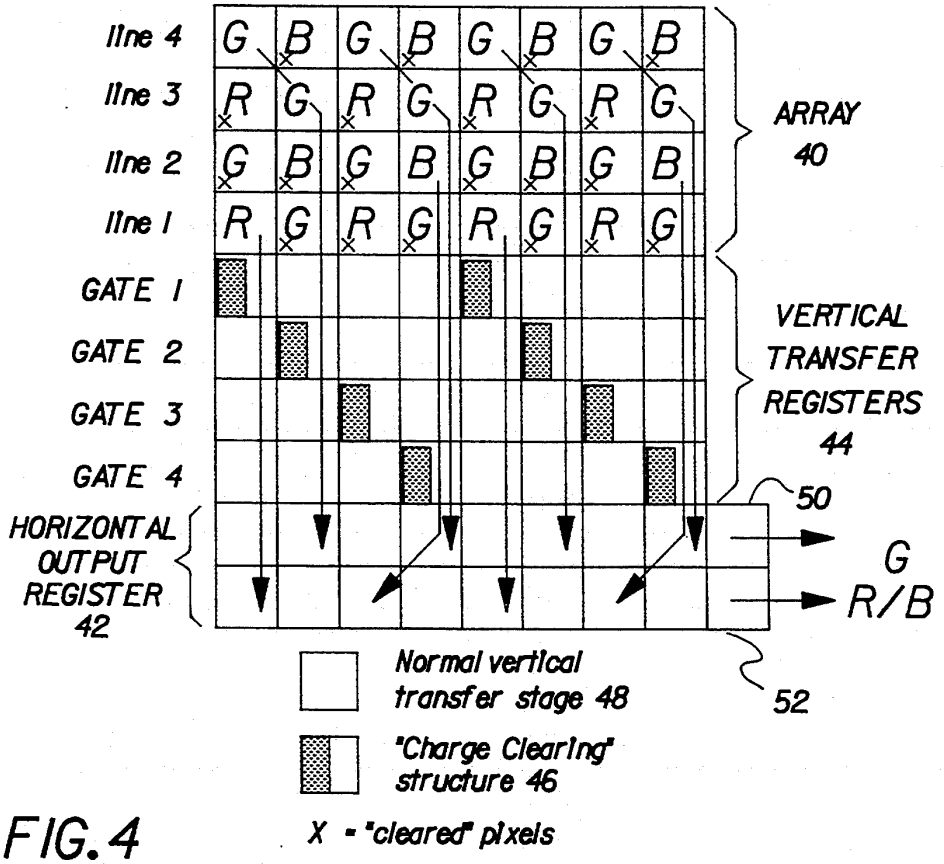
line 4
line 3
line 2
line 1
GATE 1
GATE 2
GATE 3
GATE 4
HORIZONTAL
OUTPUT
REGISTER
42
ARRAY
40
VERTICAL
TRANSFER
REGISTERS
44
50
52
G
R/B
Normal vertical
transfer stage 48
"Charge Clearing"
structure 46
X = "cleared" pixels

FIG. 4

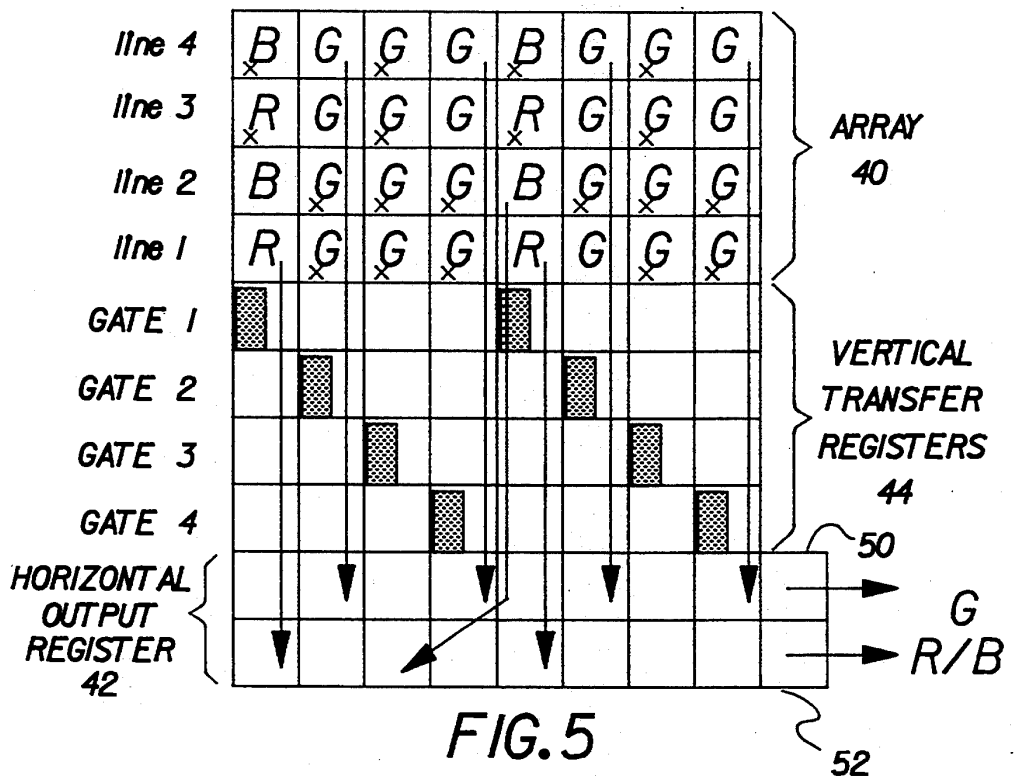
line 4
line 3
line 2
line 1
B G G G B G G G
R G G G R G G G
B G G G B G G G
R G G G R G G G
ARRAY 40
GATE 1
GATE 2
GATE 3
GATE 4
VERTICAL TRANSFER REGISTERS 44
50
HORIZONTAL OUTPUT REGISTER 42
G
R/B
52

FIG. 5

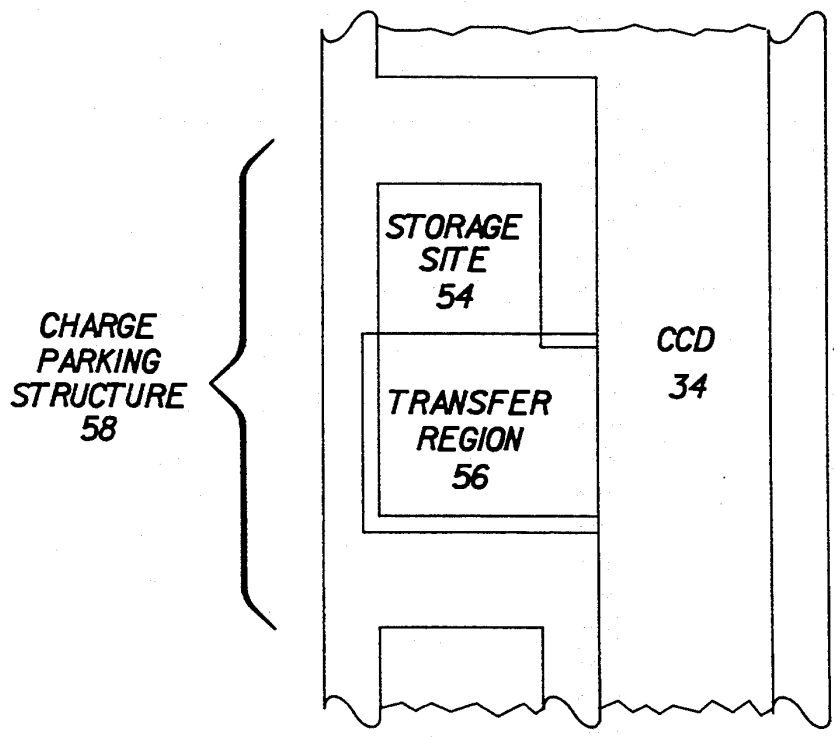
CHARGE PARKING STRUCTURE 58
STORAGE SITE 54
TRANSFER REGION 56
CCD 34

FIG. 6

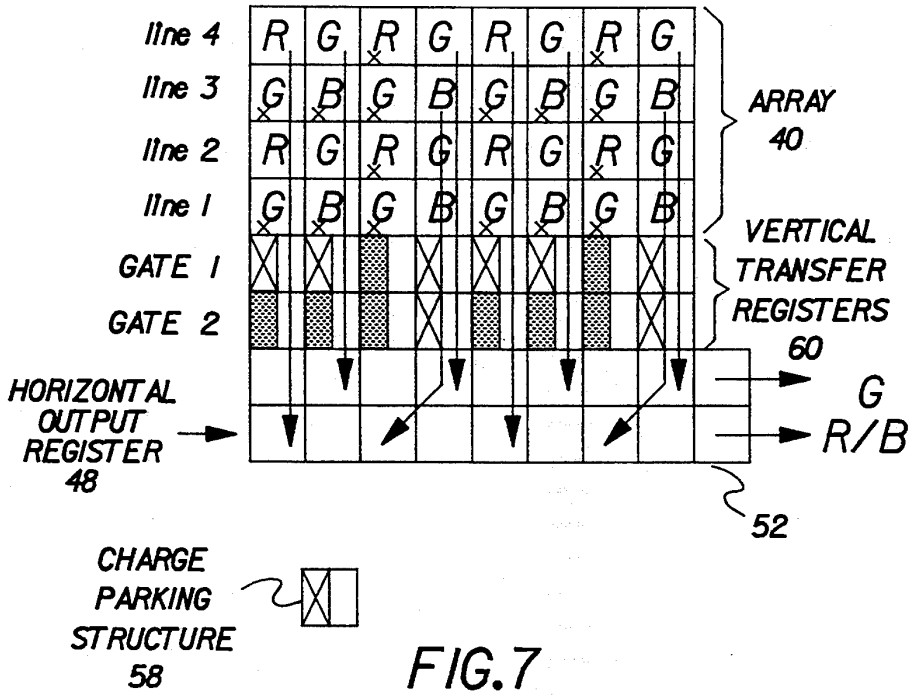
line 4
line 3
line 2
line 1
GATE 1
GATE 2
R G R G R G R G
G B G B G B G B
R G R G R G R G
G B G B G B G B
ARRAY 40
VERTICAL TRANSFER REGISTERS 60
HORIZONTAL OUTPUT REGISTER 48
G
R/B
52
CHARGE PARKING STRUCTURE 58

FIG.7

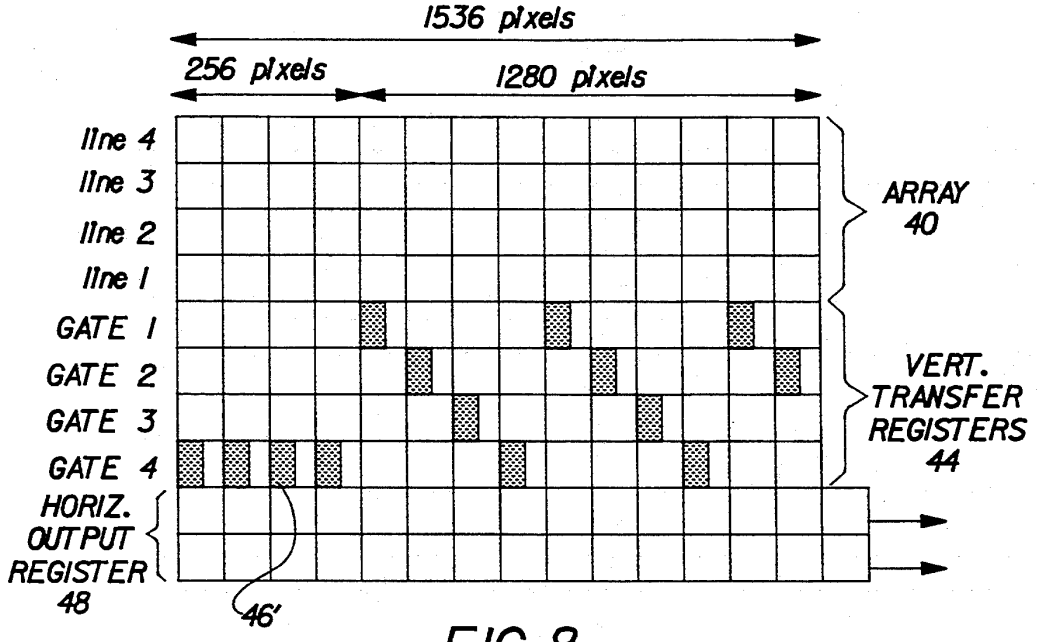
1536 pixels
256 pixels
1280 pixels
line 4
line 3
line 2
line 1
GATE 1
GATE 2
GATE 3
GATE 4
ARRAY 40
VERT. TRANSFER REGISTERS 44
HORIZ. OUTPUT REGISTER 48
46'

FIG.8

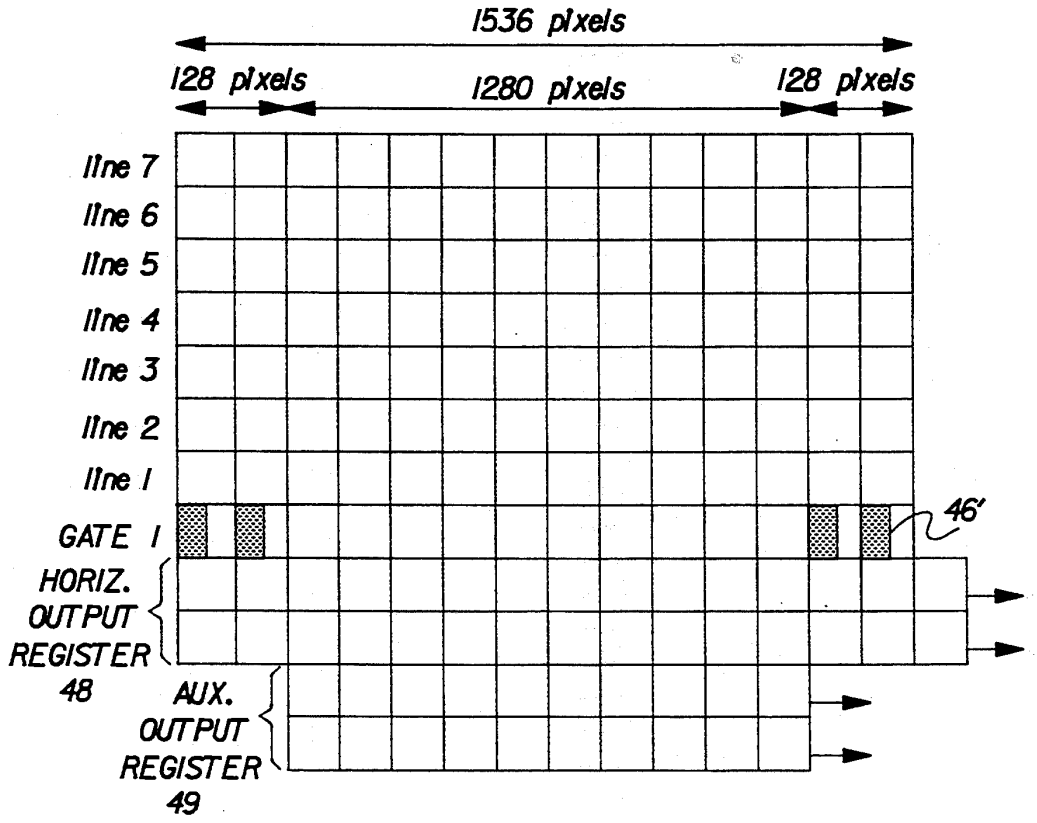
1536 pixels
128 pixels
1280 pixels
128 pixels
line 7
line 6
line 5
line 4
line 3
line 2
line 1
GATE 1
46'
HORIZ. OUTPUT REGISTER 48
AUX. OUTPUT REGISTER 49

FIG. 9

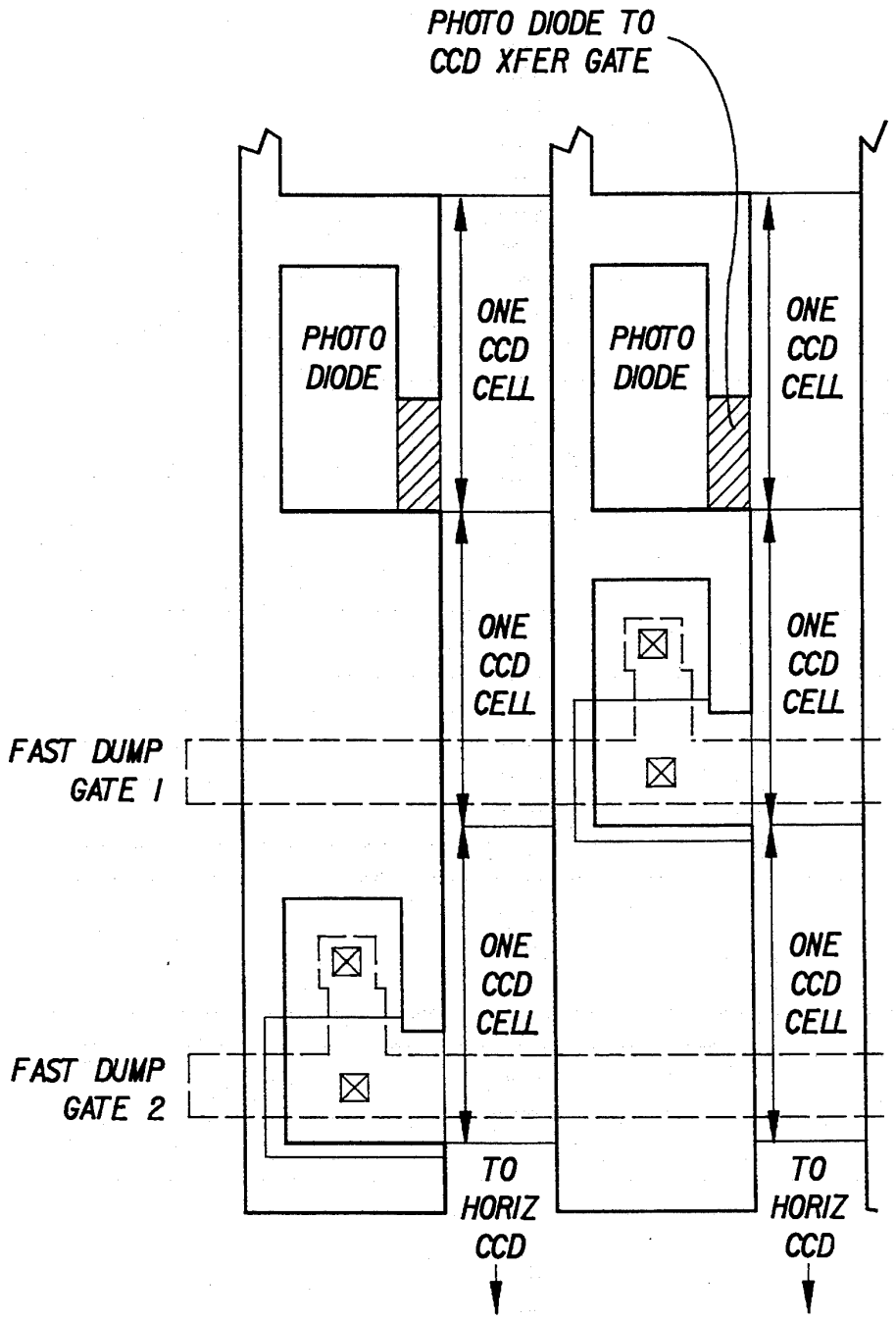
PHOTO DIODE TO CCD XFER GATE
PHOTO DIODE
ONE CCD CELL
PHOTO DIODE
ONE CCD CELL
ONE CCD CELL
ONE CCD CELL
FAST DUMP GATE 1
ONE CCD CELL
ONE CCD CELL
FAST DUMP GATE 2
TO HORIZ CCD
TO HORIZ CCD

FIG. 10

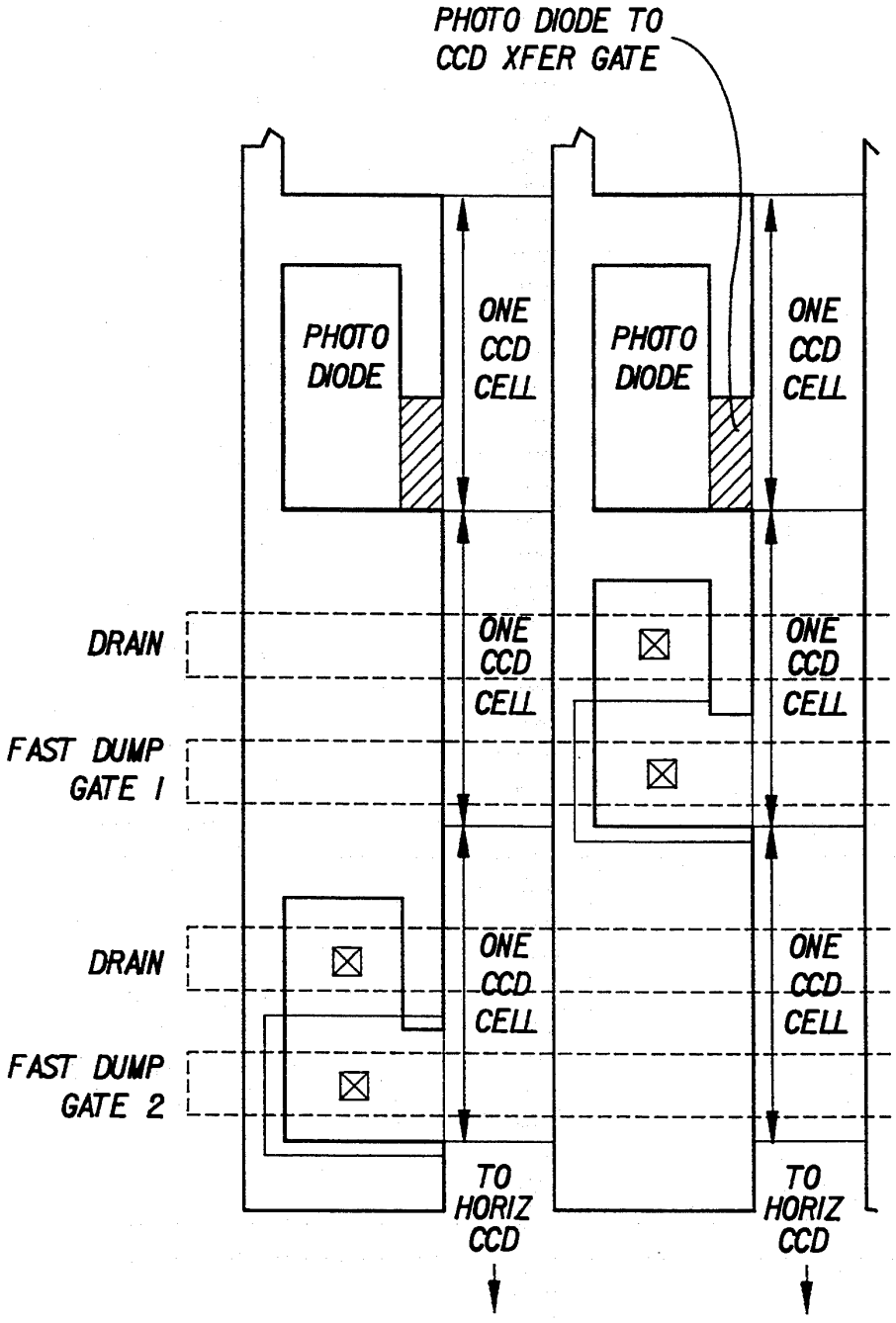
PHOTO DIODE TO CCD XFER GATE
PHOTO DIODE
ONE CCD CELL
PHOTO DIODE
ONE CCD CELL
DRAIN
ONE CCD CELL
ONE CCD CELL
FAST DUMP GATE 1
DRAIN
ONE CCD CELL
ONE CCD CELL
FAST DUMP GATE 2
TO HORIZ CCD
TO HORIZ CCD

FIG. 11

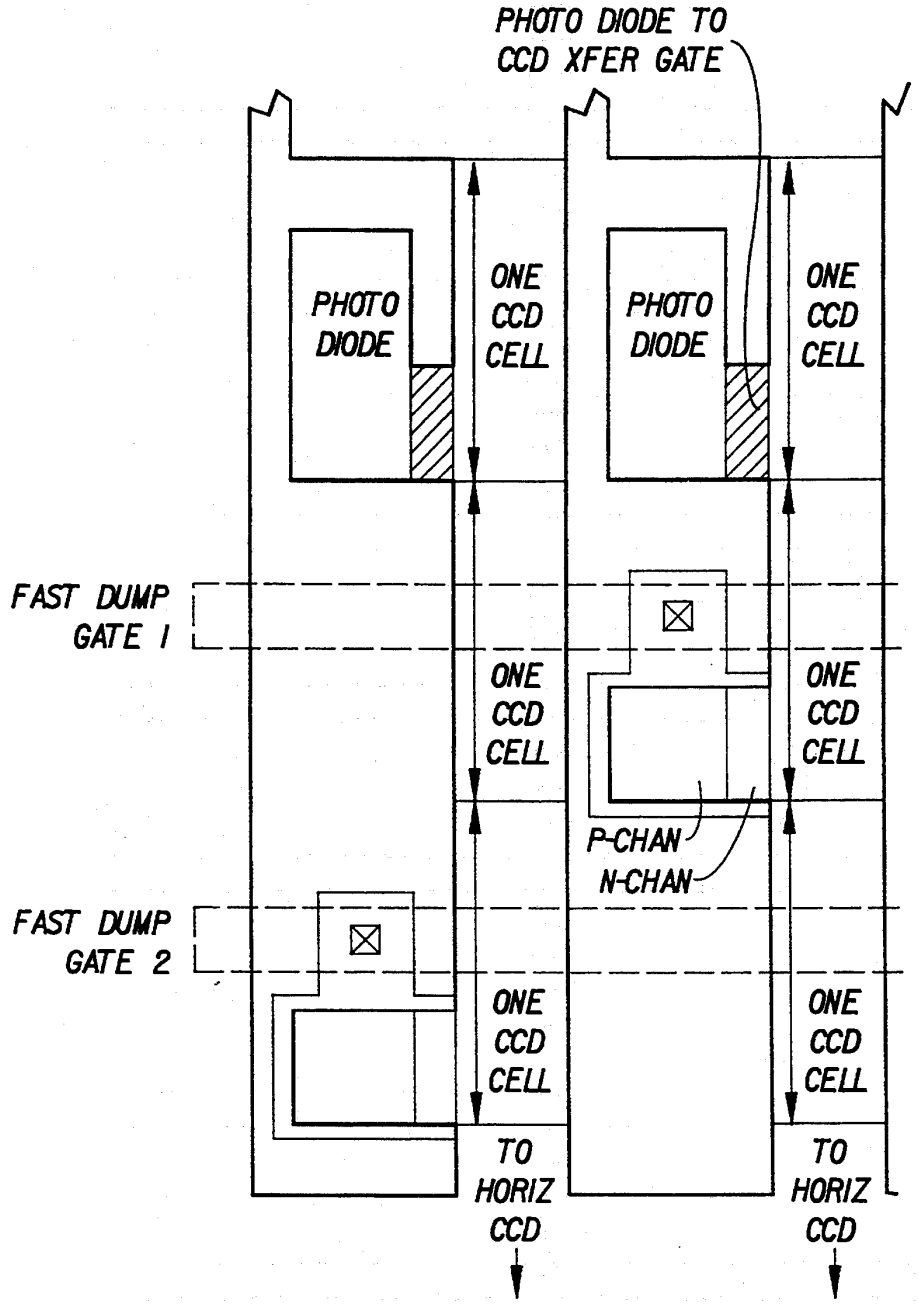
PHOTO DIODE TO CCD XFER GATE
PHOTO DIODE
ONE CCD CELL
PHOTO DIODE
ONE CCD CELL
FAST DUMP GATE 1
ONE CCD CELL
ONE CCD CELL
P-CHAN
N-CHAN
FAST DUMP GATE 2
ONE CCD CELL
ONE CCD CELL
TO HORIZ CCD
TO HORIZ CCD

FIG. 12

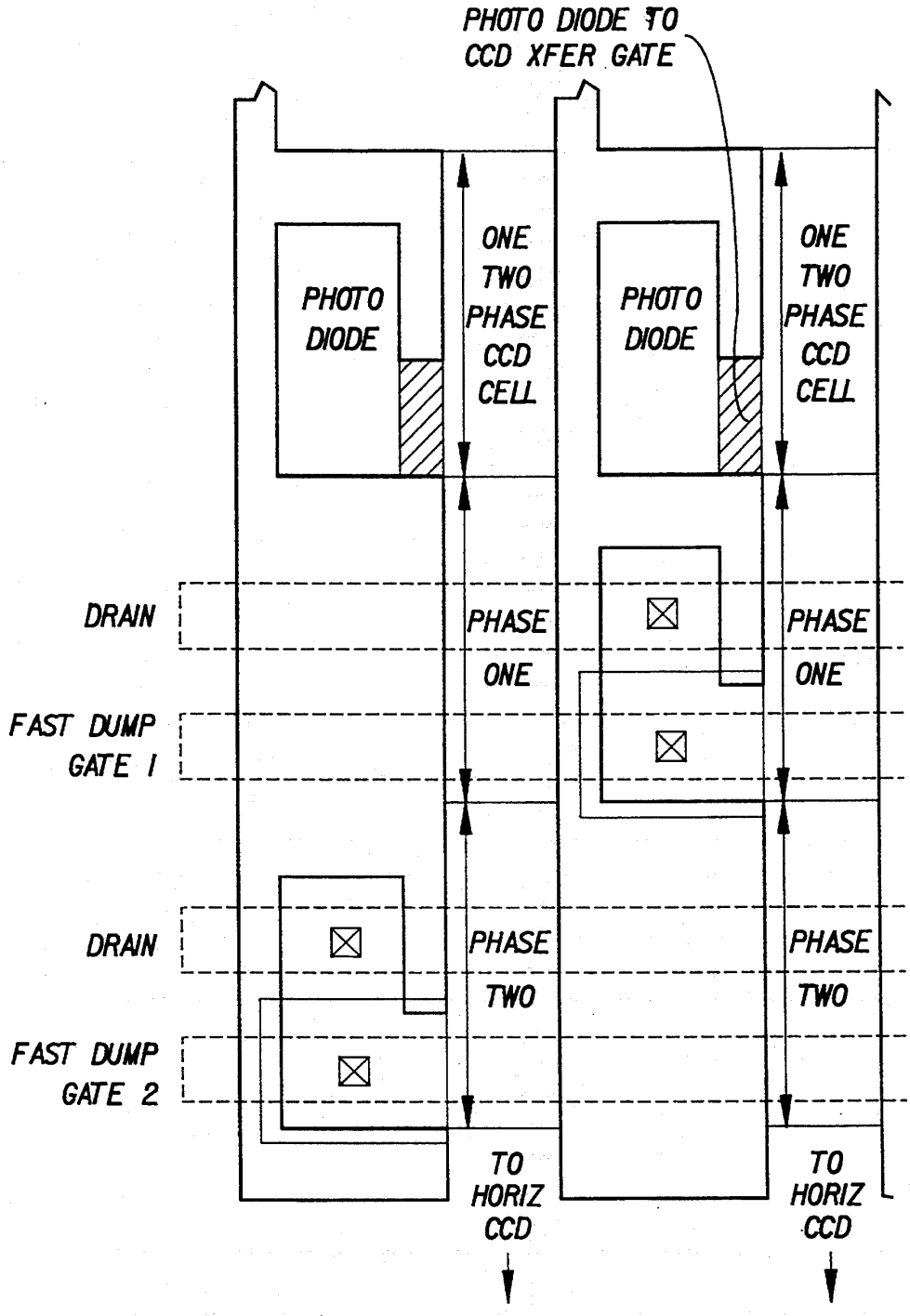
PHOTO DIODE TO CCD XFER GATE
PHOTO DIODE
ONE TWO PHASE CCD CELL
PHOTO DIODE
ONE TWO PHASE CCD CELL
DRAIN
PHASE ONE
PHASE ONE
FAST DUMP GATE 1
DRAIN
PHASE TWO
PHASE TWO
FAST DUMP GATE 2
TO HORIZ CCD
TO HORIZ CCD

FIG.13

# MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS

## FIELD OF THE INVENTION

The invention relates generally to an electronic imaging system. More specifically, the invention relates to an electronic imaging system for capturing images in both a motion mode and a still mode, wherein the electronic imaging system captures medium resolution motion images at a standard frame rate and high resolution still images at a much lower frame rate.

## BACKGROUND OF THE INVENTION

Motion/still electronic imaging systems including the capability of recording analog motion images and digital still images on the same recording medium, for example 8 mm or VHS format magnetic tape, have recently been developed by a number of manufacturers. The motion/still camcorders currently available record motion images in the same manner as conventional motion only video recording cameras. In order to record still images, the user activates an operator control to switch to a "still" mode of operation in which image data generated from the systems electronic image sensor is temporarily stored in a digital memory for subsequent recording onto videotape.

Conventional motion/still camcorders utilize the same type of NTSC resolution interlaced electronic image sensors originally developed for motion only electronic camera systems. Although the conventional image sensors provide sufficient data to produce relatively low resolution analog NTSC signals, the image sensors are not capable of generating still images having the high resolution associated with high quality electronic still imaging systems. Some current electronic still imaging systems, for example, are capable of recording over one thousand lines of image information, while only 480 lines of image information are required for one frame of an NTSC video signal.

Of course, a high definition television (HDTV) electronic image sensor could be used in a motion/still camcorder to directly obtain high resolution still images and HDTV motion images, but downconversion would be required to obtain NTSC motion images. In such a case, the electronic image sensor must be capable of operating at pixel data rates of greater than 50M pixels/-second. Electronic image sensors capable of operating at such high pixel data rates, however, are typically very costly to produce and have much higher power consumption rates than conventional NTSC compatible sensors.

In view of the above, it is an object of the invention to provide an electronic imaging system that is capable of producing NTSC motion images and high resolution still images. It is a further object of the invention to provide an electronic image sensor for the electronic imaging system, which can be operated in a low resolution mode to provide NTSC resolution motion scenes at the standard thirty frames/second rate, and operated in a high resolution mode to provide high resolution still images at slower frame rates. It is a still further object of the invention to provide an electronic image sensor, as described above, that is less expensive to produce and has lower power consumption requirements than HDTV electronic image sensors.



## SUMMARY OF THE INVENTION

The invention provides an electronic imaging system that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate.

The electronic imaging system utilizes an electronic image sensor that includes an array of photosensitive picture element sites, or "pixels" which collect photo-generated charge packets. Each charge packet is a pixel image signal. Image signals are generated from all of the pixels in the still mode of operation. In the motion mode of operation, however, the image signals generated from certain selected pixels are discarded or combined with the signals from nearby pixels in order to generate images at thirty frames per second while using a standard video rate output pixel clock (approximately 12 MHz) instead of an HDTV rate pixel clock (>50 MHz). The electronic image sensor incorporates column selective fast dump "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from non-adjacent vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail with reference to the accompanying drawings wherein:

FIG. **1** is a block diagram of an electronic imaging system in accordance with the invention;

FIG. **2** illustrates an image pixel site of the type incorporated in the electronic image sensor shown in FIG. **1**;

FIG. **3** illustrates a charge clearing structure of the type incorporated in the electronic image sensor shown in FIG. **1**;

FIG. **4** illustrates a first embodiment of the electronic image sensor shown in FIG. **1**;

FIG. **5** illustrates the use of a different color filter array with the electronic image sensor structure shown in FIG. **4**;

FIG. **6** illustrates a charge parking structure utilized in a second embodiment of the invention;

FIG. **7** illustrates an electronic image sensor in accordance with a second embodiment of the invention that utilizes the charge parking structure illustrated in FIG. **6** and the charge clearing structure illustrated in FIG. **3**;

FIG. **8** illustrates a third embodiment of the invention that incorporates aspect ratio conversion;

FIG. **9** illustrates a fourth embodiment of the invention that incorporates aspect ratio conversion;

FIGS. **10–12** illustrate three methods of creating column selectable "charge clearing" structures using 2 CCD phases per row; and

FIG. **13** illustrates a "charge clearing structure using 1 CCD phase per row.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A motion/still electronic imaging system according to the invention is illustrated in FIG. **1**. The imaging system includes an optical system **10**, a motion/still

electronic image sensor **12**, a camera control processor unit **14**, signal processing electronics **15**, a recording unit **16**, and an operator control unit **18**, which includes a mode selection switch **20** and a record or "shutter" control switch **22**. An optional flash unit may also be incorporated in the structure of the imaging system or as an accessory item. The optical system **10** of the illustrated embodiment includes a lens **24**, and an adjustable aperture **26**, which are controlled by the camera control processor unit **14**. It will be understood that the invention is not limited to the use of illustrated optical system **10**, but is also applicable to imaging systems using any type of known optical system, including those using fixed apertures and systems that utilize mechanical shutter devices.

In operation, a user places the mode switch **20** in a "motion" mode position and depresses the record switch **22** to record motion images. The camera control processor unit **14** controls the operation of the electronic image sensor **12**, the signal processing electronics **15**, and the recording unit **16** in order to record the output of the electronic image sensor. The recording unit **16** preferably includes a digital magnetic tape recording unit, so that the processed sensor output signal is recorded on a magnetic tape located in the recording unit **16** as an NTSC resolution video image sequence until the record switch **22** is released. To record a still image, the user places the mode switch **20** into the "still" mode position, so that a high resolution still image is captured and recorded by the recording unit **16** each time the record switch **16** is depressed. The recording unit **16** preferably includes digital memory means for storing the still images (for example Flash EPROM memory cards) in addition to the magnetic tape recording unit, although the still images can also be stored on tape if desired.

The electronic image sensor **12** includes a row and column array of pixels that generate signal in response to the amount of radiation incident thereon and at least one horizontal output register. A conventional color filter array (not shown) is provided so that selected pixel sites generate image signals corresponding to red, green and blue color components. In addition to the photosensitive pixels, the electronic image sensor includes column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain pixels, while the charge parking structures are used to add the charge from non-adjacent vertical pixels.

FIG. **2** illustrates a top view of one photosensitive pixel of the type included in the array of the electronic image sensor **12**. The pixel is of conventional construction, and is preferably of the type incorporated in the KAI-1001 interline image sensor manufactured by the Eastman Kodak Company of Rochester, N.Y. The design and operation of this image sensor is described in "KAI-1001 series Megapixel Interline CCD Image Sensor Performance Specification, " Rev. 1 April 1993, available, from the Microelectronics Technology Division of Eastman Kodak Company, and in "A 1 Megapixel, Progressive-Scan Image Sensor with Anti-blooming Control and Lag-Free Operation" by E. G. Stevens, et al., IEEE Trans. Electron Devices, Vol. 38, May 1991, both of which are incorporated by reference herein. The 9×9 micron pixel site includes a photodiode **30**, a transfer gate **32** and a two-phase CCD register **34**. The operation of the photosite is well known in the art and need not be discussed in great detail.

FIG. **3** illustrates a top view of one of the charge clearing structures incorporated in the electronic image sensor **12**. The charge clearing structures are located in selected columns of at least one row of vertical transfer registers located between the two-dimensional array of photosites and a horizontal output register of the electronic image sensor **12** as will be described in greater detail below. The charge clearing structure includes a fast dump gate **36** and a drain **38** located adjacent to the CCD register **34**. The fast dump gate **36**, when activated, permits charge being transferred in the CCD register **34** to be dumped to the drain **38**. The drain **38** may be a separate electrode, as shown in FIG. **11**, or, as shown in FIG. **10**, it may contact a polysilicon and a metal drain line connected via a bond wire to an external control pin on the sensor package, which is held at an appropriate potential so as to drain the charge from CCD register **34**.

FIGS. **10–12** show different charge clearing structures using one true two-phase CCD cell per row. It is also possible to use charge clearing structures having only one of the two CCD cells per row. This reduces the number of vertical transfer required to transfer the first line of charge from the photosensitive pixel array to the horizontal readout register. FIG. **10** illustrates the use of a surface-channel, fast-dump gate ($V_T>0$) so that the drain may be connected to the gate, thereby saving a pin. FIG. **11** shows a structure providing a separate gate and drain electrode, as would be required for a buried-channel, fast-dump gate ($V_T>0$). FIG. **12** shows a charge-clearing structure of a vertical type wherein the drain **38** lies below the gate (the n-type substrate). FIG. **13** shows a charge-clearing structure similar to that of FIG. **11**, except that the gate **1** row charge clearing structure is adjacent to phase one of a two phase CCD cell, and the gate **2** row charge clearing structure is adjacent to phase two of the same CCD cells whereas in FIG. **11**, each charge clearing structure is adjacent to a two phase CCD cell.

A preferred image sensor architecture incorporating photosensitive pixels of the type illustrated in FIG. **2** and charge clearing structures of the type illustrated in FIG. **3** is shown in FIG. **4**. For purposes of simplification, an array **40** of image pixel sites is shown having just four image lines, although it will be understood that any number of image lines of any desirable length may be employed. The four image lines are separated from a horizontal output register **42** by four rows of vertical transfer registers **44**, wherein each row of vertical transfer registers **44** includes at least one charge clearing structure **46** and a plurality of normal or conventional vertical transfer stages **48**. The charge clearing structures **46** in each row of vertical transfer registers **44** are respectively controlled by "gate **1**", "gate **2**", "gate **3**" and "gate **4**" signals supplied by the camera control processor unit **14** illustrated in FIG. **1**. The image pixel sites are arranged in accordance with a Bayer color filter array pattern as described in U.S. Pat. 3,971,065, "Color Imaging Array" by B. E. Bayer, assigned to Eastman Kodak Co. and incorporated herein by reference, with green photosites arranged in a checkerboard pattern and red and blue pixels arranged on alternate lines. The horizontal output register **42** includes a first horizontal transfer register **50** for green image pixel signals and a second horizontal transfer register **52** for red and blue image pixel signals.

In operation, signal charge packets from each of the lines of photoactive pixels are clocked through the four rows of vertical transfer registers **44** including the charge clearing structures **46**. When a given line is clocked from the imaging array into the "gate **1**" row of vertical transfer registers **44**, for example, the signal charge from the first and fifth columns of the line is transferred to the drains **38** of the charge clearing structures **46** if the gate **1** signal is activated. In all other columns of the line (for example columns **2, 3, 4, 6, 7**) the signal charge is unaffected. If the gate **1** signal is turned off, the charge clearing structures **46** in the gate **1** row of vertical transfer registers **44** are disabled, and the signal charge packets transferred from the array **40** to the gate **1** row are unaffected. By incorporating four "charge clearing" rows having charge clearing structures **46** offset in different columns, it is possible to eliminate all of the signal charge packets from a given image line by turning on the "clear" signals as the line of image pixel signals passes through the gate **1**, gate **2**, gate **3** and gate **4** vertical transfer rows **44**.

In a still mode of operation, all of the charge clearing structures **46** are disabled, thereby allowing all of the signal charge packets to be clocked into the horizontal output register **42**. The green image pixel signals are subsequently clocked out of the first horizontal transfer register **50** and the red and blue image pixel signals are clocked out of the second horizontal transfer register **52**. The color filter array pattern is designed to provide the best image possible in the high resolution still mode of operation.

An NTSC resolution image is obtained in a motion mode of operation by selectively activating the charge clearing structures **46**. As line one of the image passes through the vertical transfer registers **44**, gate **1** is turned off, but gate **2**, gate **3** and gate **4** are turned on. Thus, only the red image pixel signals associated with every other odd column, i.e. columns **1, 5, 9**, etc., are transferred to the horizontal output register **42**. The image pixel signals representing the green pixels and the alternate red pixels of line one are drained off by the activated charge clearing structures **46**. In order to read out image line **2**, the gate **4** signal is turned off and the other three signals are turned on, thus passing every other blue image pixel signal to the horizontal output register **42**. Following the transfer of the blue image pixel signals, the second horizontal transfer register is clocked once to put the blue pixels in their proper location. All of the green image pixel signals for the third image line are kept by deactivating all of the charge clearing structures **46** as the third image line is clocked through the rows of vertical transfer registers **44**. The fourth line of image pixel signals can either be eliminated by turning on all four gate signals or can also be passed to the first horizontal transfer register **50** and summed with the green pixels from the other image lines. The next field of the NTSC signal is "staggered" vertically by shifting the sampling by two lines in the vertical direction.

FIG. **5** shows how the same basic image sensor architecture illustrated in FIG. **4** can be used with a different color filter array pattern, for example a "3G" non-interlaced striped CFA, as described in U.S. Pat. No. 4,663,661 "Single Sensor Color Video Camera with blurring filter" by J. S. Weldy and S. H. Kristy, assigned to Eastman Kodak Company and incorporated herein by reference, to generate an NTSC signal. In this example, the red and blue image pixel signals are clocked into the horizontal output register **42** by turning off the gate **1** signal and turning on the gate **2**, gate **3** and gate **4** signals. The second horizontal transfer register **52** is clocked twice before summing. The third and fourth image lines are clocked into and summed in the horizontal output register by turning off the gate **2** and gate **4** signals and turning on the gate **1** and gate **3** signals. The fourth image lines can alternatively be discarded by turning on the gate **2** and gate **4** signals. As in the case illustrated in FIG. **4**, a still mode of operation is obtained by deactivating all of the gate signals.

Referring now to FIG. **6**, a charge "parking" or storage structure **58** is shown including a storage site **54** and a transfer gate or region **56** located adjacent to the CCD register **34**. The charge parking structure **58** is used in conjunction with the charge clearing structure **46** described above in a second embodiment of the invention. In operation, the transfer region **56** of the charge parking structure **58** is activated to transfer a signal charge packet from the CCD register **34** to the storage site **54**. The storage site **54** can be used to sum signals from different non-adjacent rows of the array of pixels.

The charge is stored by setting the channel potential of the storage site **54** to a higher potential than the transfer region **56**, which is likewise at a higher channel potential than the adjacent CCD register **34**. To later sum the stored charge with a non-adjacent row of charge which has been shifted into CCD register **34**, the channel potential of the CCD register **34** must be brought higher than that of the transfer region **56**, which must be higher than that of the storage site **54**. Otherwise, during readout of CCD register **34**, the transfer region **56** is brought to a lower channel potential than in CCD register **34** or the storage site **54** to create a barrier and prevent the transfer of charge between them.

FIG. **7** illustrates an electronic image sensor in accordance with a second embodiment of the invention. The image sensor is shown having four image lines and two rows of vertical transfer registers **60** which include both charge clearing structures **46** and charge parking structures **58**. As in the structure illustrated in FIG. **5**, electronic image sensor also includes a horizontal output register **42** having first and second horizontal transfer registers **50, 52** as shown in FIGS. **4** and **5**.

In operation, the charge clearing structure **58** location in column four of the gate **2** row, for example, allows the blue pixel values from image line one and image line three to be summed, even though there is a green pixel value between these two blue values. To obtain an NTSC resolution image, image lines **1** and **2** are clocked into the gate **1** and gate **2** rows. In the gate **2** row, the image line **1** blue pixel values from columns **4, 8**, etc. are parked or stored while the green pixels and the remaining blue pixels are cleared discarded. In the gate **1** row, the green pixels and alternate red pixels are parked while the remaining red pixels are discarded or cleared. Image lines three and four are subsequently clocked into the gate **1** and gate **2** rows. In the gate **2** row, the line **3** blue pixel values from columns **4, 8** etc. are summed with the line one blue pixel values, while the green pixels and the remaining blue pixels are cleared. In the gate **1** row, the line **4** red pixel values from columns three and seven etc are cleared, while the green pixels and the remaining red pixels are summed with the values in the charge parking registers. Finally, the image pixel signals are transferred into the horizontal output register.

One additional problem with NTSC motion/still systems is that it may be desirable to use different image aspect ratios for the motion and still modes. For example, NTSC uses a 4:3 aspect ratio image, while the requirement for high resolution stills may be a 3:2 aspect ratio as utilized, for example, in the Kodak Photo CD System. The electronic image sensor is therefore required to have a 1024×1536 image array to provide a 3:2 aspect ration, while for the NTSC mode, it might be desirable to use only 960×1280 pixels from the electronic image sensor to provide a 4:3 aspect ratio image.

A method of facilitating the readout of different aspect ratio images is shown in FIG. **8**. The structure shown in FIG. **8** utilizes **256** "aspect ratio charge clearing" structures **46'** of the type shown in FIG. **3** placed in the end of at least one row of the vertical transfer registers **44**, between the image array **40** containing the photosensitive pixels, and the horizontal output register **48**. When activated by a signal supplied by the camera control processor unit **14**, the aspect ratio charge clearing structures **46'** eliminate the signals from the columns at the left side of the image array **40** as the image lines are clocked out. As a result, the horizontal output register **48** does not receive charge from these columns.

It should be noted that there is insufficient time to clock out all of the **256** extra pixels at the end of each NTSC image line, so that charge from these extra pixels would end up at the right hand side of the horizontal readout register **48** without the use of the aspect ratio charge clearing structures **46'**. In such a case, this charge would be added to the right side of the next new line of the image causing a serious artifact. The aspect ratio charge clearing structures **46'** eliminate the signals from these pixels so that the next image line contains only the proper signal charge, namely, only the 1280 horizontal pixels needed to be clocked out.

A second embodiment that compensates for the differences in aspect ratios is shown in FIG. **9**. The second structure utilizes a second auxiliary horizontal output register **49**. The second horizontal output register **49** is centered in the middle of the image array **40** and has 256 fewer elements than the normal horizontal output register **48**. Aspect ratio charge clearing structures **46'** are used to dispose of the charge in the first and last 128 columns of the image array which are not used in the NTSC readout mode.

The invention has been described with reference to certain preferred embodiments thereof. It will be understood, however, that modifications and variations are possible within the scope of the appended claims. For example, the aspect ratio charge clearing structures need not be located within the same row of vertical transfer registers, but can be located in several rows if desired.

## INDUSTRIAL UTILITY

The invention can be utilized in electronic imaging systems to permit high resolution still images to be produced at low frame rates, while also allowing standard NTSC motion image signals to be produced by the same system. The invention is particularly applicable to commercial camcorder devices.

What is claimed is:

**1**. An electronic image sensor comprising:

a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation; a horizontal output register; and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register;

wherein the vertical transfer means includes pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

**2**. The electronic image sensor of claim **1**, wherein the vertical transfer means further comprises charge parking means for temporarily storing signal charge from at least one of the columns of each row of the array of photosensitive pixels, wherein signal charge packets from multiple rows of the array are summed in the charge parking means.

**3**. The electronic image sensor of claim **1**, wherein the horizontal output register includes first and second horizontal transfer registers.

**4**. The electronic image sensor of claim **1**, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

**5**. The electronic image sensor of claim **4**, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

**6**. The electronic image sensor of claim **1**, wherein the row and column array of vertical transfer registers comprises at least four rows.

**7**. An electronic imaging system comprising:

an electronic imaging sensor; an optical system for imaging scene light onto the electronic imaging sensor; a camera control processor coupled to the electronic imaging sensor; an operator control unit coupled to the camera control processor; and an image data storage unit coupled to the output of the electronic imaging sensor;

wherein the camera control processor controls the electronic imaging sensor to operate in either a still image mode or a motion image mode in response to a mode signal received from the operator control unit;

wherein the electronic imaging sensor comprises a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation, a horizontal output register, and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register, said vertical transfer means including pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

**8.** The electronic imaging system of claim **7**, wherein the vertical transfer means further comprises charge parking means for temporarily storing signals from at least one of the columns of each row of the array of pixels, wherein signals from multiple rows of the array are summed in said charge parking means.



**9.** The electronic imaging system of claim **7**, wherein the horizontal output register includes first and second horizontal transfer registers.

**10.** The electronic imaging system of claim **7**, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

**11.** The electronic imaging system of claim **10**, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

**12.** The electronic imaging system of claim **7**, wherein the row and column array of vertical transfer registers comprises at least four rows.

* * * * *

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(11) EP 0 720 387 A2

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## (54) Method and apparatus for providing interlaced images from a progressive scan sensor in an electronic camera

(57) Interlaced images are generated in an electronic camera from a progressive scan sensor (20) employing a mosaic color filter array pattern. A timing and control section (27) operates the camera in two modes, including a high quality progressive scan still mode for capture of still images and a pseudo-interlaced video resolution mode for driving a color viewfinder display (10). In the latter mode, the timing and control section (27) enables a fast dump structure (72) on the sensor (20) to eliminate two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to its horizontal register (70) for readout, thereby generating a pattern of lines suitable for interlaced readout. More specifically, the mosaic pattern of the color filter array is preserved in the interlaced readout for faithful color reproduction on the viewfinder display (10).

FIG. 4A

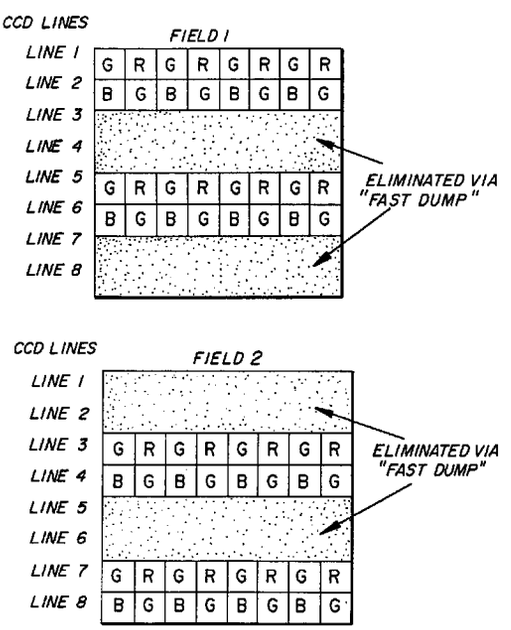



FIG. 4B

EP 0 720 387 A2

## Description

### FIELD OF THE INVENTION

The invention pertains to method and apparatus for providing interlaced images from a progressive scan sensor in an electronic camera, and, more particularly, to providing interlaced video motion images from a progressive scan sensor used in an electronic camera that also produces high quality still images.

### BACKGROUND OF THE INVENTION

It is known to alter scanning lines in order to relate the video motion images applied to a monitor to the manner in which an image sensor is driven for other purposes. For instance, U.S. Patent No. 4,928,137 (Kinoshita) shows a still video sensing apparatus of the type that utilizes conventional NTSC video timing for image recording. The sensing apparatus includes an electronic monitor having a number of scanning lines fewer than the vertical picture elements of the image sensor. A driving circuit produces a non-interlaced output in the monitor mode by reading fewer scanning lines in the monitor mode than in an image sensing mode. The reduction of lines is obtained by summing charge in adjacent lines or by inhibiting transfer of alternate fields. This technique is particularly useful in operating a monochrome sensor, or in driving a monochrome viewfinder.

Progressive scan image sensors, such as the Kodak model KAI-0310CM imager, have been developed for high quality color electronic cameras. This sensor has approximately 480 active lines, and approximately 640 active pixels per line. A progressive scan sensor provides a higher quality still image than an interlaced sensor, since all lines are captured during the same interval of time. However, reading out an image from a progressive scan image sensor normally requires a clock rate of approximately twice that used with an interlaced image sensor, if the image is to be read out in the same period of time. For example, an NTSC format interlaced image sensor with 480 lines and 640 pixels per line requires a clock rate of approximately 12.2 MHz to read out the 640 lines in the 52.4 mSec NTSC standard active line time, which provides a field rate of 1/60 second. Since a progressive scan sensor, like the model KAI-0310CM imager, must read out twice as many lines per field, it must use a clock rate of about 24 mHz to read out all 480 lines in 1/60 second. This higher clock rate requires more expensive clock drivers, analog processing, and A/D conversion than interlaced sensors require.

One way to decrease the clock rate is to combine lines of charge from the image sensor. For example, if the image sensor is monochrome or the sensor columns are of the same color (i.e., a stripe color filter array), this can be done by summing two lines into the horizontal readout register, thus providing an interlaced output signal, if the summing is staggered by 1 line on alternate fields. Such a technique is useful in an electronic camera employing a viewfinder display which is used to compose the images (via a relatively low quality "motion" mode) before they are captured (in a much higher quality still mode). However, it is not possible to provide a color image from mosaic or "checker-board" color filter arrays using this technique, since the different color pixels will be summed together.

It is further possible to alter scanning lines by incorporating a selective charge clearing structure on the sensor. For instance, in Serial Number 08/203,237, entitled "Motion/Still Electronic Image Sensing Apparatus," (filed February 28, 1994 on behalf of the same assignee as the present application), charge clearing or "storage" structures are used to selectively discard the signal charge from certain color pixels or to combine the signal charge from nearby pixels to generate images at thirty frames per second while using a standard video rate output pixel clock instead of an HDTV rate pixel clock. In this way the same sensor can be used to generate both motion and still images for recording. Elimination of charge can also produce an interlaced output for a monochrome sensor if the pixels which are eliminated are whole lines staggered by 1 line on alternate fields. However, line elimination is unsuitable for many color filter patterns used on the sensor for color viewfinders. For example, if alternate lines are eliminated from the checkerboard pattern shown below

G R G R
B G B G
G R G R
B G B G

one field will contain only green (G) and red (R) pixels, and the next field will contain only blue (B) and green (G) values. Thus, it is not possible to create a full color image from a single field read-out in this manner. What is needed is a method for reading out the image sensor data in a manner that decreases the required clock rate while providing interlace pixel values for all colors within the same field.

### SUMMARY OF THE INVENTION

The invention was driven by the anomalous situation that the lower image quality operating mode of the system, the motion image processing, requires the higher clock rate, and thus the higher cost parts-clock drivers, analog processing, A/D converters, etc. By recognizing this anomaly, and by further understanding that "perfect" interlace symmetry is unnecessary for typical viewfinder motion applications, a cost-effective solution can be found.

Accordingly, the invention includes an image sensor comprising a two-dimensional array of photosites arranged in rows and columns, a plurality of vertical registers adjacent photosite columns for transferring rows of image charge from the photosites to a horizontal register for readout, and a charge drain structure interposed between the output of the vertical registers and the horizontal register for eliminating complete rows of image

charge at a time from the image sensor. A timing and control section controls the charge drain structure so as to eliminate two or more consecutive lines of image charge from the image sensor for every one or more lines of image charge that are transferred to the horizontal register for readout, thereby generating a pattern of lines suitable for interlaced readout.

The advantage of the invention is that it can be used in an electronic camera employing a color viewfinder display to compose the images (via a relatively low quality "motion" mode) at motion video rates without requiring high speed, and high cost, components (which are unnecessary for a much higher quality "still" mode that need not be run at motion video rates).

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, whereon

Figure 1 is a block diagram of an electronic camera incorporating a progressive scan sensor according to the invention;

Figures 2A and 2B are diagrams of progressive scan image sensors useful with the camera of Figure 1;

Figure 3 is a diagram of the Bayer color filter geometry for the sensor used with the camera of Figure 1;

Figure 4 shows a first pseudo-interlace pattern;

Figure 5 shows the line timing for the still mode of operation;

Figures 6A and 6B show the line timing for the first pseudo-interlace pattern shown in Figure 4;

Figure 7 shows a second pseudo-interlace pattern; and

Figure 8 shows the line timing for the second pseudo-interlace pattern shown in Figure 7.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A block diagram of a camera incorporating interlace processing according to the invention is shown in Figure 1. The camera includes an electronic color viewfinder display 10, for example, a color liquid crystal display or a color CRT display, and a user control section 12 having a number of user control buttons, including zoom buttons 14, a preview button 15 and a capture button 16. To take a still picture, the user turns on the camera (using a power switch (not shown), which may be automatically enabled when the user depresses the zoom buttons 14 or the preview button 15, or partially depresses the capture button 16). The user composes the picture by depressing the "zoom in" or "zoom out" buttons 14, and by adjusting the position of the camera, while observing the viewfinder image. When the user is satisfied with the composition on the viewfinder 10, the user depresses the capture button 16. The camera then captures a single still image, firing a flash 18 if necessary when the ambient illumination level is low. The still image is focused upon an image sensor 20 by a motor driven zoom lens 22. The intensity of the image light upon the sensor 20 is regulated by a motor driven mechanical aperture 24, while exposure time is regulated electronically by appropriate clocking of the sensor 20. The still image from the image sensor 20 is processed and digitally stored on a removable memory card 26.

Control of the sensor is provided by a timing and control section 27, which specifically includes a sensor timing circuit 28. The sensor timing circuit 28 provides the signals to enable sensor drivers 30, which provides horizontal clocks (H1, H2), vertical clocks (V1, V2), as well as a signal FDG for activating a drain structure on the sensor 20. The output of the image sensor 20 is amplified and processed in an analog gain and sampling (correlated double sampling (CDS)) circuit 32, and converted to digital form in A/D converter 34. The A/D output signal is provided via a high speed interface 56 to a processor section 35, which includes a digital processor 36 which temporarily stores the still images in a DRAM memory 38. The digital processor 36 then performs image processing on the still images, and finally stores the processed images on the removable memory card 26 via a memory card interface circuit 40, which may use the PCMCIA 2.0 standard interface. An EPROM memory 42 is used to store the firmware which operates the processor 36. The components of the processor section 35 are interconnected through a data bus 43, which also connects to the timing and control section 27 and to the card interface 40.

The motor driven zoom lens 22 includes a zoom motor 44, a focus motor 46, and an aperture motor 48 (all controlled by lens motor drivers 50). The timing and control section 27 further includes a control interface 52 connected to the lens motor drivers 50 and to a flash control circuit 53 via a photosystem interface block 54, which controls the operation of the zoom lens 22 and the flash 18. The lens zoom position is controlled by the photosystem interface block 54 based on position input from the zoom control buttons 14. Sensor data is passed to the processor section 35 through the high speed interface 56 in the timing and control section 27, and is also directed to the viewfinder 10 through a display driver 58.

The sensor 20 is a progressive scan interline image sensor (having a noninterlaced architecture), as shown in more detail in Figure 2A. The sensor comprises a two-dimensional array of photosites 66, e.g. photodiodes, arranged in rows and columns, a plurality of vertical registers 68 adjacent photosite columns for transferring rows of image charge from the photosites 66 to a horizontal register 70 for readout, and a charge drain structure (specifically, a fast dump structure 72) interposed between the output of the vertical registers 68 and the horizontal register 70 for eliminating complete rows of image charge at a time from the image sensor 20. A preferred image sensor is the Kodak model KAI-0310CM CCD image sensor, which has approximately 480 active lines with approximately 640 active pixels per line and an image aspect ratio of 4:3. This sensor is described in a

Performance Specification document available from Eastman Kodak Company, Rochester, New York. Each pixel measures 9 x 9 $\mu m^2$. The sensor uses a color filter array pattern known as the "Bayer checkerboard" pattern, described in U.S. patent 3,971,065, which is shown in Figure 3. Such a color filter array is characterized by a mosaic pattern in which the filter colors alternate in both line and column directions. In the normal operating mode, all of the pixels on the sensor are transferred to the horizontal register 70, which delivers the image signals to the analog gain and CDS circuit 32 (see Figure 1).

The sensor 20 uses a progressive scan readout method, which allows the entire image to be read out in a single scan. The accumulated or integrated charge for the photodiodes comprising the pixels 66 is transported from the photosites to light protected vertical (parallel) registers 68 by applying a large positive voltage to the phase-one vertical clock (V1). This reads out every row, or line, into the vertical registers 68. The charge is then transported from the vertical registers 68 to the horizontal register 70 by two-phase clocking of the vertical clocks (V1, V2). Between the vertical and horizontal registers is the fast dump structure 72, which is further described in the Performance Specification document for the KAI-0310CM sensor. The fast dump structure 72 includes a fast dump gate and a fast dump drain (not shown separately). By setting a suitable positive potential on a fast dump gate line FDG, charge from the row of pixel values currently adjacent to the fast dump structure 72 is transferred from the CCD channel directly into the fast dump drain rather than to the horizontal register 70. This dump, or line clear, is accomplished during the vertical-to-horizontal transfer time. When properly controlled by the sensor timing circuit 28, the fast dump structure 72 allows lines of charge to be eliminated. (A conventional use of the structure 72 is to eliminate stray charge in the vertical registers 68 during especially long integration times, and just before transfer of image charge to the vertical registers 68.)

As taught by the invention, the timing and control section 27 operates the electronic camera shown in Figure 1 in two modes, including a first, or normal, mode wherein all rows of signal charge corresponding to each line are progressively read out through the horizontal register 70 during a single scan, and a second mode wherein some of the rows of signal charge corresponding to some lines are eliminated through the fast dump structure 72 prior to readout. As applied to the embodiment of Figure 1, the first mode corresponds to a high quality still imaging mode while the second mode corresponds to a "pseudo" interlace scan mode for driving the viewfinder 10. (The second mode is referred to as "pseudo" because the interlace pattern produced is not an evenly spaced pattern.) In the second mode, the timing and control section 27 controls the fast dump structure 72 to eliminate two or more consecutive lines of image charge from the image sensor 20 for every one or more lines of image charge that are transferred to the horizontal register 70 for readout, thereby generating a pattern of lines suitable for interlaced readout. An interlaced video signal comprising two fields is generated either by alternating between two patterns of lines each obtained by eliminating two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register 70, or by simply repeating the line pattern twice. Other applications are possible for the second mode of operation. For instance, the second mode could be used to record motion images in a motion-still electronic camera. As the advantage of the second mode of operation relates to the production of more images per unit of time, the second mode could be used in an electronic still camera to optionally capture and record a burst of still images.

The sensor timing circuit 30 is controlled by the control interface 52 to provide the clock signals V1, V2, H1, H2, and the gate signal FDG according to the two modes of operation. The timing signals for the first mode are shown in Figure 5; those for the second mode are shown in Figure 6a and 6b. The two-phase cycling of signals V1 and V2 control the transfer of lines of image charge from the vertical registers 68 to the horizontal register 70. The two-phase cycling of signals H1 and H2 control the transfer of pixels from the horizontal register 70 to subsequent circuits in the camera. The level of the signal FDG determines whether the image charge is dumped to the fast dump drain or transferred to the horizontal register 70. When the sensor 20 is clocked using the first timing mode shown in Figure 5, all lines of the sensor are clocked out, one after the other, through the horizontal register 70, processed in subsequent camera circuitry, and stored in the removable memory 26. This timing mode provides a high quality progressive scan still image, but may take 1/30 second or longer to read out the still image. Such timing, however, is acceptable for still mode usage, and, as mentioned before, does not require unusually high speed components.

To provide an image to the color viewfinder display 10, a lower resolution image is suitable, but the update rate must be sufficient to provide good motion and eliminate display flicker. An update rate of 60 fields/sec is appropriate. Moreover, the sensor 20 includes the aforementioned array of color filters arranged in a particular color pattern (e.g., the checkerboard Bayer pattern of Fig. 3), and the lines of image charge that are transferred to the horizontal register 70 should preserve that particular color pattern in the pattern of lines that are generated for interlaced readout. To provide this kind of image, the sensor is read out in the second mode as shown in Figure 4, using the timing shown in Figures 6A and 6B. During field one, as shown in Figure 6A, the first two lines (1 and 2) are read out as in the normal mode. These provide a green-red and a blue-green line. The next two lines (3 and 4) are eliminated by turning on the fast dump structure 72 during the time that these lines are transferred past the fast dump structure 72. Next, lines 5 and 6 are read out normally, and then lines 7 and 8 are eliminated. This process proceeds for the 1/60 field time, dur-

ing which 120 pairs of lines are read out, and 120 pairs of lines are eliminated.

During field two, as shown in Figure 6B, the first two lines (1 and 2) are eliminated by turning on the fast dump structure 72 during the time that these lines are transferred past the fast dump structure 72. The next two lines (3 and 4) are read out as in the normal mode. These provide a green-red and a blue-green line. Next, lines 5 and 6 are eliminated, and lines 7 and 8 are read out normally. This process proceeds for the 1/60 field time, during which the 120 pairs of lines eliminated during field 1 are read out, and the 120 pairs of lines read out during field 1 are eliminated. This mode is called "pseudo-interlace", since the center-to-center spacing between two adjacent lines of the same field is not equal to two lines, as with normal interlace scanning, but alternates between 1 line and 3 lines.

The "pseudo-interlace" readout causes some minor vertical sampling artifacts, but these are not noticeable in most small LCDs or CRT displays. The pixels output for the sensor 20 in pseudo-interlace mode continue to have the Bayer-type color filter repeating pattern, so that they can be processed using the algorithms designed for the Bayer pattern. Moreover, the second field may be simply a repeat of the first field pattern shown in Figure 1; this is particularly appropriate if the color viewfinder display consists of a single-field non-interlaced arrangement of display pixels (e.g., 240 lines of display pixels in a typical liquid crystal display).

In a second embodiment, the video motion mode vertical subsampling features a center-to-center spacing between two adjacent readout lines of a given field which is always the same for both fields, because an even number of rows of charge are eliminated after each line is read out. Because an even number of lines are skipped, the line readout of the Bayer checkerboard provides the desired green-red, blue-green, green-red, blue-green sequence. An example is shown in Figure 7, where two rows are eliminated after each line is read out. For example, line 1, a green-red line is read out, and then lines 2 and 3 are eliminated via the fast dump structure 72. Next, line 4, a blue-green line is read out, and then lines 5 and 6 are eliminated. The timing diagram is shown in Figure 8. In this example, in order to provide an image with 240 lines per field, the sensor should contain 720 line per frame. Each field is obtained simply by repeating the pattern shown in Figure 7. Alternatively, alternate fields can be offset by alternating the sequence of line dumping, i.e., field one would dump lines 2 and 3, 5 and 6, etc., while field two would dump lines 1 and 2, 4 and 5, etc. To maintain the same image aspect ratio, either the pixel size or the number of pixels per line must be changed.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention. For instance, Figure 2B shows a progressive scan sensor with two readout registers 76 and 78 (which corresponds to the Performance Specification document for the KAI-0310CM image sensor; the preferred embodiment of Figure 2A simply uses but one register). The purpose is to double the system speed by having two complete processing channels (analog processing, A/D, etc.); the fast dump structure 72 of such a sensor would be operated as described in connection with foregoing figures to eliminate two or more consecutive lines of charge so as to preserve the color filter array pattern in the interlaced readout. Furthermore, although the Bayer pattern was described, other mosaic-type filter patterns could be used to advantage, for example, complementary patterns involving cyan, magenta, and yellow filters.

The invention is summarized as follows:

1. An electronic camera, comprising:

an image sensor comprising a two-dimensional array of photosites arranged in rows and columns, a plurality of vertical registers adjacent photosite columns for transferring rows of image charge from the photosites to a horizontal register for readout, and a charge drain structure interposed between the output of the vertical registers and the horizontal register for eliminating complete rows of image charge at a time from the image sensor; and

a timing and control section for controlling the charge drain structure so as to eliminate two or more consecutive lines of image charge from the image sensor for every one or more lines of image charge that are transferred to the horizontal register for readout, thereby generating a pattern of lines suitable for interlaced readout.

2. An electronic camera as in 1 wherein said timing and control section provides an interlaced video signal by alternating between two patterns of lines each obtained by eliminating two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register.

3. An electronic camera as in 2 wherein said camera further includes an electronic viewfinder, and wherein said interlaced video signal is provided to the electronic viewfinder.

4. An electronic camera as in 2 wherein said camera further provides for recording of motion images, and wherein said interlaced video signal is provided for motion recording.

5. An electronic camera as in 1 wherein the image sensor is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines of image charge that are transferred to the horizontal register are transferred as fields that preserve the particular color pattern in the pattern of lines that are generated for interlaced readout in each field.

6. An electronic camera as in 5 wherein the array of color filters are arranged in the following mosaic pattern of red, green, and blue filters

R G R G
G B G B
R G R G
G B G B

and wherein the lines of image charge that are transferred to the horizontal register for interlaced readout preserve the same mosaic pattern in each field.

7. An electronic camera, comprising:

a progressive scan image sensor capable of producing an entire image in a single scan in response to clocking signals, said image sensor comprising a two-dimensional array of photosites arranged in rows and columns, a plurality of vertical registers adjacent photosite columns for transferring rows of image charge from the photosites to a horizontal register for readout, and a charge drain structure interposed between the output of the vertical registers and the horizontal register for dumping complete rows of image charge at a time from the image sensor; and

a timing and control section for producing clocking signals to read out the entire array of photosites in a single scan, said timing and control section further enabling the charge drain structure to dump two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register for readout, thereby generating a pattern of lines suitable for interlaced readout.

8. An electronic camera as in 7 wherein said timing and control section provides an interlaced video signal that are transferred as fields, and wherein said camera is operable in two modes, including a first mode in which the entire array of photosites are read out in a single scan, and a second mode in which said two or more consecutive lines of image charges are dumped by the charge drain structure for every one or more lines of image charge transferred to the horizontal register to provide the interlaced video signal.

9. An electronic camera as in 8 further including an electronic viewfinder, and wherein said interlaced video signal is provided to the electronic viewfinder in the second mode of operation.

10. An electronic camera as in 8 wherein the image sensor is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines transferred to the horizontal register to provide the interlaced video signal comprise a pattern that replicates the particular color pattern of the array of color filters in each field.

11. An electronic camera as in 10 wherein the array of color filters are arranged in the following mosaic pattern of red, green, and blue filters

R G R G
G B G B
R G R G
G B G B

and wherein the lines of image charge that are transferred to the horizontal register for interlaced readout preserve the same mosaic pattern in each field.

12. An electronic camera as in 8 wherein the image sensor is a color sensor having an array of color filters that provides image charge corresponding to several different colors, and the plurality of lines transferred to the horizontal register to provide each field includes all of the several different colors.

13. An electronic camera, comprising:

a progressive scan sensor having an area image sensing section composed of a plurality of lines and a horizontal readout register for outputting lines of image charge from the image sensing section, both the area image sensing section and the horizontal readout register being arranged on a substrate, said progressive scan sensor also including a fast dump structure arranged between the image sensing section and the readout register for dumping lines of image charge to a drain; and

a timing and control unit for operating the camera in two modes, including a first mode wherein lines of signal charge corresponding to each line in the image sensing section are progressively read out through the horizontal register and a second mode wherein some of the lines of signal charge corresponding to adjacent lines in the image sensing section are eliminated through the fast dump structure prior to readout.

14. An electronic camera as in 13 wherein said timing and control unit provides an interlaced video signal by alternating between two patterns of lines each obtained by eliminating two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register.

15. An electronic camera as in 14 wherein said camera further includes an electronic viewfinder, and wherein said interlaced video signal is provided to the electronic viewfinder.

16. An electronic camera as in 13 wherein the image sensor is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines of image charge that are transferred to the horizontal register are transferred as fields that preserve the particular color pattern in the pattern of lines that are generated for interlaced readout in each field.

17. An electronic camera operable in an image capture mode and in a viewing mode, said camera comprising:

a progressive scan sensor capable of producing an entire color image in a single scan in response to clocking signals, said image sensor having a two-dimensional array of photosites arranged in rows and columns, a plurality of vertical registers adjacent the photosite columns for transferring rows of image charge from the photosites to a horizontal register for reading out a color image signal from the image sensor, a fast dump structure interposed between

the outputs of the vertical registers and the horizontal register for draining complete rows of image charge at a time from the image sensor, and a color filter array arranged in a particular mosaic pattern over the photosites;

a timing control unit for operating the progressive scan image sensor in the two modes, wherein said timing and control unit produces clocking signals in the image capture mode to read out the entire array of photosites in a single scan according to the particular mosaic pattern and in the viewing mode to further enable the fast dump structure to drain some lines of image charge from the sensor while transferring a sequence of lines to the horizontal register for readout that preserves the particular mosaic pattern, thereby generating a pattern of lines suitable for interlaced color readout.

18. An electronic camera as in 17 wherein said timing and control unit provides an interlaced video signal by alternating between two patterns of lines each obtained by eliminating two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register.

19. An electronic camera as in 18 wherein said camera further includes an electronic color viewfinder, and wherein said interlaced video signal is provided to the electronic viewfinder.

20. A method for providing interlaced images from a progressive scan sensor in an electronic camera, the sensor including an array of photosites, an output register, and a charge drain structure interposed between the array of photosites and the output register, said method comprising the steps of:

transferring image charge line by line from sensor photosites toward the output register;

draining a regular sequence of lines from the sensor through the charge drain structure, said regular sequence including two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register; and

outputting the remaining lines from the output register in a pattern of lines suitable for interlaced readout.

21. A method as in 20 further comprising the step of applying the remaining lines from the output register to an electronic viewfinder display.

22. A method as in 20 wherein the sensor is a color sensor employing a mosaic pattern of color filters and wherein the outputting step transfers color fields that maintain the same mosaic pattern in the remaining lines as found on the sensor.

## Claims

1. An electronic camera, comprising:

an image sensor (20) comprising a two-dimensional array of photosites (66) arranged in rows and columns, a plurality of vertical registers (68) adjacent photosite columns for transferring rows of image charge from the photosites to a horizontal register (70) for readout, and a charge drain structure (72) interposed between the output of the vertical registers and the horizontal register for eliminating complete rows of image charge at a time from the image sensor; and

a timing and control section (27) for controlling the charge drain structure (72) so as to eliminate two or more consecutive lines of image charge from the image sensor for every one or more lines of image charge that are transferred to the horizontal register (70) for readout, thereby generating a pattern of lines suitable for interlaced readout.

2. An electronic camera as claimed in claim 1 wherein said timing and control section (27) provides an interlaced video signal by alternating between two patterns of lines each obtained by eliminating two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register (70).

3. An electronic camera as claimed in claim 2 wherein said camera further includes an electronic viewfinder (10), and wherein said interlaced video signal is provided to the electronic viewfinder.

4. An electronic camera as claimed in claim 2 wherein said camera further provides for recording of motion images, and wherein said interlaced video signal is provided for motion recording.

5. An electronic camera as claimed in claim 1 wherein the image sensor (20) is a color sensor having an array of color filters arranged in a particular color pattern and wherein the lines of image charge that are transferred to the horizontal register (70) are transferred as fields that preserve the particular color pattern in the pattern of lines that are generated for interlaced readout in each field.

6. An electronic camera as claimed in claim 5 wherein the array of color filters are arranged in the following mosaic pattern of red, green, and blue filters

R G R G
G B G B
R G R G
G B G B

and wherein the lines of image charge that are transferred to the horizontal register (70) for interlaced readout preserve the same mosaic pattern in each field.

7. An electronic camera, comprising:

a progressive scan image sensor (20) capable of producing an entire image in a single scan in response to clocking signals, said image sensor

comprising a two-dimensional array of photosites (66) arranged in rows and columns, a plurality of vertical registers (68) adjacent photosite columns for transferring rows of image charge from the photosites to a horizontal register (70) for readout, and a charge drain structure (72) interposed between the output of the vertical registers and the horizontal register for dumping complete rows of image charge at a time from the image sensor; and

a timing and control section (27) for producing clocking signals to read out the entire array of photosites in a single scan, said timing and control section further enabling the charge drain structure (72) to dump two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register (70) for readout, thereby generating a pattern of lines suitable for interlaced readout.

**8.** A method for providing interlaced images from a progressive scan sensor in an electronic camera, the sensor (20) including an array of photosites (66), an output register (70), and a charge drain structure (72) interposed between the array of photosites and the output register, said method comprising the steps of:

transferring image charge line by line from sensor photosites (66) toward the output register (70);

draining a regular sequence of lines from the sensor through the charge drain structure (72), said regular sequence including two or more consecutive lines of image charge for every one or more lines of image charge that are transferred to the horizontal register (70); and

outputting the remaining lines from the output register (70) in a pattern of lines suitable for interlaced readout.

**9.** A method as claimed in claim 8 further comprising the step of applying the remaining lines from the output register (70) to an electronic viewfinder display (10).

**10.** A method as claimed in claim 8 wherein the sensor (20) is a color sensor employing a mosaic pattern of color filters and wherein the outputting step transfers color fields that maintain the same mosaic pattern in the remaining lines as found on the sensor.

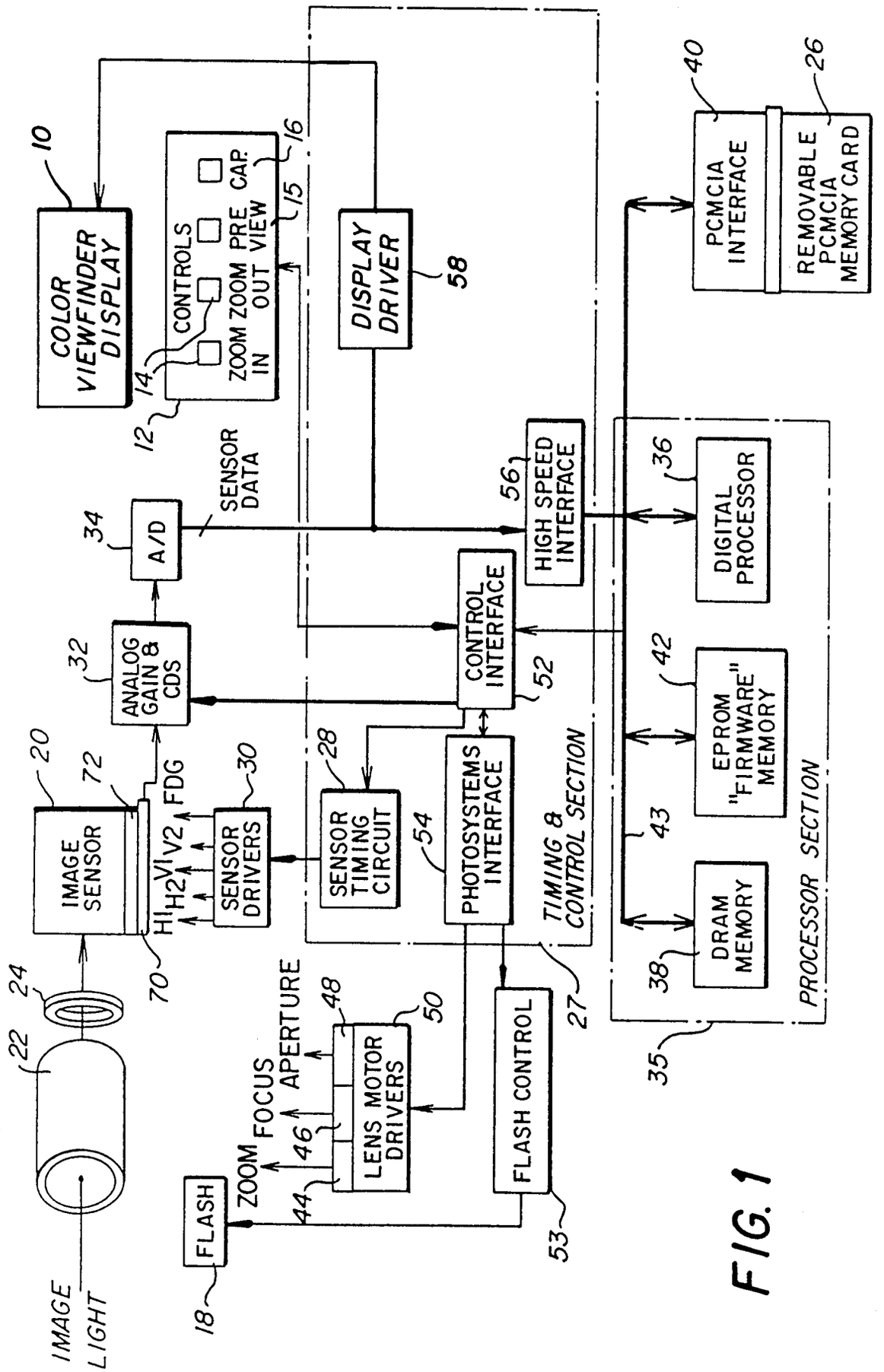



FIG. 1

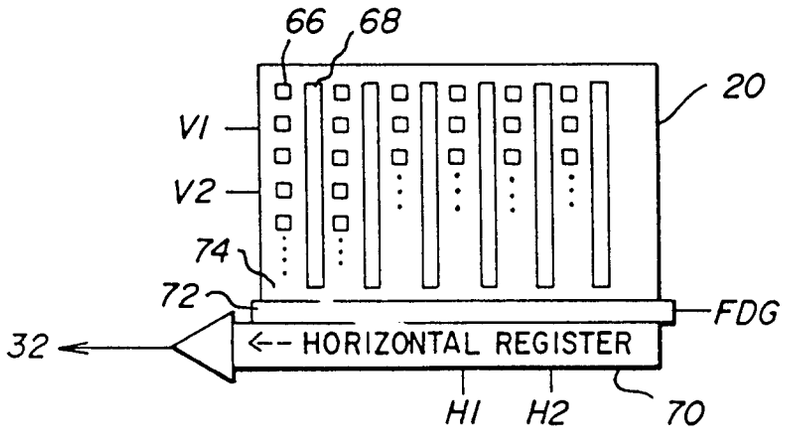



FIG. 2A

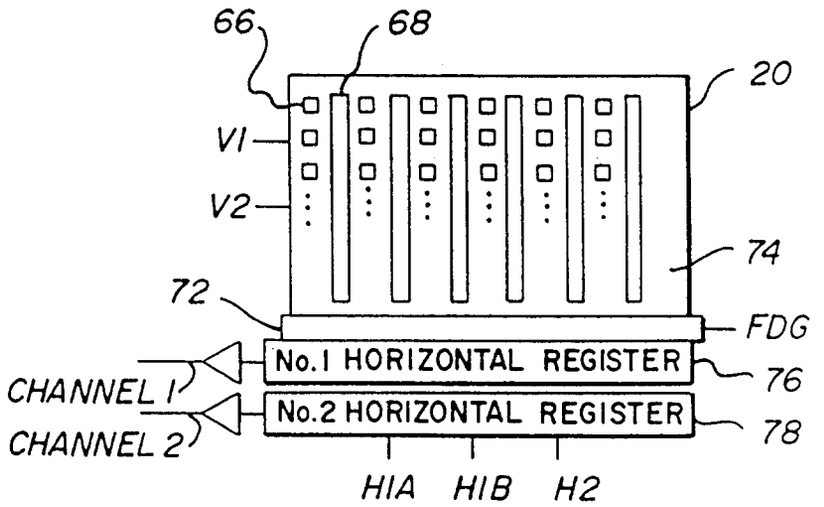


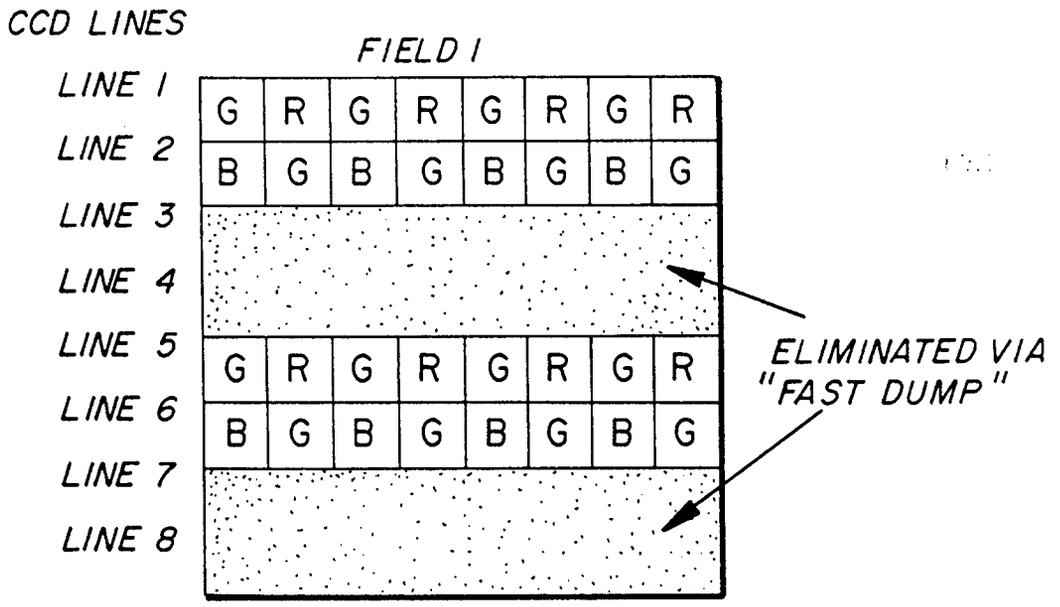

FIG. 2B

CCD LINES

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LINE 1 | G | R | G | R | G | R | G | R |
| LINE 2 | B | G | B | G | B | G | B | G |
| LINE 3 | G | R | G | R | G | R | G | R |
| LINE 4 | B | G | B | G | B | G | B | G |
| LINE 5 | G | R | G | R | G | R | G | R |
| LINE 6 | B | G | B | G | B | G | B | G |
| LINE 7 | G | R | G | R | G | R | G | R |
| LINE 8 | B | G | B | G | B | G | B | G |

FIG. 3

FIG. 4A



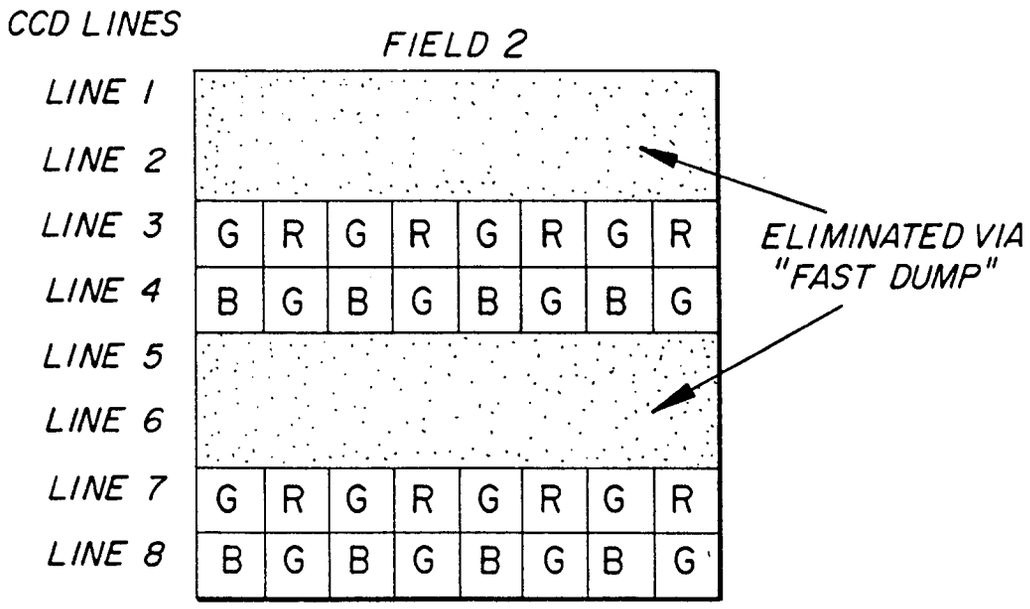




FIG. 4B

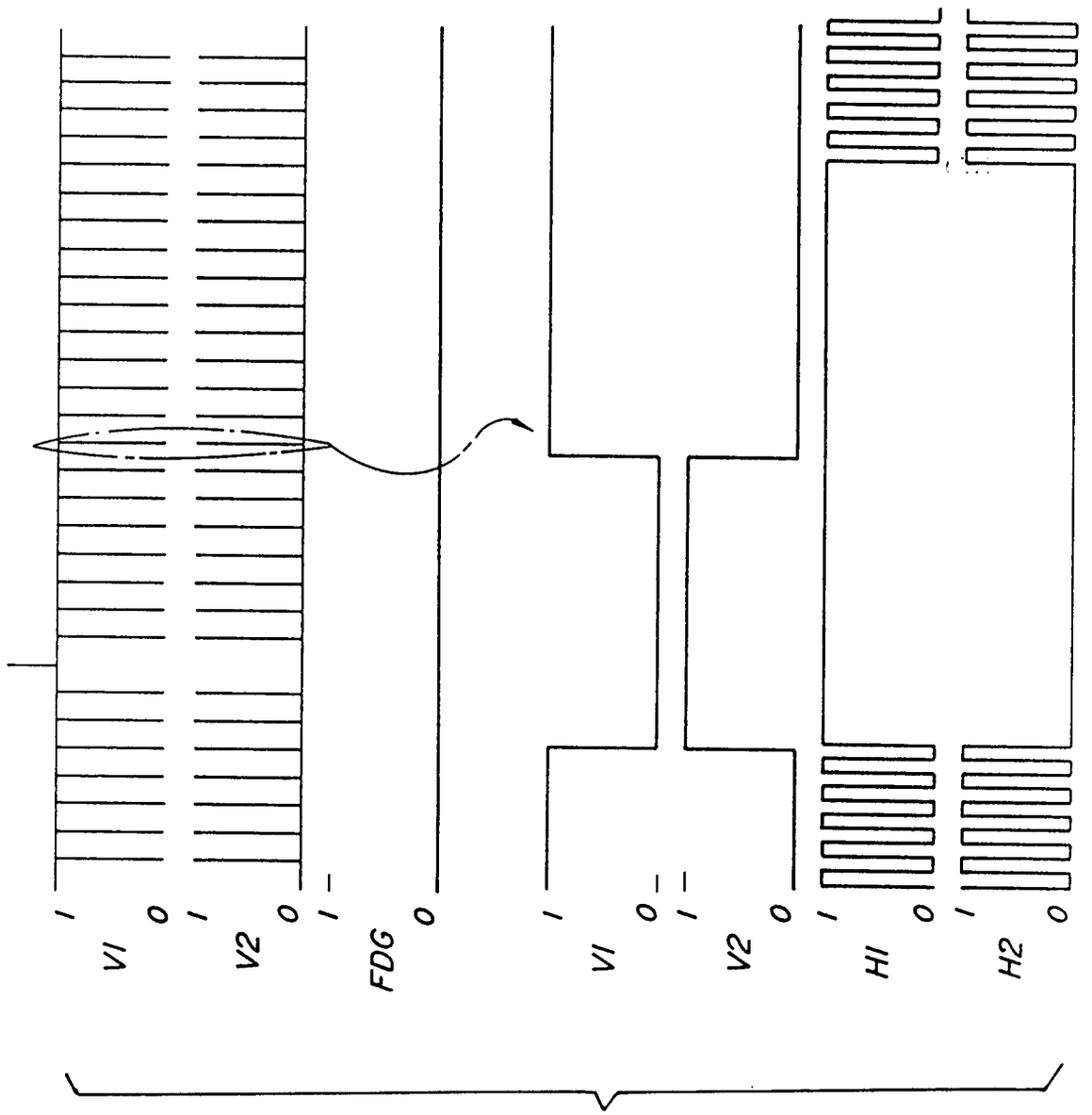



FIG.5

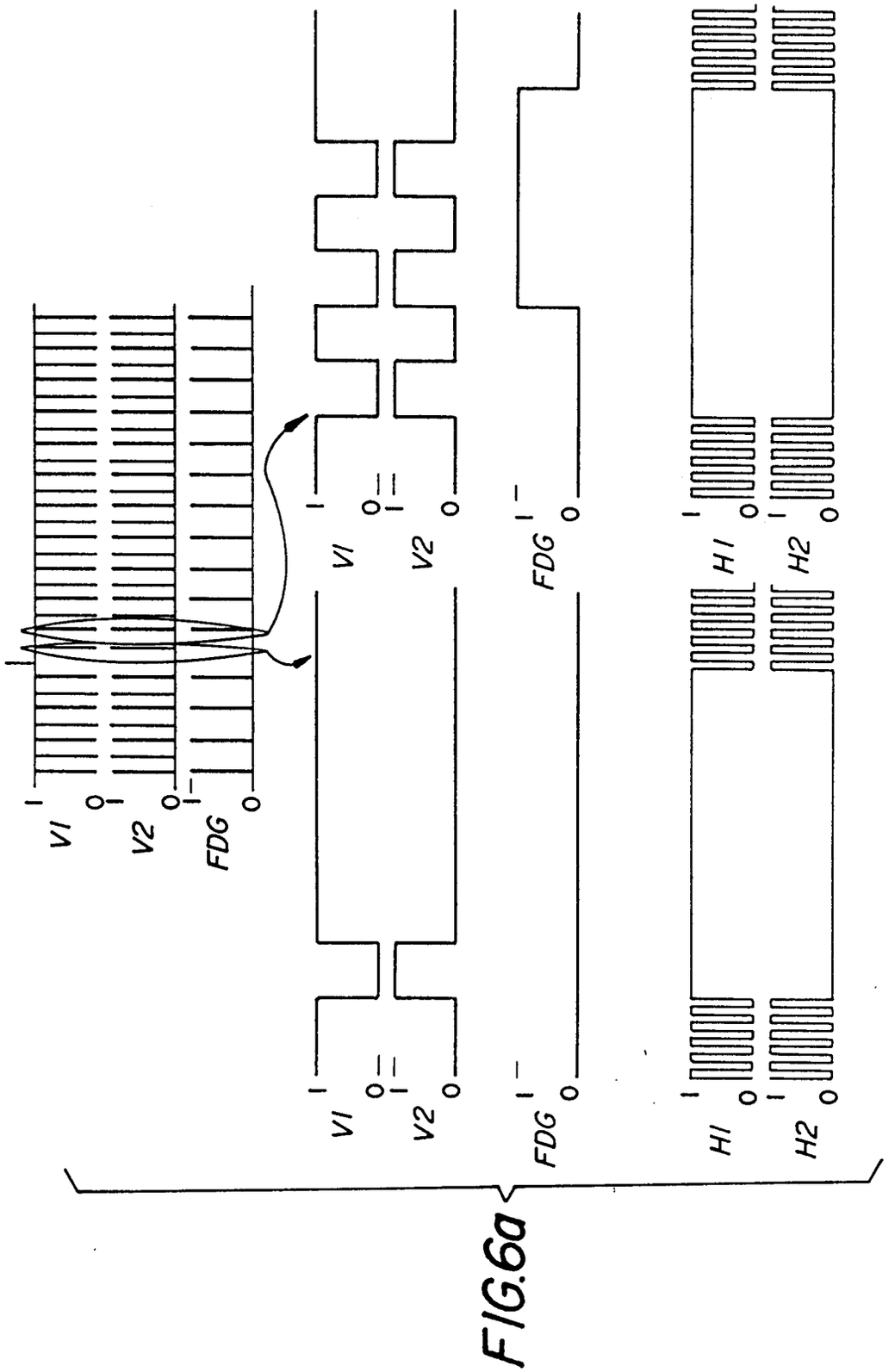



FIG.6a

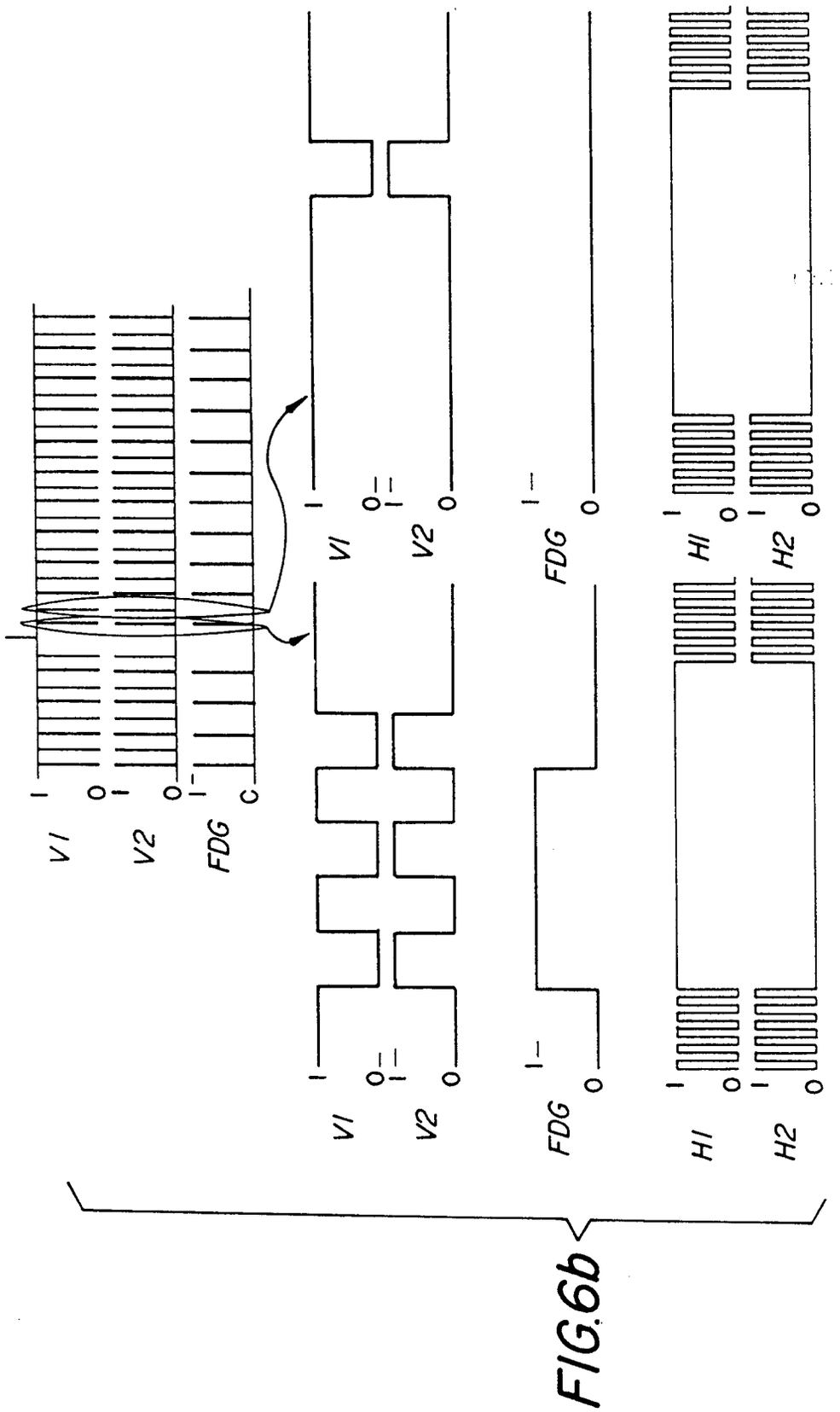
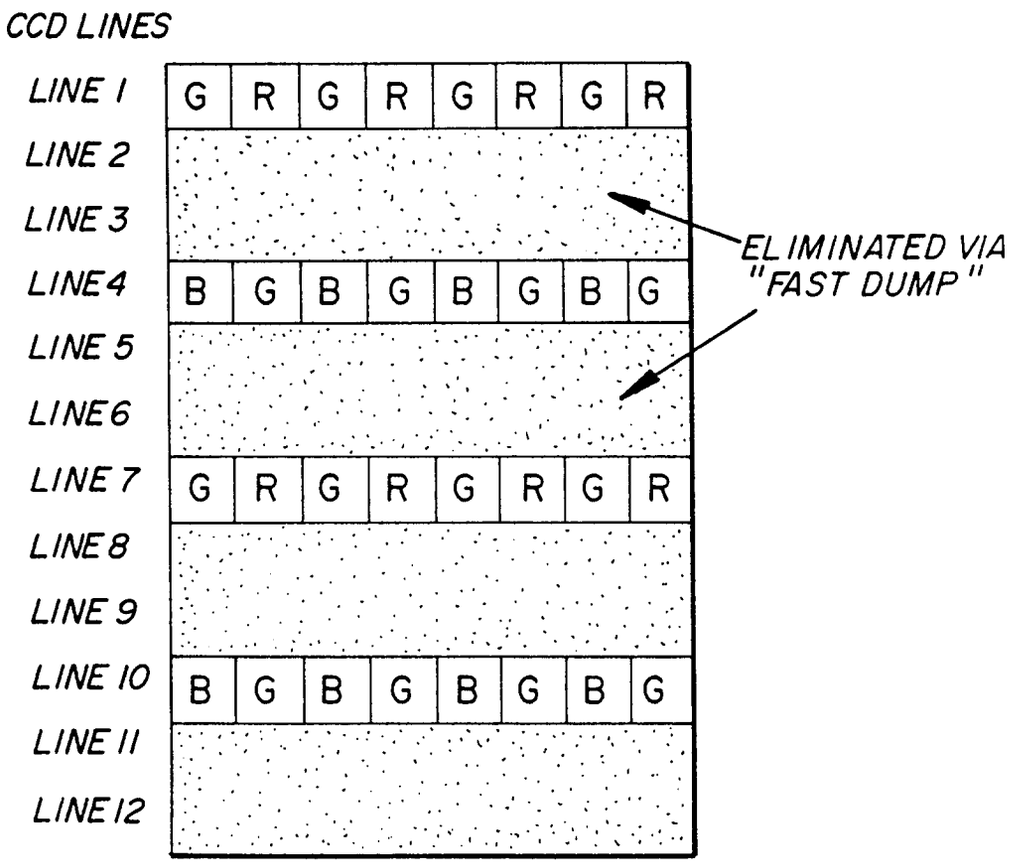



FIG.6b

FIG. 7



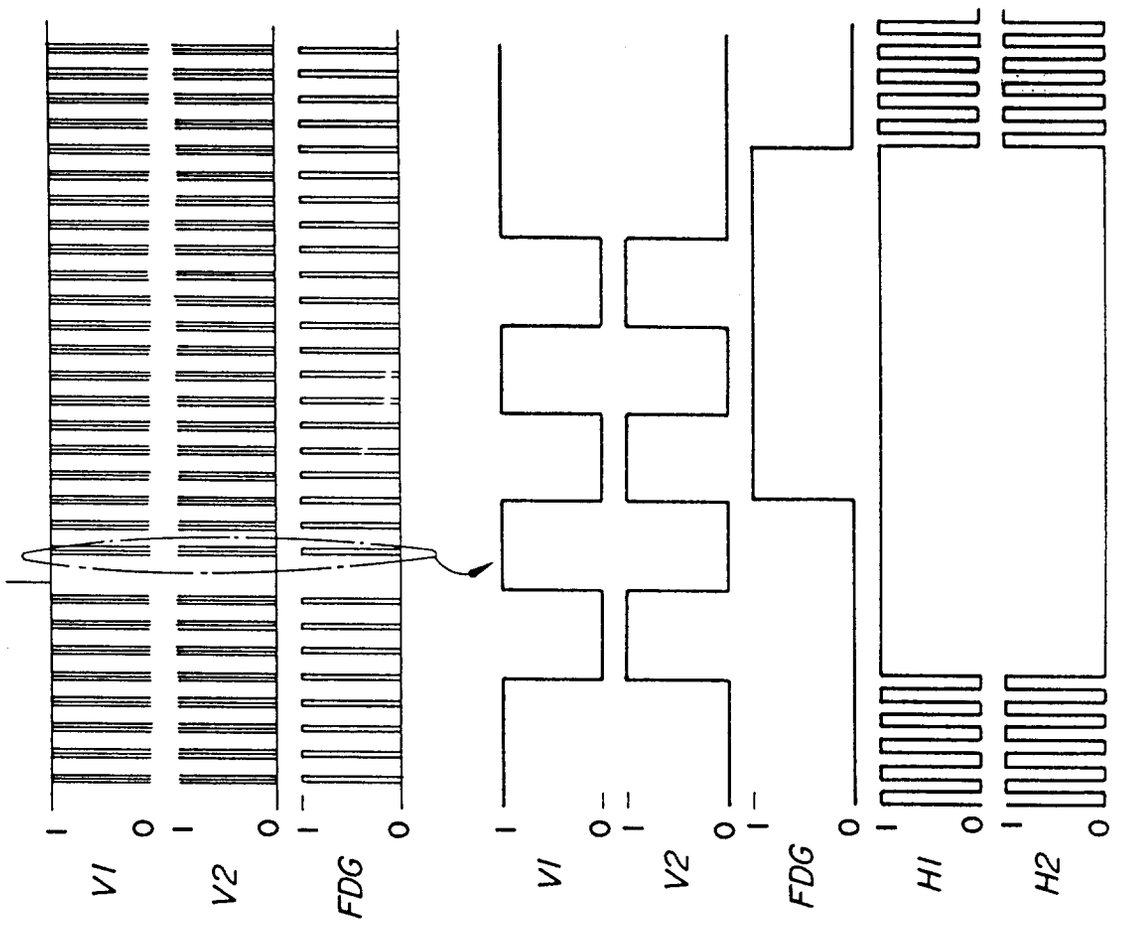



FIG.8

US006661451B1

(12) **United States Patent**
**Kijima et al.**

(10) **Patent No.: US 6,661,451 B1**
(45) **Date of Patent: *Dec. 9, 2003**

(54) **IMAGE PICKUP APPARATUS CAPABLE OF PERFORMING BOTH A STILL IMAGE PROCESS AND A DYNAMIC IMAGE PROCESS**

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(73) Assignee: **Olympus Optical Co., Ltd.**, Tokyo (JP)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **08/961,408**

(22) Filed: **Oct. 30, 1997**

(30) **Foreign Application Priority Data**

Nov. 1, 1996 (JP) ..... 8-291752

(51) **Int. Cl.**[7] ..... **H04N 5/225**; H04N 5/335

(52) **U.S. Cl.** ..... **348/220.1**; 348/322; 348/294

(58) **Field of Search** ..... 348/220, 222, 348/207, 229, 272, 273, 279, 294, 311, 312, 315, 317, 319, 322, 324, 362, 333.09, 333.11, 446, 441, 220.1, 222.1, 207.99, 229.1; 358/906, 909.1

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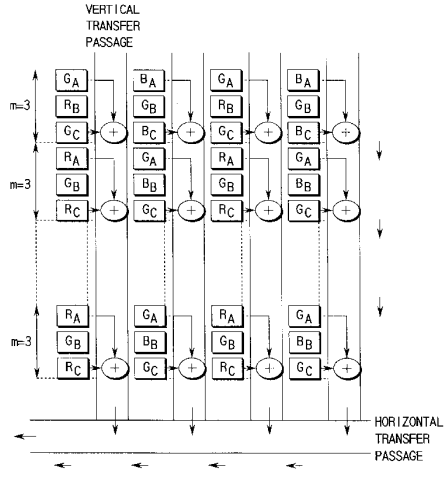
*Primary Examiner*—Aung S. Moe
(74) *Attorney, Agent, or Firm*—Frishauf, Holtz, Goodman & Chick, P.C.

(57) **ABSTRACT**

An imaging apparatus includes an interline type CCD image sensor having 1,000,000 or more pixels, which has a Bayer configuration color filter suitable for reading all pixel signals in a line-sequential scanning manner. The imaging apparatus drives the CCD image sensor in a high speed mode usually, and in a high quality image mode only for a trigger depression. In the high speed mode, the CCD image sensor outputs pixel signals for one line at intervals of three lines in the vertical direction. During the high speed mode operation of the CCD image sensor, images are displayed on a liquid crystal display portion at a frame rate of 60 frames/second, the images being recognized by the human eyes as a dynamic image, i.e., a motion picture.

**7 Claims, 13 Drawing Sheets**



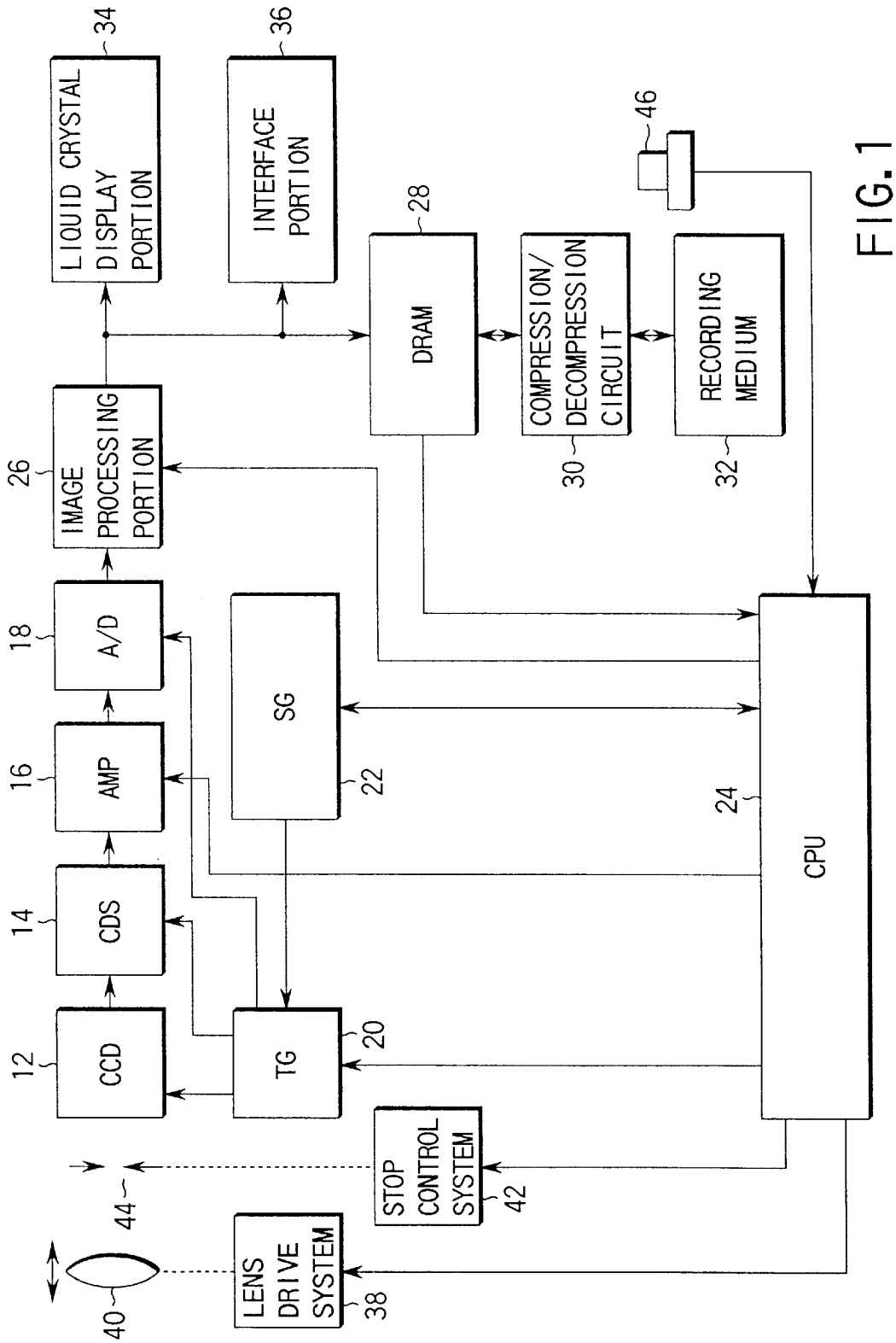

LIQUID CRYSTAL DISPLAY PORTION
34
INTERFACE PORTION
36
46
DRAM
28
COMPRESSION/ DECOMPRESSION CIRCUIT
30
RECORDING MEDIUM
32
IMAGE PROCESSING PORTION
26
A/D
18
AMP
16
CDS
14
CCD
12
SG
22
TG
20
CPU
24
STOP CONTROL SYSTEM
42
44
LENS DRIVE SYSTEM
38
40

FIG. 1

FIG. 2

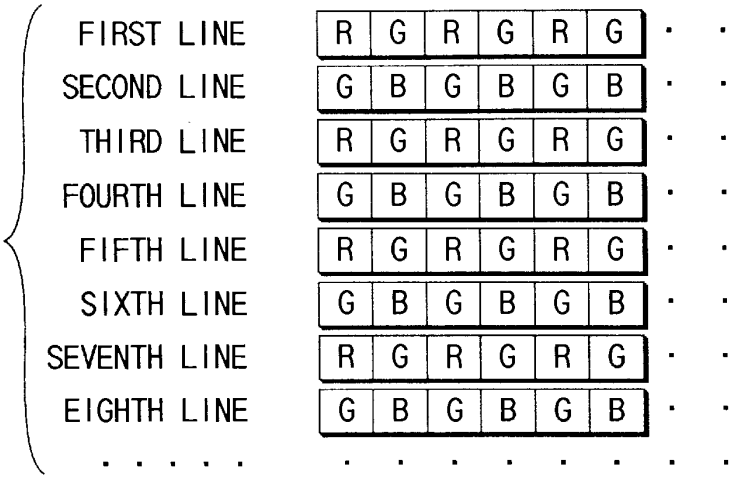
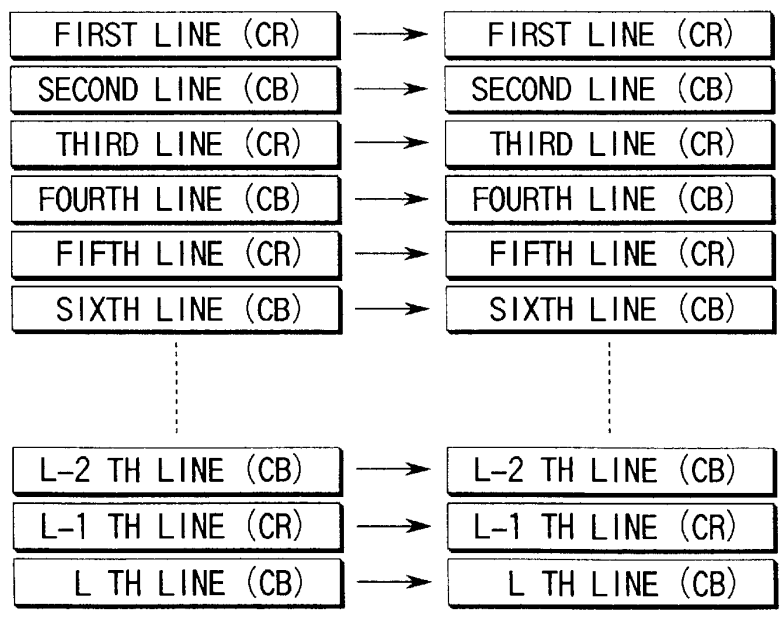

FIRST LINE
SECOND LINE
THIRD LINE
FOURTH LINE
FIFTH LINE
SIXTH LINE
SEVENTH LINE
EIGHTH LINE
R G R G R G
G B G B G B
R G R G R G
G B G B G B
R G R G R G
G B G B G B
R G R G R G
G B G B G B

FIG. 3


FIRST LINE (CR)
SECOND LINE (CB)
THIRD LINE (CR)
FOURTH LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
L-2 TH LINE (CB)
L-1 TH LINE (CR)
L TH LINE (CB)
FIRST LINE (CR)
SECOND LINE (CB)
THIRD LINE (CR)
FOURTH LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
L-2 TH LINE (CB)
L-1 TH LINE (CR)
L TH LINE (CB)

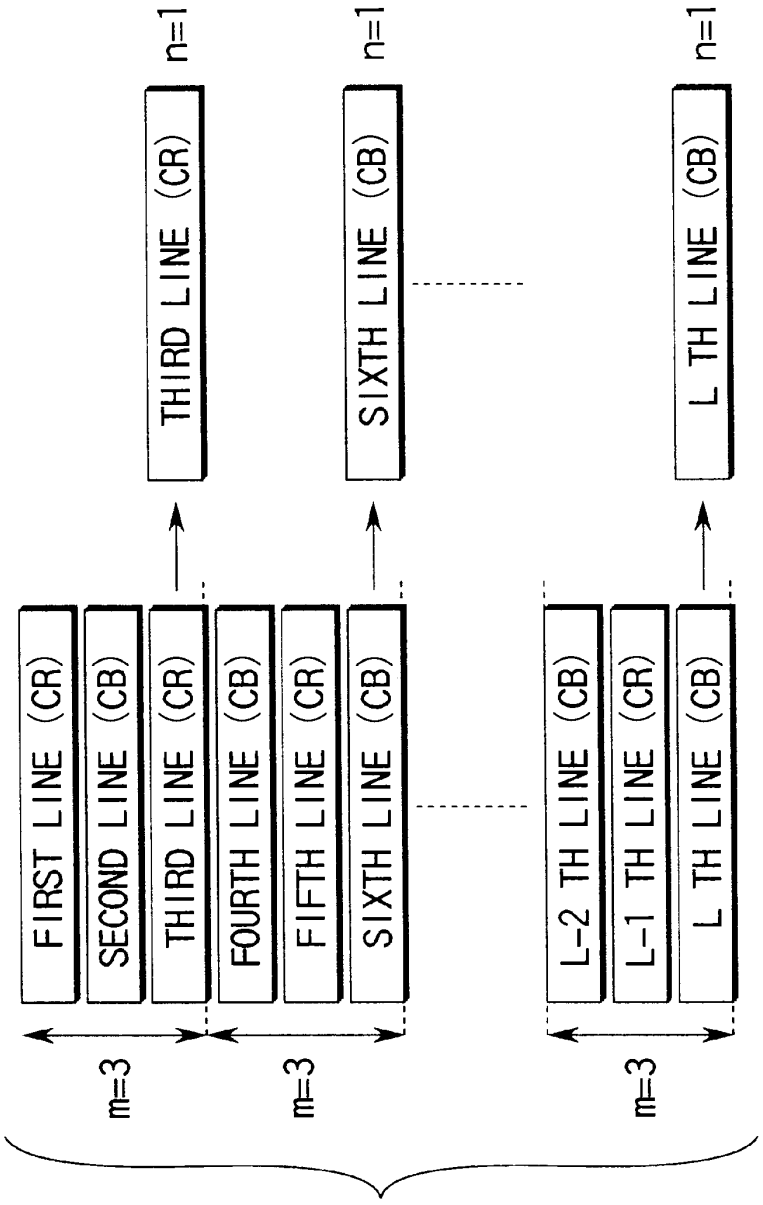

n=1
n=1
n=1
THIRD LINE (CR)
SIXTH LINE (CB)
L TH LINE (CB)
FIRST LINE (CR)
SECOND LINE (CB)
THIRD LINE (CR)
FOURTH LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
L-2 TH LINE (CB)
L-1 TH LINE (CR)
L TH LINE (CB)
m=3
m=3
m=3

FIG. 4

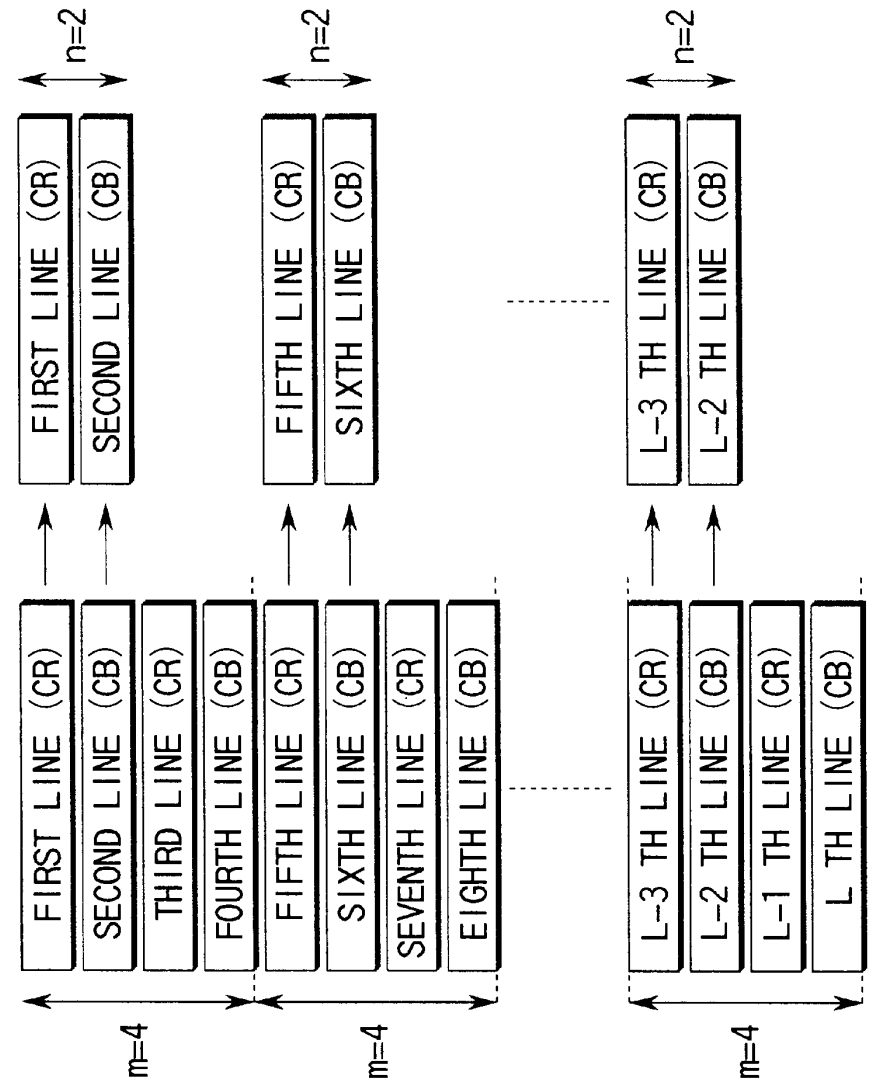

n=2
n=2
n=2
FIRST LINE (CR)
SECOND LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
L-3 TH LINE (CR)
L-2 TH LINE (CB)
FIRST LINE (CR)
SECOND LINE (CB)
THIRD LINE (CR)
FOURTH LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
SEVENTH LINE (CR)
EIGHTH LINE (CB)
L-3 TH LINE (CR)
L-2 TH LINE (CB)
L-1 TH LINE (CR)
L TH LINE (CB)
m=4
m=4
m=4

FIG. 5

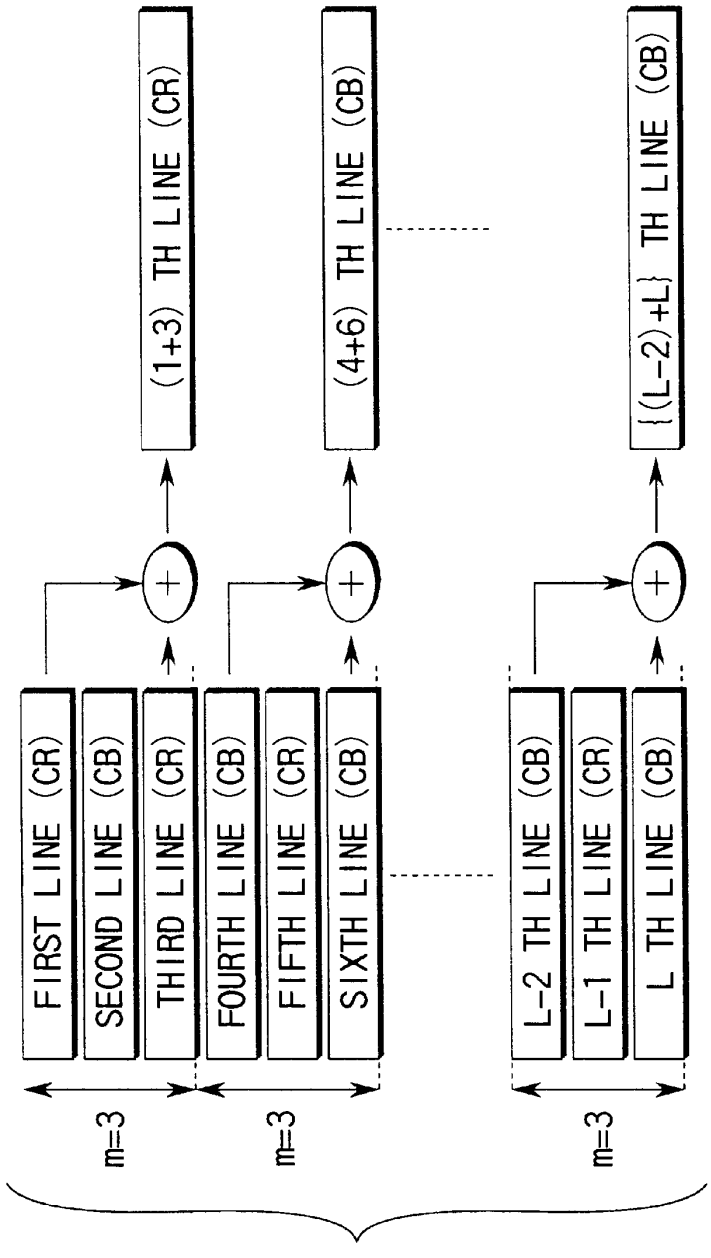

FIRST LINE (CR)
SECOND LINE (CB)
THIRD LINE (CR)
FOURTH LINE (CB)
FIFTH LINE (CR)
SIXTH LINE (CB)
L-2 TH LINE (CB)
L-1 TH LINE (CR)
L TH LINE (CB)
(1+3) TH LINE (CR)
(4+6) TH LINE (CB)
{(L-2)+L} TH LINE (CB)
m=3
m=3
m=3

FIG. 6

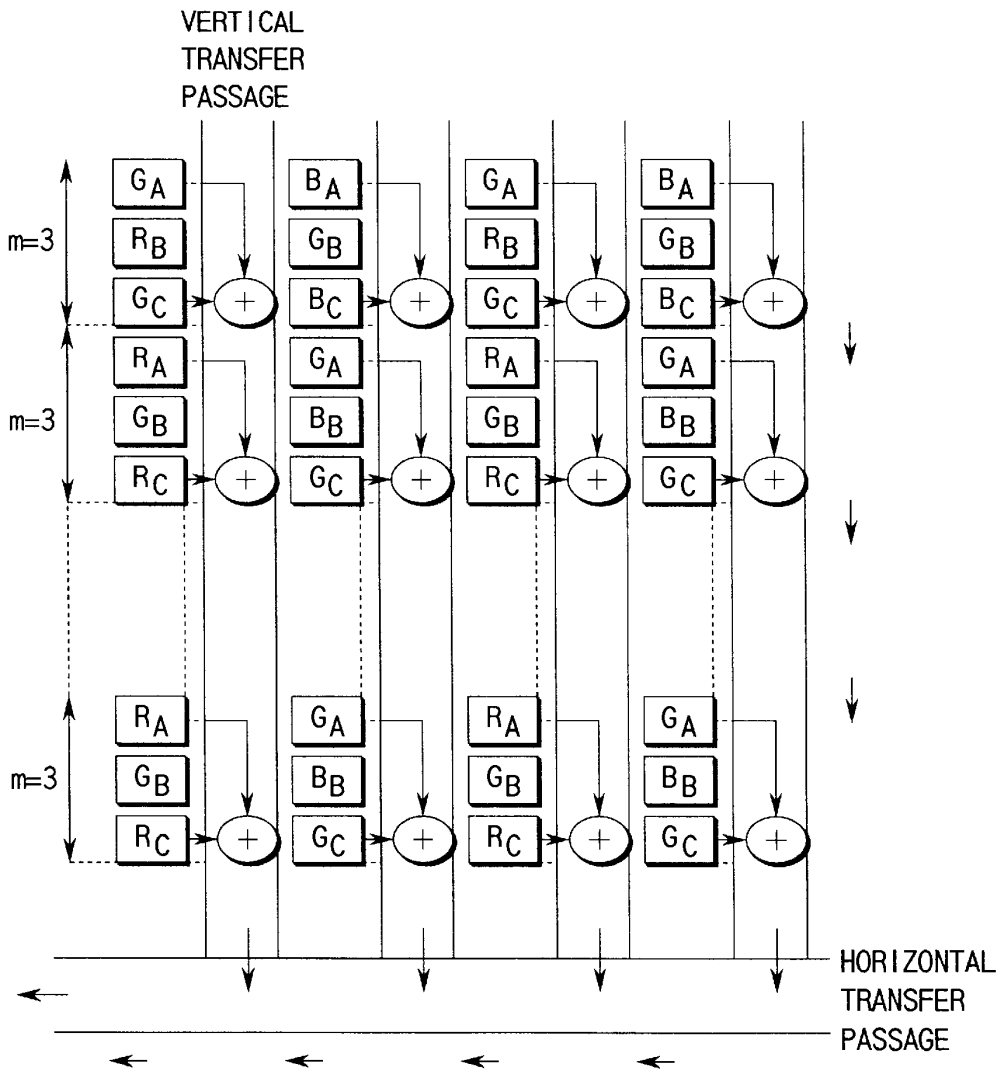

VERTICAL
TRANSFER
PASSAGE
m=3
m=3
m=3
HORIZONTAL
TRANSFER
PASSAGE

FIG. 7

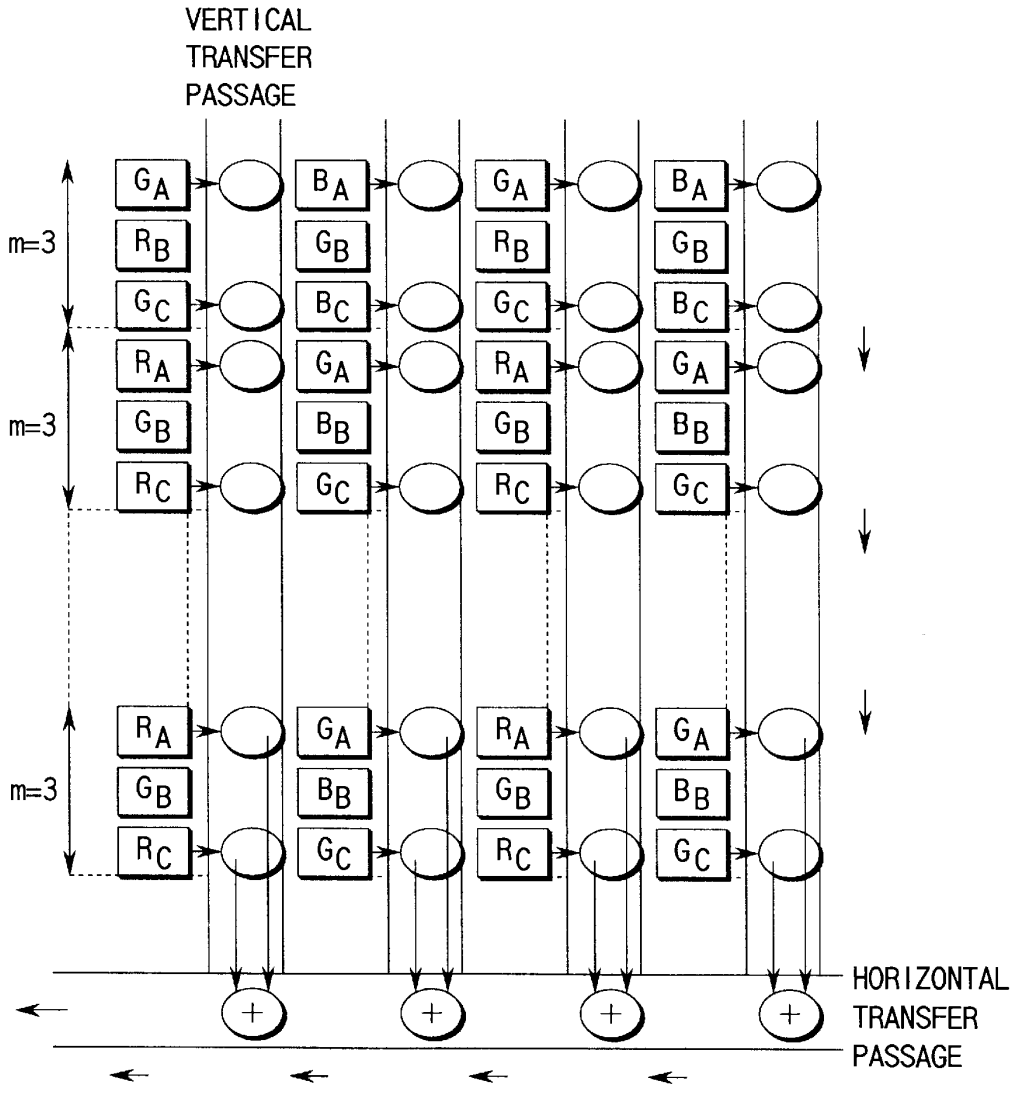

VERTICAL
TRANSFER
PASSAGE
m=3
m=3
m=3
HORIZONTAL
TRANSFER
PASSAGE

FIG. 8

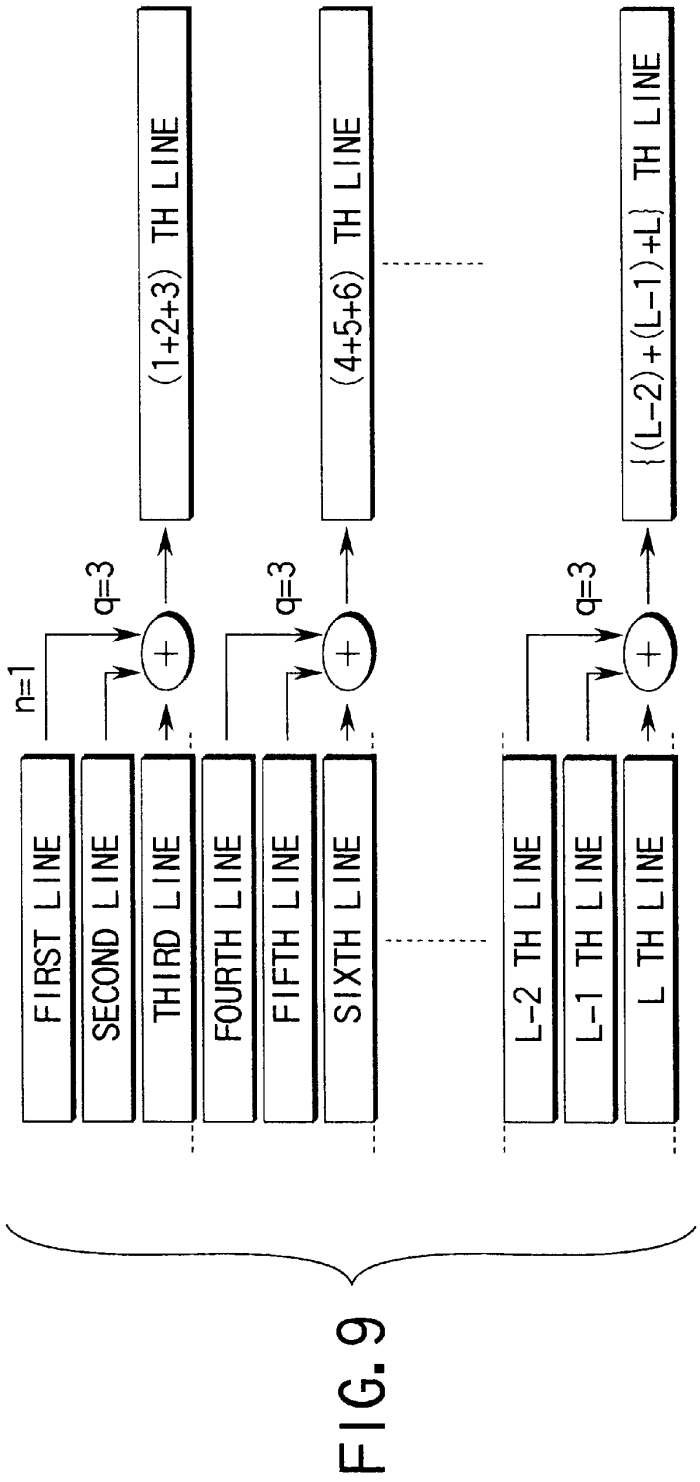

FIRST LINE
SECOND LINE
THIRD LINE
FOURTH LINE
FIFTH LINE
SIXTH LINE
L-2 TH LINE
L-1 TH LINE
L TH LINE
n=1
q=3
q=3
q=3
(1+2+3) TH LINE
(4+5+6) TH LINE
{(L-2)+(L-1)+L} TH LINE

FIG. 9

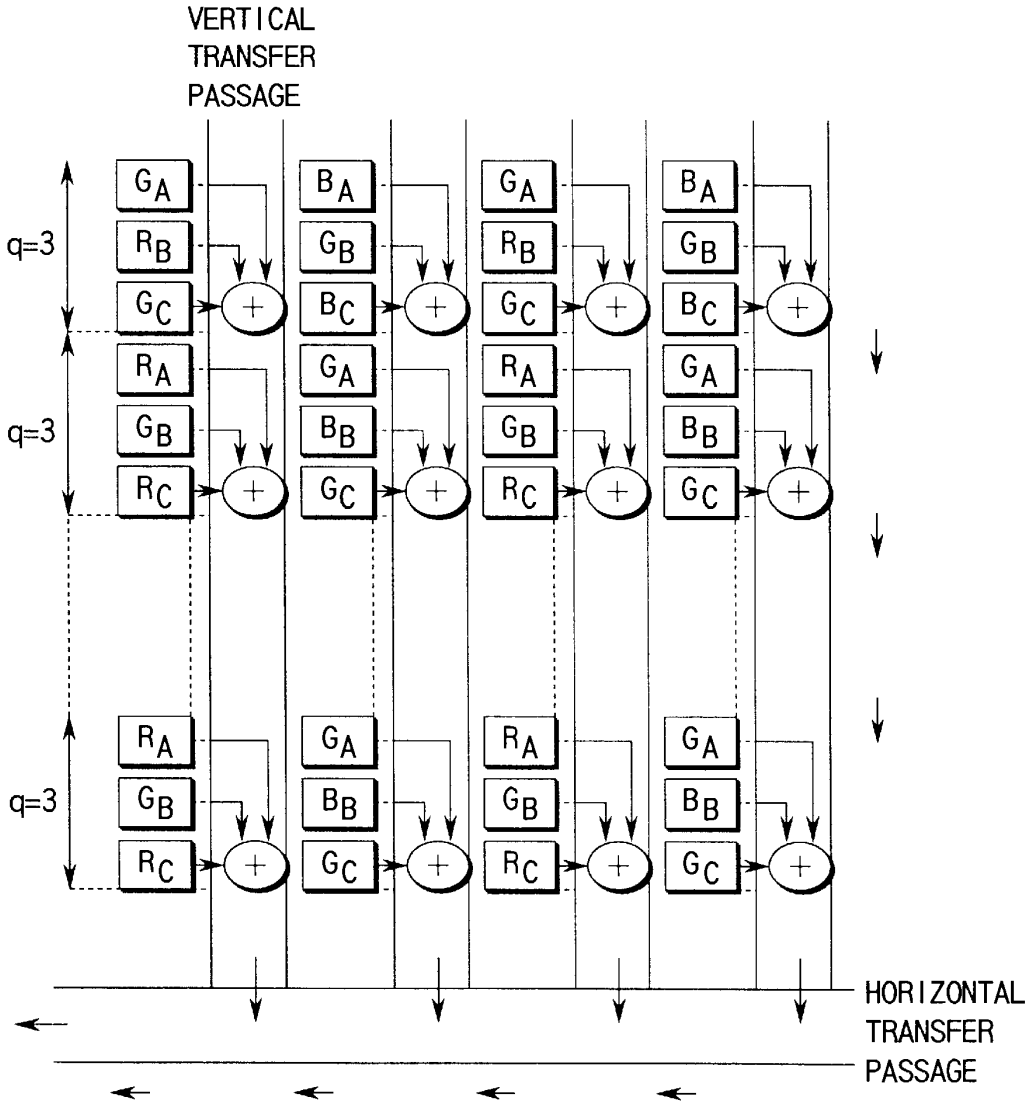

VERTICAL
TRANSFER
PASSAGE
q=3
q=3
q=3
HORIZONTAL
TRANSFER
PASSAGE

FIG. 10

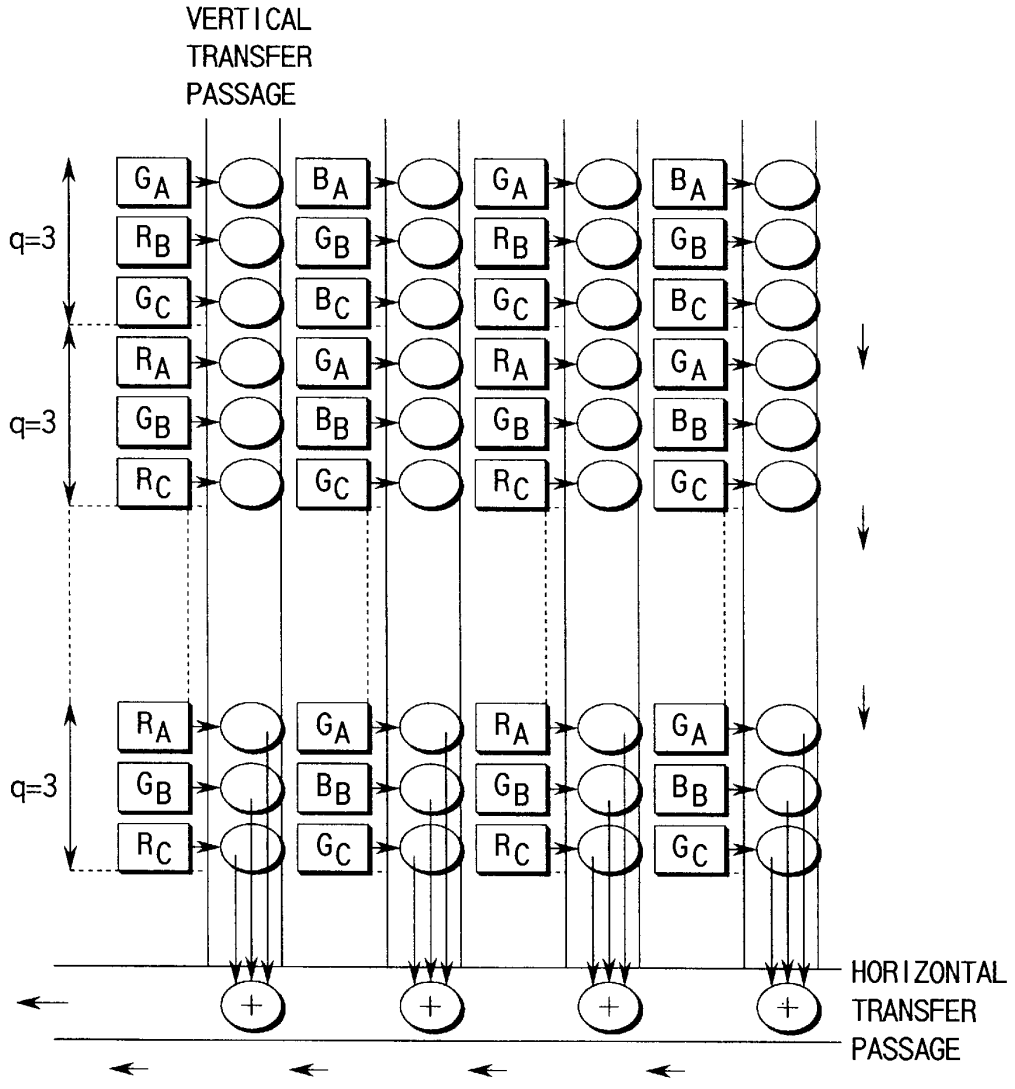

VERTICAL
TRANSFER
PASSAGE
q=3
q=3
q=3
HORIZONTAL
TRANSFER
PASSAGE

FIG. 11

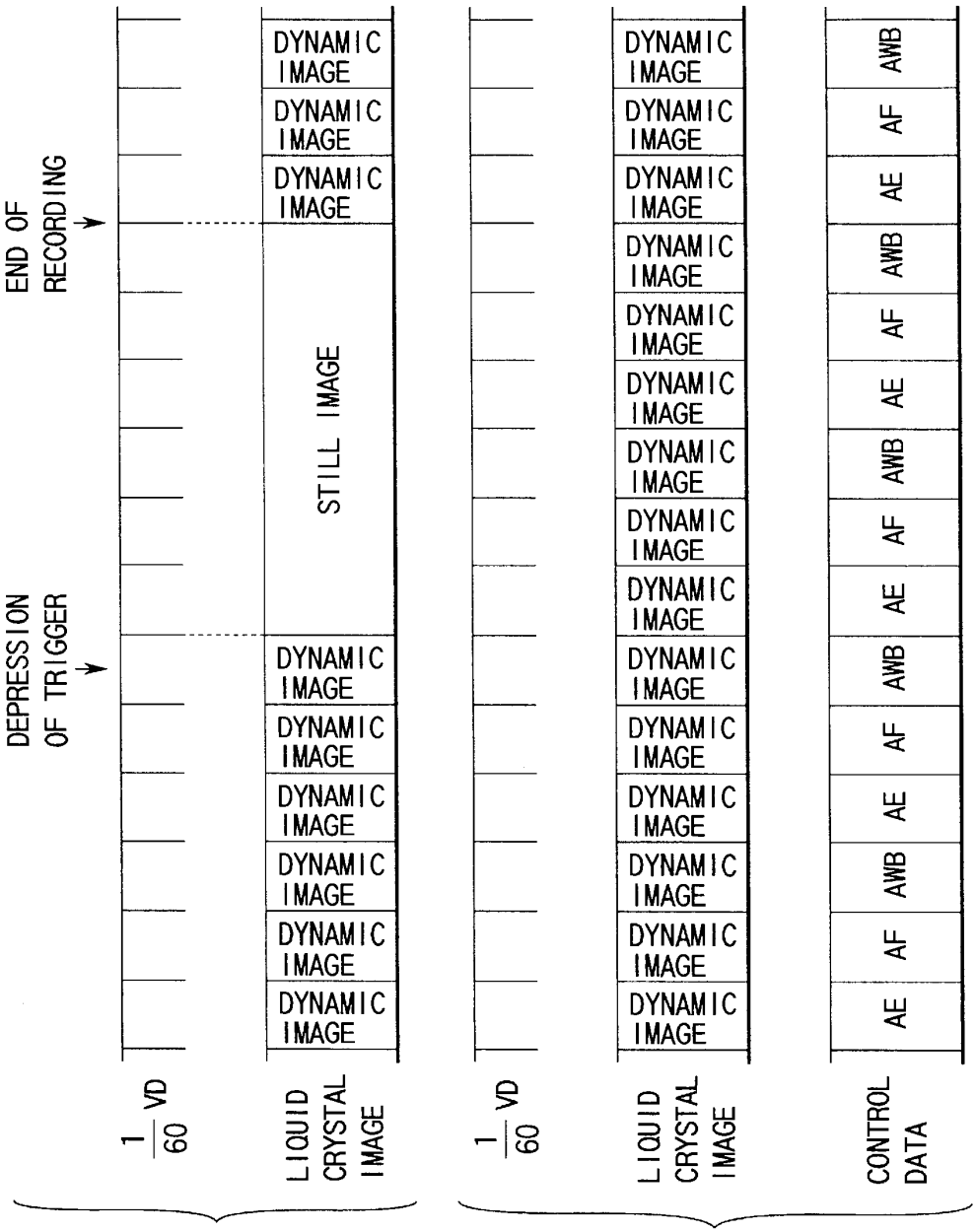

END OF RECORDING
DEPRESSION OF TRIGGER
DYNAMIC IMAGE
STILL IMAGE
1/60 VD
LIQUID CRYSTAL IMAGE
CONTROL DATA
AE
AF
AWB

FIG. 12

FIG. 13

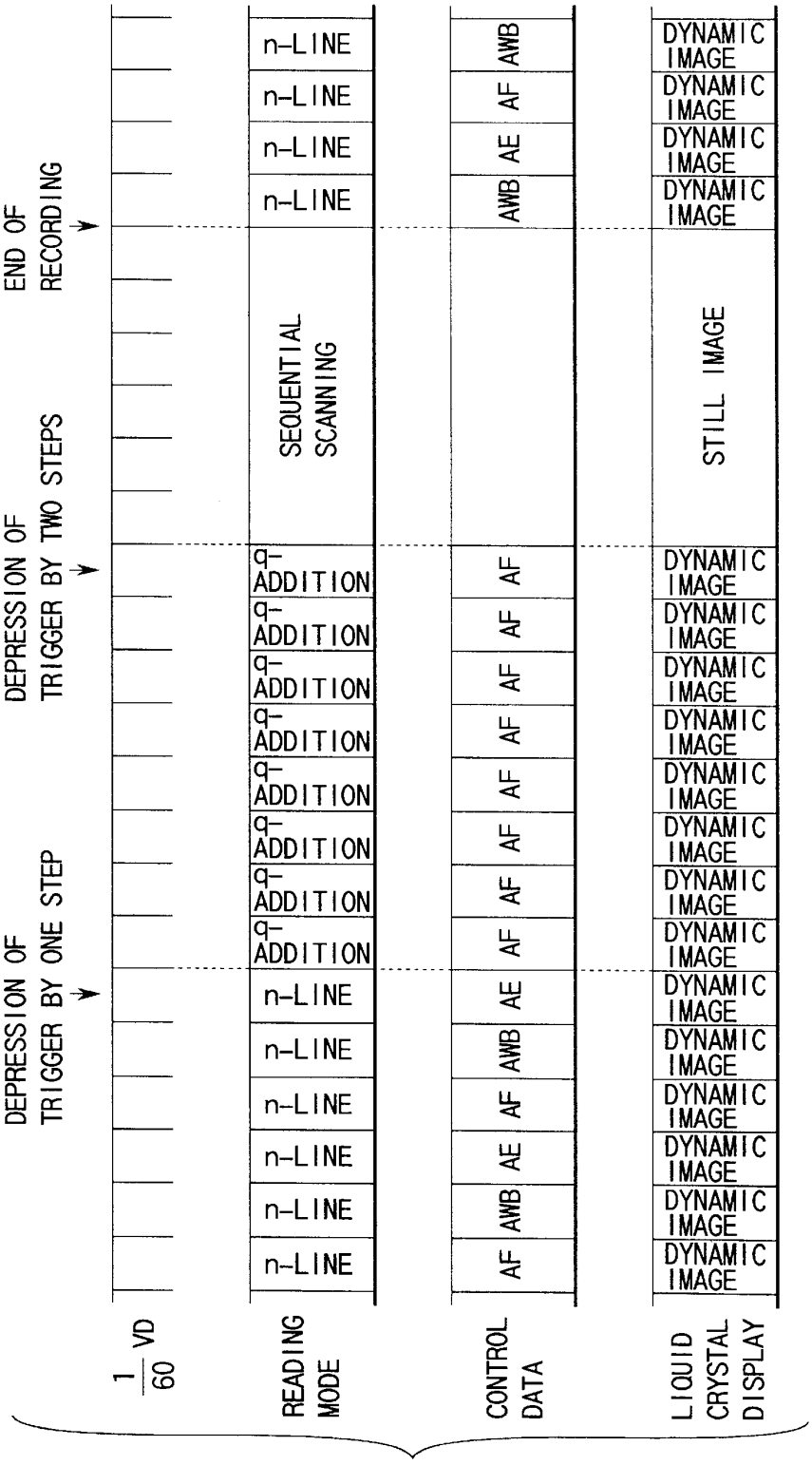

DEPRESSION OF TRIGGER BY ONE STEP
DEPRESSION OF TRIGGER BY TWO STEPS
END OF RECORDING
1/60 VD
READING MODE
CONTROL DATA
LIQUID CRYSTAL DISPLAY
n-LINE
SEQUENTIAL SCANNING
q-ADDITION
AF
AE
AWB
DYNAMIC IMAGE
STILL IMAGE

FIG. 14

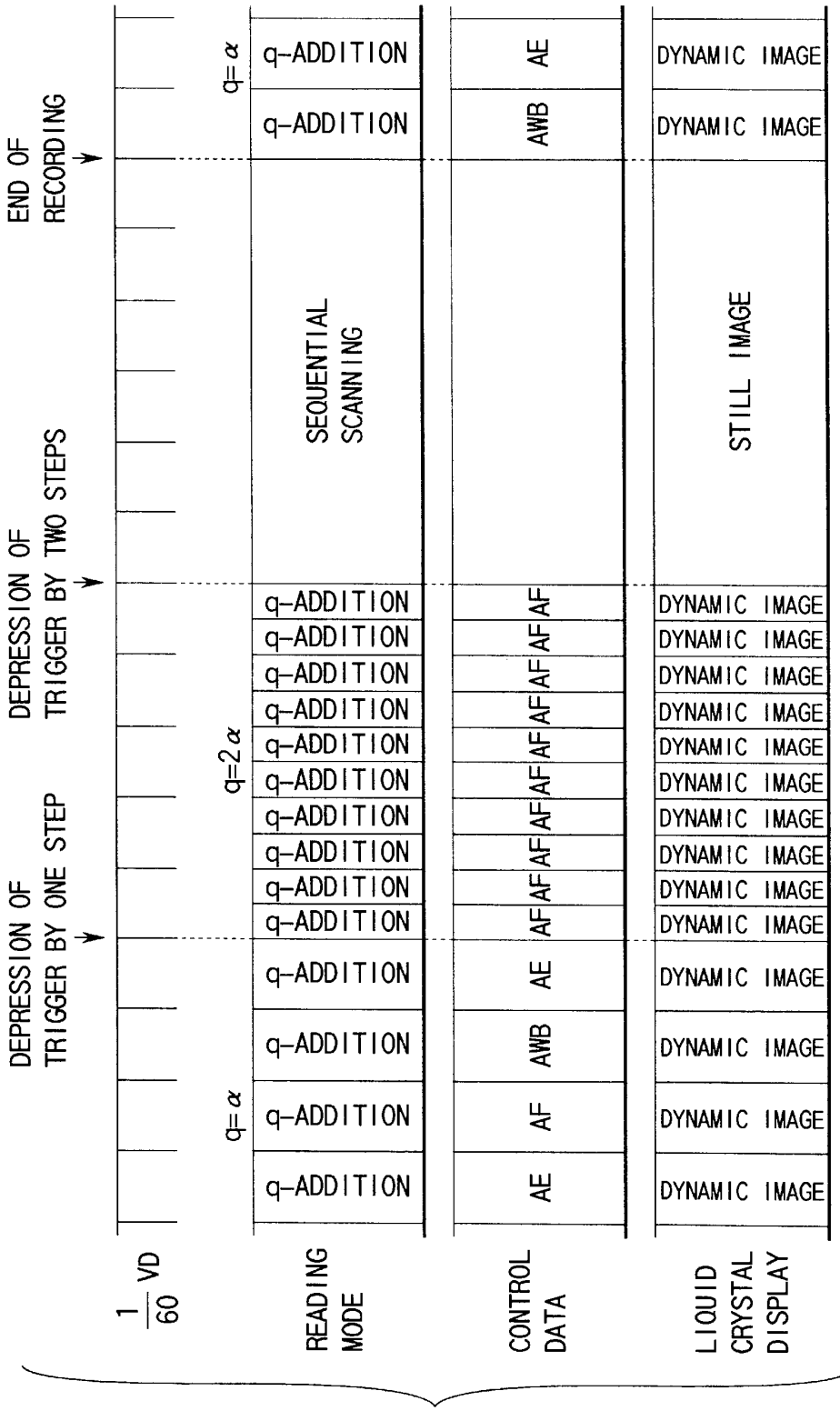

DEPRESSION OF TRIGGER BY ONE STEP
DEPRESSION OF TRIGGER BY TWO STEPS
END OF RECORDING
1/60 VD
READING MODE
CONTROL DATA
LIQUID CRYSTAL DISPLAY
q=α
q=2α
q=α
q-ADDITION
SEQUENTIAL SCANNING
AE
AWB
AF
DYNAMIC IMAGE
STILL IMAGE

FIG. 15

# IMAGE PICKUP APPARATUS CAPABLE OF PERFORMING BOTH A STILL IMAGE PROCESS AND A DYNAMIC IMAGE PROCESS

## BACKGROUND OF THE INVENTION

The present invention relates to an electronic imaging apparatus having a CCD image sensor, that is, a so-called electronic still camera.

Recently, research and development of electronic imaging apparatuses capable of inputting image data to multimedia equipment, so-called electronic still cameras have energetically been performed. In general, the electronic still camera obtains an image by using a CCD image sensor to display the obtained image on an electronic view finder, such as a liquid crystal panel, and to record the image on a recording medium by, for example, a magnetic means in accordance with depression of the trigger performed by a user.

Although the electronic still camera is a very easy device to use because no development of film is required, further improvement in the image quality and case of have been required of the electronic still camera. To satisfy the foregoing requirements, an image having the same angle of views which is the same as that of the image which must be photographed is required to be observed in real time through an electronic view finder, and a CCD image sensor having a large number of pixels must be used.

CCD image sensors having the number of effective pixels, which is larger than 1,000,000, have been realized. It is considered that CCD image sensors having larger pixels will be put into practical use. CCD image sensors arranged to photograph a still image and adapted to sequential scanning for sequentially, reading image signals for each line have been used in place of the conventional interlaced scanning. The reason for this lies in that prevention of deterioration in the image quality attributable to the difference in time required to read pixel signals from adjacent lines has been attempted.

The main stream of the operation clock frequencies of marketed A/D converters is about 15 MHz to about 20 MHz. When also reduction in the electric power consumption is attempted, higher drive frequencies are detrimental to the improvement. Frame rates of about 10 to 15 frames/second can be realized by the sequential scanning operation of CCD image sensors of 1,000,000-pixel class.

With the above-mentioned degree of the frame rate, the displayed image is recognized by the human eyes as a pseudo dynamic image (or motion picture) realized by frame advance in place of being recognized as a natural image. To display an image as a natural image for the human eyes, a frame rate of 30 to 60 frames/second is required.

## BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide an electronic imaging apparatus having a large number of pixels, for example, 1,000,000 pixels, and which is capable of displaying an image which is recognized as a dynamic image in a non-photographing mode even with a relatively low operation frequency, for example, 20 MHz or lower.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained particularly pointed out in the appended claims.



## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. **1** is a block diagram showing the structure of a circuit in an electronic imaging apparatus according to an embodiment of the present invention.

FIG. **2** shows the structure of a Bayer configuration color filter.

FIG. **3** shows a state where pixel signals are read in a high quality image mode.

FIG. **4** shows a state where pixel signals are read in a first high speed mode.

FIG. **5** shows a state where pixel signals are read in a second high speed mode.

FIG. **6** shows a state where pixel signals are read in a third high speed mode.

FIG. **7** shows addition of pixel signals in a vertical transfer passage relating to the mode shown in FIG. **6**.

FIG. **8** shows addition of pixel signals in a horizontal transfer passage relating to the mode shown in FIG. **6**.

FIG. **9** shows a state where pixel signals are read in a fourth high speed mode.

FIG. **10** shows addition of pixel signals in the vertical transfer passage relating to the mode shown in FIG. **9**.

FIG. **11** shows addition of pixel signals in the horizontal transfer passage relating to the mode shown in FIG. **9**.

FIG. **12** shows switch of images displayed on a liquid crystal display portion.

FIG. **13** shows a state where control data for AF, AWB and AE is sequentially obtained for each frame.

FIG. **14** shows an example of switching of a reading mode in accordance with the operation of a trigger.

FIG. **15** shows another example of switching of the reading mode in accordance with the operation of the trigger.

## DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings, an embodiment of the present invention will now be described.

FIG. **1** is a block diagram showing the structure in a circuit in an electronic imaging apparatus according to an embodiment of the present invention. The electronic imaging apparatus has a CCD image sensor **12**, a correlation double sampling circuit (CDS) **14**, a gain control amplifier (AMP) **16** and an analog-to-digital converter **18**. The CCD image sensor **12** is operated in response to a transfer pulse supplied from a timing generator **20**. The correlation double sampling circuit (CDS) **14** is operated in response to a sample holding pulse supplied from the timing generator **20**. The timing generator **20** is operated in synchronization with a signal generator **22** in accordance with a synchronizing signal generated by the signal generator **22**.

An image processing portion **26** processes pixel signals supplied from the A/D converter **18** to form an image. A DRAM **28** temporarily stores image data supplied from the image processing portion **26**, while a compressing/decompression circuit **30** compresses image data stored in the DRAM **28**. A recording medium **32** is used to record

compressed image data supplied from the compressing/decompression circuit **30**. The compressing/ decompression circuit **30** decompresses compressed image data recorded on the recording medium **32**, while the DRAM **28** is used to temporarily store decompressed image data supplied from the compressing/decompression circuit **30**.

An interface portion **36** is a terminal which enables data communication with an external unit, such as a monitor, a personal computer or the like. Thus, output of image data supplied from the image processing portion **26** or the DRAM **28** to the external unit is enabled or, in some cases, image data to be captured from the external unit.

A liquid crystal display portion **34** displays an image on the basis of the image data supplied from the image processing portion **26** or the decompressed image data supplied from the DRAM **28**.

A CPU **24** controls the timing generator **20**, the signal generator **22**, a lens drive system **38** and a stop control system **42**. Specifically, the CPU **24** follows an instruction to capture a still image issued from a trigger **46** to switch the operation mode of the CCD image sensor **12** and performs automatic focus control to drive a lens **40** in accordance with the image data supplied from the DRAM **28**, control to change the aperture of a stop **44** and control of the quality of exposure of the CCD image sensor **12**.

The CCD image sensor **12** is an inter-line type image sensor having 1,000,000 or more pixels and comprising a Bayer configuration color filter suitable for reading all pixels by line-sequential scanning. In this specification, "reading all pixels by line-sequential scanning" means sequential reading of data of pixels included in each line in the ascending line order as a first line, a second line and a third line to read all pixel signals as a result of one scanning operation.

The structure of the Bayer configuration color filter is shown in FIG. **2**. Referring to FIG. **2**, symbols R, G and B represent filter elements respectively permitting red, green and blue light to pass through. Each of the filter elements is disposed in front of one of photodiodes of the CCD image sensor **12**. The foregoing Bayer configuration color filter is structured in such a manner that R (red) and G (green) filter elements are alternately disposed on the odd-numbered lines, while G (green) and B (blue) filter elements are alternately disposed on the even-numbered lines. Moreover, G (green) filter elements are disposed to form a checkered pattern as a whole.

The CCD image sensor **12** is operated in either of a high quality image mode or a high speed mode. Switching of the operation mode is performed by the timing generator **20** in such a manner that the timing generator **20** changes the transfer pulse to be output to the CCD image sensor **12**. The high quality image mode is an operation mode in which all of the pixel signals obtained by the CCD image sensor **12** are read by the line-sequential scanning manner and with which a fine image can be obtained. However, time of 1/15 second to 1/10 second is required to read one image. On the other hand, the high speed mode is an operation mode arranged in such a manner that the number of horizontal transferring operations is reduced. The high speed mode is an operation mode in which pixel signals obtained by the CCD image sensor **12** are selectively read or added, and then read. Although the obtainable image quality is inferior to that obtainable from the high quality image mode, one image can be read in 1/60 second to 1/30 second. Therefore, an image can be obtained at a frame rate of 30 to 60 frames/second with which adaptation to a usual display of a dynamic image or motion picture is permitted.

In a usual state, that is, when no photographing operation is performed, the CCD image sensor **12** is operated in the high speed mode. Only when the trigger **46** has been depressed, that is, only when a photographing operation is performed, the CCD image sensor **12** is operated in the high quality image mode. During a period in which the CCD image sensor **12** is operated at the high speed mode, images are displayed on the liquid crystal display portion **34** at a frame rate of 30 to 60 frames/second, the images in the foregoing state being recognized as dynamic images. The fine image obtained in the high quality image mode is recorded on the recording medium **32**. After the operation for recording the still image has been ended, the reading mode for the CCD image sensor **12** is returned to the high speed mode. The foregoing operation will be described with reference to FIG. **12**.

Note that the electronic imaging apparatus may have a structure that the CCD image sensor **12** is operated in the high quality image mode also when the trigger **46** has been depressed. In the foregoing case, the image displayed on the liquid crystal display portion **34** is always recognized for the eyes of a human being as a dynamic image.

FIG. **3** illustrates a state where a pixel signal is read in the high quality image mode. In FIG. **3**, the left-hand columns indicate pixel signals on respective lines obtained by the CCD image sensor **12**, while the right-hand columns indicate pixel signals which are actually read. A consideration is made that odd-numbered lines include color data about red (R) in accordance with the correspondence to the color filter shown in FIG. **2**, the odd-numbered lines are expressed as CR. On the other hand even-numbered lines are expressed as CB because the even-numbered lines include color data about blue (B).

In the high quality image mode the CCD image sensor **12** sequentially outputs pixel signals for each line. That is, pixel signals for a first line are output. After output of pixel signals for the first line has been ended, pixel signals for a second line are output. After output of the pixel signals for the second line has been ended, pixel signals for a third line are output. Then, the same process is repeated, and finally pixel signals for an L th line are output.

The line-sequential scanning operation, arranged to alternately read lines (CR) including information indicating red and lines (CB) including information indicating blue, enables a high resolution image to be obtained. Since pixel signals for the adjacent lines are exposed for the same time, a high quality image can be obtained. However, time of 1/15 to 1/10 second is required to read all of the pixel signals.

A variety of reading manners may be employed for the high speed mode. Specifically, a variety of manners may be considered by changing the manner of selecting lines from which pixel signals are read and the manner of processing the selected lines. A representative portions of variety of modes adaptable to the electronic imaging apparatus will now be described.

FIG. **4** illustrates a state where pixel signals are read in a first high speed mode. In FIG. **4**, the left-hand column indicate pixel signals obtained by the CCD image sensor **12** for line units, while the right-hand column indicate, for line units, pixel signals which are actually read. Similarly to FIG. **3**, lines including color data about red (R) are expressed as CR and lines including color data about blue (B) are expressed as CB.

As shown in FIG. **4**, the foregoing high speed mode is arranged in such a manner that the CCD image sensor **12** sequentially outputs pixel signals for every three lines, that

is, outputs pixel signals at intervals of three lines in the vertical direction. That is, pixel signals of a third line are initially output. After output of the pixel signals of the third line has been ended, pixel signals of a sixth line are output. After output of pixel signals of a sixth line has been ended, pixel signals of a ninth line are output. Then, the same process is repeated. Finally, pixel signals of an L th line are output. Although FIG. **4** shows that pixel signals of the L th line are output finally, that is, L is a multiple of 3 for convenience, there is no inevitability that L is a multiple of 3.

In the CCD image sensor, time required to perform the horizontal transfer generally contributes to time required to read pixel signals. That is, the number of horizontal transfer operations determines time required to read pixel signals.

In the high'speed mode shown in FIG. **4**, the number of lines, from which pixel signals are actually read, is one-third of the overall lines. Therefore, the number of the horizontal transfer operations is one-third of the number required for the high quality image mode. Thus, pixel signals are substantially read in one-third time. That is, pixel signals for one image can be read in 1/45 to 1/30 second. Therefore, an image can be obtained at a frame rate of 30 to 45 frames/second. The foregoing frame rate is a value with which a usual display of a dynamic image can be realized.

Since pixel signals for every three lines are read in the high speed mode shown in FIG. **4** with respect to the color filter having the Bayer configuration, that is, since pixel signals for one line are read at intervals of three lines in the vertical direction, read pixel signals, that is lines (CR) including red color information and lines (CB) including blue color information are alternately disposed in the vertical direction on the right-hand columns shown in FIG. **4**. Therefore, a high resolution image can be obtained.

The configuration in which lines (CR) including red color information in the read pixel signal and lines (CB) including blue color information of the same are alternately positioned in the vertical direction is, in this specification, called "color line-sequential". Moreover, alternate reading of lines (CR) including red information and lines (CB) including blue information is called "color line-sequential scanning".

In the high speed mode shown in FIG. **4**, pixel signals for one line are read at intervals of three lines in the vertical direction. The number of lines is not limited to the foregoing number of lines. For example one line at intervals of five lines in the vertical direction may be read. As an alternative to this, pixel signals for one or three lines may be read at intervals of seven lines.

Also in the case where pixel signals for one line are read at the intervals of three lines in the vertical direction, the line to be read is not limited to the third line. The line to be read may be a first line or a second line.

In view of the foregoing, the first high speed mode described with reference to FIG. **4** is a mode in which pixel signals for n lines are read at intervals of m lines in the vertical direction (where m and n are natural numbers satisfying m>n). Specifically, the mode is a mode in which pixel signals for $(2\beta-1)$ lines are read at intervals of $(2\alpha-1)$ lines in the vertical direction (where $\alpha$ and $\beta$ are natural numbers satisfying $\alpha>\beta$).

In other words, the lines of the CCD image sensor are divided into a plurality of blocks in the vertical direction, each of the blocks including m lines, and the pixel signals for n lines are read from the each block. Specifically, the pixel signals for the $(2\beta-1)$ lines are read from the each block consisting of the $(2\alpha-1)$ lines.

In this case, time required to read pixel signals is substantially n/m of time required to read pixel signals in the high quality image mode, that is, $(2\beta-1)/(2\alpha-1)$. Pixel signals are read by the color line-sequential manner to the Bayer configuration color filter.

FIG. **5** illustrates a state where pixel signals are read by a second high speed mode. The meanings and expressions of CR and CB are the same as those shown in FIG. **4**.

As shown in FIG. **5**, the foregoing high speed mode is arranged in such a manner that the CCD image sensor **12** sequentially outputs pixel signals for two lines at intervals of three lines. That is, it outputs pixel signals for two lines at intervals of four lines in the vertical direction. That is, pixel signals for a first line are initially output. After output of the pixel signals for the first line has been ended, pixel signals for a second line is output. After output of the pixel signals for the second line has been ended, pixel signals for a fifth line are output. After output of the pixel signals for the fifth line has been ended, pixel signals for a sixth line are output. Then, the same process is repeated, and finally pixel signals for an L-**3** th line are output. Then, pixel signals for an L-**2** th line are output. Although FIG. **5** illustrates that L is a multiple of four for convenience, there is no inevitability that L is a multiple of four.

In the high speed mode shown in FIG. **5**, the actual number of lines from which pixel signals are read is half of the all of the lines. Therefore, the number of horizontal transfer operations is one-half of that required in the high quality image mode shown in FIG. **3**. Thus, pixel signals are read in substantially one-half time. That is, pixel signals for one image can be obtained in 1/30 second. Therefore, an image can be obtained at a frame rate of 30 frames/second. The frequency frame rate is a value with which usual display of dynamic image can be realized.

In the high speed mode shown in FIG. **5**, pixel signals for two lines are read at intervals of three lines to the color filter having the Bayer configuration. That is, pixel signals for two lines are read at intervals of four lines in the vertical direction. Therefore, the read pixel signals, that is, the right-hand columns shown in FIG. **5** are in the form of color line-sequential in which lines (CR) including red color information and lines (CB) including blue color information are alternately positioned in the vertical direction. Therefore, a high resolution image can be obtained.

In the high speed mode shown in FIG. **5**, pixel signals for the first line and the second line are read at intervals of four lines in the vertical direction. Therefore, read pixel signals include color information of the line. Thus, an image free from considerable moire can be obtained.

Although pixel signals for two lines are, in the high speed mode shown in FIG. **5**, read at intervals of four lines in the vertical direction, the number of lines is not limited to the foregoing number. For example, pixel signals for two lines may be read at intervals of 6 lines in the vertical direction. As an alternative to this, pixel signals for four lines may be read at intervals of 8 lines.

Also in the case where pixel signals for two lines are read at the intervals of four lines in the vertical direction, the lines to be read is not limited to the first and second lines. The lines may be the second line and a third line, or a third line and a fourth line or the first line and the fourth line.

In view of the foregoing, the second high speed mode described with reference to FIG. **5** is a mode in which pixel signals for n lines are read at intervals of m lines in the vertical direction (where m and n are natural numbers satisfying m>n). Specifically, the mode is a mode in which

pixel signals for 2β lines are read at intervals of 2α lines in the vertical direction (where a and D are natural numbers satisfying α>β).

In other words, the lines of the CCD image sensor are divided into a plurality of blocks in the vertical direction, each of the blocks including m lines, and the pixel signals for n lines are read from the each block. Specifically, the pixel signals for the 2β lines are read from the each block consisting of the 2α lines.

In this case, time required to read pixel signals is substantially β/α of time required to perform reading in the high quality image mode.

Specifically, it can be said that 2β lines are composed of adjacent lines or lines obtained by reducing even-numbered lines. In this case, pixel signals are read by the color line-sequential manner to the Bayer configuration color filter. The pixel signals to be read include color information of adjacent lines.

FIG. **6** illustrates a state where pixel signals are read by a third high speed mode. The meanings of the drawing and expressions of CR and CB are the same as those shown in FIG. **4**.

As shown in FIG. **6**, the foregoing high speed mode is arranged in such a manner that the CCD image sensor **12** adds and outputs pixel signals for two lines at intervals of three lines in the vertical direction. That is, pixel signals for a first line and pixel signals for a third line are initially added and output. Then, pixel signals for a fourth line and pixel signals for a sixth line are added and output. Then, the same process is repeated, and finally pixel signals for the L-**2** th line and pixel signals for an L th line are added and output. Although FIG. **6** illustrates that L is a multiple of 3 for convenience, there is no inevitability that L is a multiple of 3.

In the high speed mode shown in FIG. **6**, the actual number of read lines is one-third of all of the lines. Therefore, the number of horizontal transfer operations is one-third of that required in the high quality image mode shown in FIG. **3**. Thus, the pixel signals can substantially be read in one-third time. Therefore, pixel signals for one image can be obtained in 1/45 to 1/30 second. The foregoing frame rate is a value with which usual display of dynamic image can be realized.

In the high speed mode shown in FIG. **6**, pixel signals for two lines are added and read at intervals of three lines in the vertical direction to the Bayer configuration color filter. Therefore, read pixel signals are in the form of color line-sequential configuration in which lines (CR) including red information and lines (CB) including blue information are positioned alternately in the vertical direction. Therefore, a high resolution image can be obtained.

Since pixel signals for the uppermost line at intervals of three lines in the vertical direction and pixel signals for the lowermost line at the same are added and read in the high speed mode shown in FIG. **6**, read pixel signals include color information of adjacent lines. Therefore, an image free from considerable moiré can be obtained.

Addition of the pixel signals is performed in vertical transfer passages or a horizontal transfer passage. The addition in the vertical transfer passages will now be described, and then the addition in the horizontal transfer passage will be described.

FIG. **7** illustrates addition of pixel signals in the vertical transfer passages. Referring to FIG. **7**, each square indicates a photodiode which is each pixel of the CCD image sensor. Characters R, G and B of the alphabet indicate colors which are respectively recognized by the photodiode. The photodiodes positioned at relatively the same positions when the photodiodes are divided into three lines in the vertical direction are given one of subscripts A, B and C corresponding to the uppermost line, the central line and the lowermost line and added to any one of the characters R. G and B of the alphabet indicating the colors.

In other words, the photodiodes are divided into a plurality of blocks in the vertical direction, each of which includes three lines. In the every blocks, the photodiodes in the uppermost line are represented by one of the alphabetic characters R, G and B with the subscript A, the photodiodes in the central line are represented by one of the alphabetic characters R, G and B with the subscript B, and the photodiodes in the lowermost line are represented by one of the alphabetic characters R, G and B with the subscript C.

Addition of the pixel signals on the uppermost line (photodiodes each of which is indicated by the letter of the alphabet having the subscript A) and the pixel signals on the lowermost line (photodiode each of which is indicated by the letter of the alphabet having the subscript C) is performed, for example, as follows: as shown in FIG. **7**, initially, the pixel signals from the photodiodes indicated by the letter of the alphabet having the subscript A are shifted to a vertical transfer passage, and then the charges, which are the pixel signals, are stored in potential wells formed in the vertical transfer passages by the side of the photodiodes in the uppermost line. Then, the potential wells having the charge of the pixel signals are downwards shifted through the vertical transfer passages. Simultaneously with shift of the charges to the side of the photodiodes positioned downwards by two lines, that is, the photodiodes indicated by the letter of the alphabet having the subscript C, the pixel signals of the lowermost line photodiodes, that is, the photodiodes indicated by the letter of the alphabet having the subscript C are shifted to the vertical transfer passages. As a result, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript A and those shifted from the photodiodes indicated by the letter of the alphabet having the subscript C are collectively stored in the potential wells (indicated with an ellipse surrounding +shown in the drawing). That is, the pixel signals of the uppermost line photodiodes and the pixel signals of the lowermost photodiodes are added to each other. Then, the potential wells in which the added pixel signals are stored, are continuously moved on the vertical transfer passages in the downward direction to reach the horizontal transfer passage, and then shifted to the left so as to sequentially be read in line units.

The size of the potential wells may be the same as that of the potential wells which are used when all of the pixels are read, or may be different from therefrom.

If the size of the potential wells is the same as that of the potential wells which are used when all of the pixel signals are read, that is, if the capacity of the potential wells are the same as the capacity of the photodiodes when all of the pixels are read, the capacity of the photodiodes is preferably adjusted to one-half of the capacity of the potential wells by changing the overflow drain substrate voltage. In other words, the photodiodes are preferably operated with a dynamic range which is one half of that when all of the pixels are read. The foregoing change in the capacity, that is, the dynamic range prevents the charges from overflowing the vertical transfer passages after addition has been performed. Although the dynamic range of the photodiodes is limited to one-half, the following signal processing operation can be performed without any problem because the signal level after reading is the same as that when all pixels are read.

If the size of the potential wells is different from that of the potential wells which are used when all of the pixel signals are read, the size of the potential wells are preferably two times that of the potential wells which are used when all pixels are read if the photodiodes are operated without change in the dynamic range. The foregoing setting of the potential wells prevents charges from overflowing the vertical transfer passages after the addition. In this case, there is a merit in terms of the SN ratio because the dynamic range of the photodiodes can be fully used.

FIG. **8** illustrates addition of pixel signals in the horizontal transfer passage. The meanings of square and letters in the alphabet in the drawings are the same as those shown in FIG. **7**.

The pixel signals on the uppermost line and pixel signals on the lowermost line are added as follows. Referring to FIG. **8**, pixel signals of photodiodes indicated by the letter of the alphabet having the subscript A and pixel signals of the photodiodes indicated by the letter of the alphabet having the subscript C are collectively shifted to the vertical transfer passage so that charges which are the pixel signals are stored in potential wells (each of which is indicated by a white ellipse) formed on the side of each photodiode. Then, all of the potential wells are uniformly moved downwards on the vertical transfer passages. Even after the charges stored in the potential wells in the lowermost line divided into three lines have been shifted to the potential wells (each of which is indicated by an ellipse surrounding +as shown in the drawing), downward shift of the potential wells for only two lines is continued. Also the charges stored in the potential wells on the uppermost line divided into three lines are shifted to the potential well formed on the horizontal transfer passage. As a result, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript A and the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript C are stored in the potential wells on the horizontal transfer passage. That is, the pixel signals of the photodiodes on the uppermost line and the pixel signals of the photodiodes on the lowermost line are added. Then, the potential wells on the horizontal transfer passage are shifted to the left so as to sequentially be read in line units.

Since the horizontal transfer passage is formed on the outside of the image forming region differently from the vertical transfer passages extending between photodiodes, the potential wells formed on the horizontal transfer passage can have a capacity twice as large as that of the potential wells on the vertical transfer passages. Since the horizontal transfer passage is able to have potential wells each having a large capacity as described above, there is no possibility that charges overflow the horizontal transfer passage even if the photodiodes are operated with full dynamic ranges. In the foregoing case, there is a merit in terms of SN ratio because the dynamic range of the photodiodes can be fully used.

Although the high speed mode shown in FIG. **6** is arranged in such a manner that pixel signals for two lines are read at intervals of three lines in the vertical direction, the number of lines is not limited to the foregoing number. For example, pixel signals for two lines may be added and read at intervals of five lines in the vertical direction. As an alternative to this, pixel signals for two or three lines may be added and read at intervals of seven lines.

In view of the foregoing, the third high speed mode described with reference to FIG. **6** is a mode in which pixel signals for n lines at intervals of m lines in the vertical direction are added and read (where m and n are natural numbers satisfying m>n). Specifically, the foregoing mode is a mode for adding and reading pixel signals for **0** lines at intervals of (2β−1) lines in the vertical direction (where α and β are natural numbers satisfying 2α−1>β>1).

In other words, the lines of the CCD image sensor are divided into a plurality of blocks in the vertical direction, each of the blocks including m lines, and the pixel signals for n lines are read and added for the each block. Specifically, the pixel signals for the β lines are read and added for the each block consisting of the (2β−1) lines.

In this case, time required to read pixel signals is substantially n/m, that is, β/(2α−1) of time required to perform reading in the high quality image mode.

Specifically, the β lines include at least each of the uppermost and lowermost lines at intervals of the (2β−1) lines. That is, the β lines include the uppermost and lowermost lines of the each block. In this case, read pixel signals include color information of adjacent lines.

More specifically, the D lines is composed of odd-numbered lines including each of the uppermost and lowermost lines at intervals of the (2β−1) lines. That is, the β lines consist of the odd-numbered lines including the uppermost and lowermost lines of the each block. In this case, pixel signals are read by the color line-sequential manner to the Bayer configuration color filter.

The addition described with reference to FIG. **7** is addition in which shift of charges for n lines to the vertical transfer passage is divided into n times and vertical transfer is performed by m−1 times so that addition of n lines is performed in the vertical transfer passage, and then vertical transfer clocks are supplied in units of m times to perform transfer to the horizontal transfer passage.

The addition described with reference to FIG. **8** is arranged in which charges for n lines are shifted to the vertical transfer passage and vertical transfer clocks are supplied in units of m times to perform transfer to the horizontal transfer passage so that addition of n lines is performed in the horizontal transfer passage.

FIG. **9** illustrates a state where pixel signals are read in a fourth high speed mode. The meanings of the drawings and expressions CR and CB are the same as those shown in FIG. **4**.

As shown in FIG. **9**, the foregoing high speed mode is arranged in such a manner that the CCD image sensor **12** adds and outputs pixel signal for three lines consecutive in the vertical direction. That is, pixel signals for the first line, pixel signals for the second line and pixel signals for the third line are initially added and output. Then, pixel signals frequency the fourth line, pixel signals for the fifth line and pixel signals for the sixth line are added and output. Then, the same process is repeated, and finally pixel signals for the L-**2** th line, pixel signals for the L-**1** th line and pixel signals for the L th line are added and output. Although FIG. **9** illustrates that L is a multiple of 3 for convenience, there is no inevitability that L is a multiple of 3.

In the high speed mode shown in FIG. **9**, the number of lines which are actually read is one-third of all of the lines. Therefore, the number of horizontal transfer operations is one-third of the number in the high quality image mode shown in FIG. **3**. Thus, pixel signals are substantially read in one-third times. Therefore, pixel signals for one image can be obtained in 1/45 to 1/30 second. Therefore, an image can be obtained in a frame rate of 30 to 45 frames/second. The foregoing frame rate is a value with which a usual display of dynamic image can be realized.

Addition of the pixel signals are performed in the vertical transfer passages or the horizontal transfer passage. The addition in the vertical transfer passages will be first described. Then, the addition in the horizontal transfer passage will be described.

FIG. **10** illustrate the addition of pixel signals in the vertical transfer passages. The meanings of the square and alphabet are the same as those shown in FIG. **7**.

The addition of pixel signals is performed, for example, as follows. Referring to FIG. **10**, pixel signals of photodiodes indicated by the letter of the alphabet having the subscript A are initially shifted to the vertical transfer passages so that charges, which are pixel signals, are stored in the potential wells formed on the sides of the photodiodes. Then, the potential wells in which charges of the pixel signals of the photodiodes on the uppermost line are downwards moved through the vertical transfer passages. Simultaneously with shift of the charges to the photodiodes positioned downwards by one line, that is, the photodiodes indicated by the letter of the alphabet having the subscript B, pixel signals of photodiodes of a next line, that is, photodiodes indicated by the letter of the alphabet having the subscript B are shifted to the vertical transfer passages. As a result, charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript A and charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript B are collectively stored in the potential wells. Then, the potential wells in which charges of the pixel signals of the uppermost line and the next line are continuously moved downwards on the vertical transfer passages. Simultaneously with shift of the charges to the sides of the photodiodes positioned downwards by one line, that is, photodiodes indicated by the letter of the alphabet having the subscript C, pixel signals of the photodiodes of the lowermost line, that is, the photodiodes indicated by the letter of the alphabet having the subscript C are shifted to the vertical transfer passages. As a result, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript A, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript B and the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript C are collectively stored in the potential wells (indicated by ellipses each surrounding +shown in the drawing). That is, the pixel signals of the photodiodes on the uppermost line, the pixel signals of the photodiodes on the second line and the pixel signals of the photodiodes on the lower-most line are added. Then, the potential wells, in which the added pixel signals are stored, are continuously moved downwards on the vertical transfer passages. After the added pixel signals have been shifted to the horizontal transfer passage, they are shifted to the left so as to sequentially be read in line units.

The size of the potential wells may be the same as that of the potential wells which is used when all of the pixels are read, or may be different from therefrom.

If the size of the potential wells is the same as that of the potential wells which are used when all of the pixel signals are read, that is, if the capacity of the potential wells is the same as the capacity of the photodiodes when all of the pixels are read, the capacity of the photodiodes is preferably adjusted to one-third of the capacity of the potential wells by changing the overflow drain substrate voltage. In other words, the photodiodes are preferably operated with a dynamic range which is one-third of that when all of the pixels are read. The foregoing change in the capacity, that is, the dynamic range prevents the charges from overflowing the vertical transfer passages after addition has been performed. Although the dynamic range of the photodiodes is limited to one-third, the following signal processing operation can be performed without any problem because the signal level after reading is the same as that when all pixels are read.

If the size of the potential wells is different from that of the potential wells which are used when all of the pixel signals are read, the size of the potential well is preferably three times that of the potential wells which are used when all pixels are read if the photodiodes are operated without change in the dynamic range. The foregoing setting of the potential wells prevents charges from overflowing the vertical transfer passages after the addition. In this case, there is a merit in terms of the SN ratio because the dynamic range of the photodiodes can be fully used.

FIG. **11** shows addition of pixel signals in the horizontal transfer passage. The meanings of the square and alphabet are the same as those shown in FIG. **7**.

Addition of the pixel signals is performed as follows: referring to FIG. **11**, pixel signals of photodiodes indicated by the letter of the alphabet having the subscript A, pixel signals of photodiodes indicated by the letter of the alphabet having the subscript B and pixel signals of photodiodes indicated by the letter of the alphabet having the subscript C are collectively shifted to the vertical transfer passage so that charges, which are the pixel signals, are stored in potential wells (indicated by white ellipses shown in the drawing) formed on the sides of the photodiodes. Then, all of the potential wells are uniformly moved downwards on the vertical transfer passage. Even after the charges stored in the potential wells of the lowermost line divided every three lines have been shifted to the potential wells (each of which is indicated by an ellipse surrounding +) formed in the horizontal transfer passage, the downward movement of the potential wells for only the two lines is continued. Also the charges stored in the potential wells on the next line divided every three lines and charges stored in the potential wells on the uppermost are shifted to the potential wells formed on the horizontal transfer passage. As a result, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript A, the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript B and the charges shifted from the photodiodes indicated by the letter of the alphabet having the subscript C are stored in the potential wells in the horizontal transfer passage. That is, pixel signal of the photodiodes of the three lines continued in the vertical direction are added. Then, the potential wells in the horizontal transfer passage are shifted to the left so as to sequentially be read in line units.

Since the horizontal transfer passage is positioned on the outside of the image forming region differently from the vertical transfer passage extending among the photodiodes, the width of the horizontal transfer passage can be enlarged. That is, the capacity of the horizontal transfer passage can be enlarged. Therefore, the capacity of the potential wells, which are formed in the horizontal transfer passage, can be enlarged to three or more times the capacity of the potential wells in the vertical transfer passages. Since the large-capacity potential wells can be formed in the horizontal transfer passage, there is no possibility that charges overflow the horizontal transfer passage. In this case, there is a merit in terms of SN ratio because the dynamic range of the photodiode can fully be used.

In the high speed mode shown in FIG. **9**, pixel signal for three lines continued in the vertical direction are added and

read. However, the number of lines is not limited to the foregoing number. For example, pixel signals for four or five lines continued in the vertical direction may be added and read.

When pixel signals for even-numbered lines in the vertical direction are added and read, the pixel signals read to the Bayer configuration color filter include R+2G+B color information items. The foregoing value is close to the structure of a brightness signal and thus information of contrast can easily be obtained. Therefore, it is suitable for data for controlling automatic focusing.

In view of the foregoing, the fourth high speed mode described with reference to FIG. **9** is a mode in which pixel signal for q lines continued in the vertical direction (where q is a natural number).

The addition described with reference to FIG. **10** is addition in which shift of charges for q lines to the vertical transfer passage is divided into q times and vertical transfer is performed q−1 times to addition of n lines is performed in the vertical transfer passage after which vertical transfer clocks are supplied in units of q times to perform transfer to the horizontal transfer passage.

The addition described with reference to FIG. **11** is addition in which charges for q lines is shifted to the vertical transfer passage, after which vertical transfer clocks are supplied in units of q times to perform transfer to the horizontal transfer passage so that addition of q lines is performed in the horizontal transfer passage.

As described above, the CCD image sensor **12** is, in a usual state, operated in the high speed mode and operated in the high quality image mode only when the trigger **46** is depressed to record a fine image on the recording medium **32**. As shown in, for example, FIG. **12**, the liquid crystal display portion **34** displays one image at each frame, that is, every 1/60 second. Immediately after the trigger **46** has been depressed, one image is displayed for time corresponding to six frames, that is, in 1/10 second. Display of one image in 1/60 second, that is, display of an image at a frame rate of 60 frames/second can be recognized for the eyes of a human being as a dynamic image. Therefore, an image obtainable in the high speed mode is expressed as a "dynamic image", while an image obtainable in the high quality image mode is expressed as a "still image" so as to be distinguished from the dynamic image. In relation to this, an image obtainable in the high speed mode is sometimes expressed as a "dynamic image" and an image obtainable from the high quality image mode is sometimes expressed as a "still image" in the following description.

Since time (1/10 second in the structure shown in FIG. **12**) corresponding to a plurality of frames is required to read a still image, the still image is displayed on the liquid crystal display portion **34** for a certain period after the trigger has been depressed. During this, the still image is recorded on the recording medium **32**. After the still image has been recorded, the reading mode of the CCD image sensor **12** is again switched to the high speed mode so that a dynamic is again displayed on the liquid crystal display portion **34**.

The electronic imaging apparatus according to this embodiment obtains control data for an automatic focusing mechanism (AF), an automatic white balance adjustment mechanism (AWB) and an automatic exposure adjustment mechanism (AE) every frame, that is, every 1/60 second. Control data for AF, AWB and AE is obtained by the CPU **24** in accordance with image data temporarily stored in the DRAM **28** in the mode in which a partial image is read. That is, the CPU **24** extracts image data temporarily stored in the DRAM **28** at every frame, that is, every 1/60 second to subject image data to a proper calculation process to calculate data for any one of AF, AWB and AE. Control for AF, AWB and AE is sequentially calculated for each frame, and calculations of control data is repeatedly performed during display of a dynamic image.

Calculated control data for AF is supplied to the lens drive system **38** so that the lens drive system **38** shift the lens **40** in the direction of optical axis in accordance with supplied control data. Control data for AE is supplied to the stop control system **42** so that the stop control system **42** adjusts the aperture diameter of the stop **44** in accordance with the supplied control data. Control data for AWB is supplied to the image processing portion **26** so as to be used to correct the hue of the image.

Since control data for AF, AWB and AE is obtained at each frame, the DRAM **28** for temporarily storing image data may be employed as an electric circuit for obtaining control data. Although the conventional apparatus arranged to simultaneously obtain control data for AF, AWB and AE requires three systems of exclusive circuits, the apparatus according to this embodiment is not need to have the foregoing circuits.

The high speed mode for displaying a dynamic image may be switched in the above-mentioned four modes. Moreover, a manner of calculating control data may be switched as the mode is switched. The reading mode is switched during display of a dynamic image is performed by, for example, operating the trigger. In this case, the trigger **46** is a two-step depression type trigger which acts as a first switch when the trigger is depressed by one step and acts as a second switch when the trigger is depressed by two steps after that. FIG. **14** illustrates an example of switch of the reading mode in accordance with the operation of the trigger.

In a usual state, the CCD image sensor **12** is operated in any one of the first, second and third high speed modes. FIG. **14** illustrates the foregoing high speed modes as "n-line" mode. During this, control data for AF, AWB and AE is repeatedly calculated for each frame in accordance with image data obtained from the n-line mode so that AF control, AWB control and AE control are performed.

In a certain time after the trigger **46** has been depressed by one step, the CCD image sensor **12** is operated in the fourth high speed mode. FIG. **14** illustrates the foregoing high speed mode as a "q-addition" mode. During this, control for the AF is calculated for each frame in accordance with image data obtained in the q-addition mode so that only AF control is performed. That is, a predetermined time after the trigger has been depressed by one step is assigned to only AF control. Since pixel signals read in the q-addition mode include R+2G+B color information items and close to the structure of the brightness signal as described above, contrast information can easily be obtained and it is suitable for use in calculating control data for the AF. Therefore, the AF control using the optimal control data is performed in the foregoing period.

When the trigger **46** is depressed by two steps, the CCD image sensor **12** is switched to the reading mode immediately in the case of that a predetermined time for only the AF control has elapsed or after the predetermined time pass in the case of that the predetermined time has not been elapsed so as to be operated in the high quality image mode by the sequential scanning manner. Then, a fine image obtained by the sequential scanning operation is recorded on the recording medium **32** in 6 frames, that is, 1/10 second. After the still image has been recorded, the reading mode of the CCD image sensor **12** is returned to the n-line mode.

Since only the AF control is performed in accordance with optimal control data because of the switch of the reading mode and change of the control data, a further focused fine image can efficiently be obtained.

FIG. **15** illustrates another example of the switch of the reading mode which is performed in accordance with the operation of the trigger. In this example the CCD image sensor **12** is always operated in the q-addition mode except for the number of addition lines immediately before the still image is recorded is twice the number in the usual operation.

In a usual state, the CCD image sensor **12** is operated in the q-addition mode in which pixel signals for α lines (α is a natural number not smaller than 2) are added and read. During this, control data for AF, AWB and AE is repeatedly calculated at intervals of 1/60 second in accordance with image data obtained in the q-addition mode so that the AF control, the AWB control and the AE control are performed.

In a certain period after depression of the trigger **46** by one step, the CCD image sensor **12** is operated in the q-addition mode in which pixel signals for 2α lines continued in the vertical direction are added and read. During this, control data for the AF is calculated at intervals of 1/120 second in accordance with image data obtained in the q-addition mode. In accordance with control data, the AF control is performed.

When the trigger **46** is depressed by two steps, reading mode of the CCD image sensor **12** is switched immediately in the case of that a predetermined time for only the AF control has elapsed or after the predetermined time pass in the case of that the predetermined time has not been elapsed so as to be operated in the high quality image mode by the sequential scanning manner. Then, a fine image obtained by the sequential scanning operation is recorded on the recording medium **32** in 6 frames, that is, 1/10 second. After the still image has been recorded, the reading mode of the CCD image sensor **12** is returned to the q-addition mode for a usual state.

Since only the AF control is performed in accordance with control data which can be obtained at a rate which is twice the rate in a usual state because of switch of the reading mode and change of control data, a fine image focused more quickly can efficiently be obtained at an optimal shutter release opportunity.

As easily understood from the above description, the CCD image sensor is, when no photographing operation is performed, operated in a high speed mode in which, for example, pixel signals for n lines are read at intervals of m lines in the vertical direction. As a result, an electronic imaging apparatus can be obtained which has a 1,000,000 pixel class CCD image sensor which displays an image which can be recognized as dynamic images when no photographing operation is performed even with an operation frame rate is not higher than 20 MHz.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

**1**. An electronic imaging apparatus comprising:

a solid state imaging device;

a multistep switch for switching an operation mode of the solid state imaging device, the operation mode including a first operation mode, a second operation mode which starts in response to a first stage of the multistep switch, and a third operation mode which starts in response to a second stage of the multistep switch;

control means for extracting pixel signals from the solid state imaging device, wherein the control means: extracts pixel signals of the solid state imaging device adding n lines in units of m lines in a vertical direction (where n is a natural number and m>n) to display a dynamic image when the solid state imaging device is operated in the first operation mode, extracts pixel signals of the solid state imaging device adding q lines in units of q successive lines in the vertical direction (where q is a natural number) when the solid state imaging device is operated in the second operation mode, and extracts all pixel signals of the solid state imaging device by sequential scanning to record a still image when the solid state imaging device is operated in the third operation mode.

**2**. An electronic imaging apparatus according to claim **1**, wherein the solid state imaging device includes a Bayer configuration color filter, and m=2α−1 and n=β (where α and β are natural numbers and 2α−1>β>1).

**3**. An electronic imaging apparatus according to claim **1**, wherein when the solid state imaging device is operated in one of the first and second operation modes, an output signal from the solid state imaging device is used as one of AF information AE information and AWB information, and control data for one of AF, AE and AWB is repeatedly calculated in turn for each frame.

**4**. An electronic imaging apparatus according to claim **1**, wherein when the solid state imaging device is operated in the second operation mode, an output signal from the solid state imaging device is used as AF information, and control data for AF is repeatedly calculated for each frame.

**5**. An electronic imaging apparatus comprising:

a solid state imaging device;

a multistep switch for switching an operation mode of the solid state imaging device, the operation mode including a first operation mode, a second operation mode which starts in response to a first stage of the multistep switch, and a third operation mode which starts in response to a second stage of the multistep switch;

control means for extracting pixel signals from the solid state imaging device, wherein the control means: reads pixel signals of a part of lines in the solid state imaging device to repeatedly extract the pixel signals with a first rate to display a dynamic image when the solid state imaging device is operated in the first operation mode, reads pixel signals of a part of lines in the solid state imaging device to repeatedly extract the pixel signals with a second rate higher than the first rate when the solid state imaging device is operated in the second operation mode, and extracts all pixel signals of the solid state imaging device by sequential scanning to record a still image when the solid state imaging device is operated in the third operation mode.

**6**. An electronic imaging apparatus according to claims **5**, wherein when the solid state imaging device is operated in one of the first and second operation modes, an output signal from the solid state imaging device is used as one of AF information, AE information and AWB information, and control data for one of AF, AE and AWB is repeatedly calculated in turn for each frame.

**7**. An electronic imaging apparatus according to claim **5**, wherein when the solid state imaging device is operated in the second operation mode, an output signal from the solid state imaging device is used as AF information, and control data for A is repeatedly calculated for each frame.

* * * * *

SONY

# Semiconductor Integrated Circuit Data Book 1990

## PREFACE

This is the 1990 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

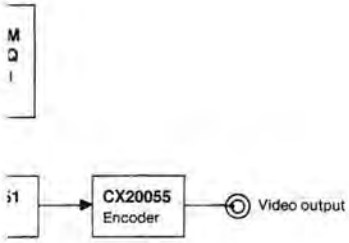
In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

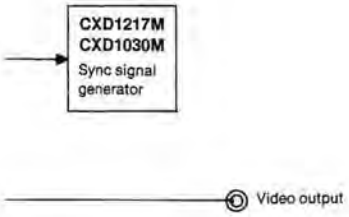
Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. **Sony** cannot assume responsibility for any problems arising out of the use of these circuits.

# Contents

· SYSTEM

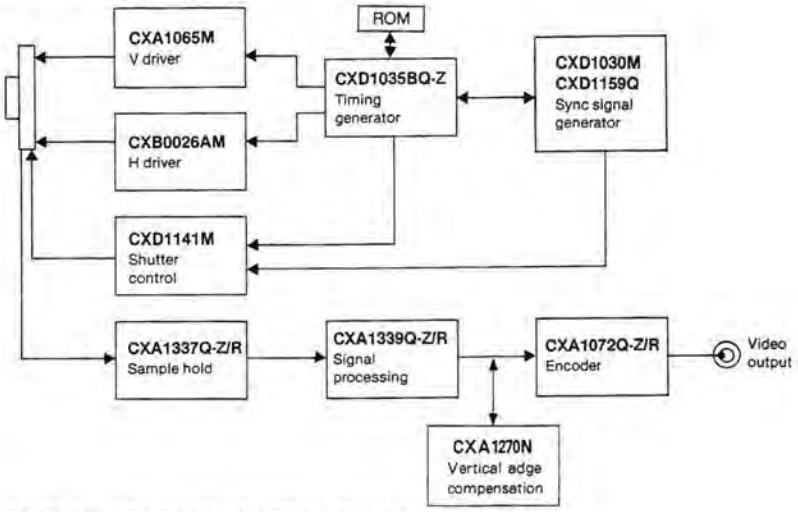



'STEM



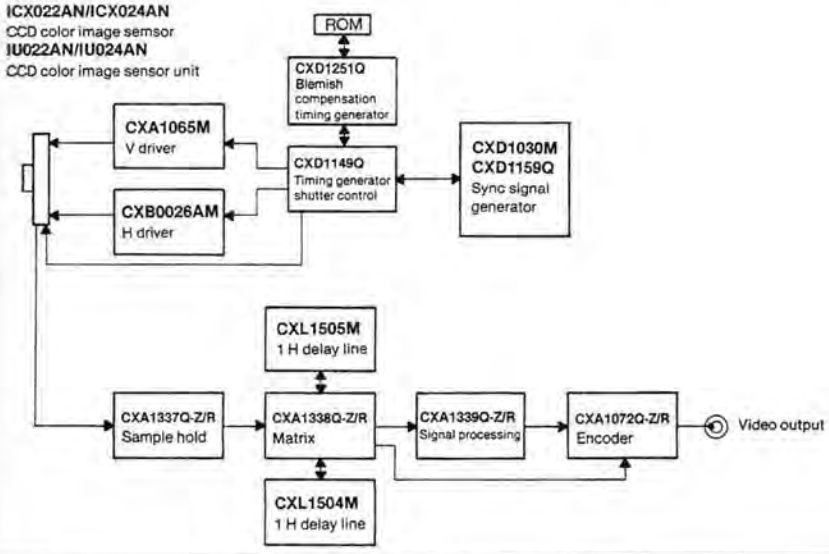

■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3" LENS SYSTEM

**ICX022AK/ICX024AK**
CCD color image sensor
**IU022AK/IU024AK**
CCD color image sensor unit




■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3" LENS SYSTEM

**ICX022AN/ICX024AN**
CCD color image sensor
**IU022AN/IU024AN**
CCD color image sensor unit



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# ICX022AK-3

## Interline-type CCD Solid Image Sensor

**Description**

ICX022AK-3 is an interline-type CCD solid imaging device designed for color video cameras.
Effective pixels number 768 horizontally and 493 vertically.

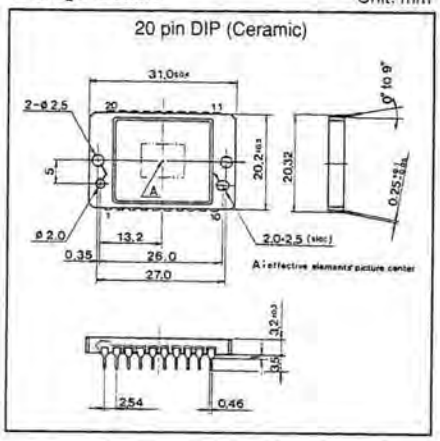
Color filters incorporated Ye, G and Cy are vertical stripe filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

**Element Structure**

- Interline type CCD image sensor
- Effective pixels: 768 (H) x 493 (V)
- Image size: 2/3 inches (8.8 mm (H) x 6.6 mm (V))
- Color filters (on-chip): Ye, G, Cy vertical stripe filters
- Field integration system
- Electronic shutter function
- Anti-blooming function
- Chip size: 10.0 mm (H) x 8.2 mm (V)
- Unit Cell size: 11.0 µm (H) x 13.0 µm (V)
- Effective optical black
  Horizontal: Front 5pixels
  Back 45pixels
  Vertical: Front 16pixels
  Back 4pixels
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)

**Package Outline** Unit: mm



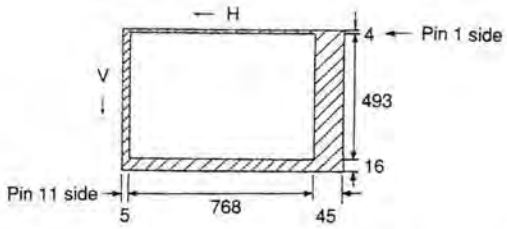




**Fig. 1 Optical black configuration**

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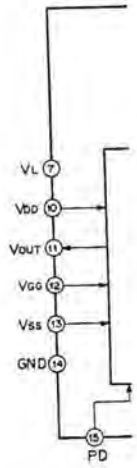
**Pin Configuration and (Top View)**

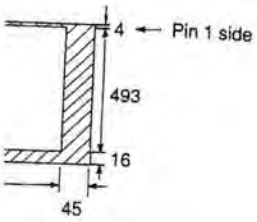
| No. | Symbol | |
|---|---|---|
| 1 | Vφ4 | V |
| 2 | Vφ3 | V |
| 3 | Vφ2 | V |
| 4 | SUB | S |
| 5 | GND | G |
| 6 | Vφ1 | V |
| 7 | VL | R |
| 8 | NC | |
| 9 | NC | |
| 10 | VDD | G |

**Imaging Device Funct**



# (022AK-3

Unit: mm

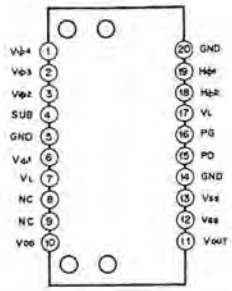




**k configuration**

70609A-YA

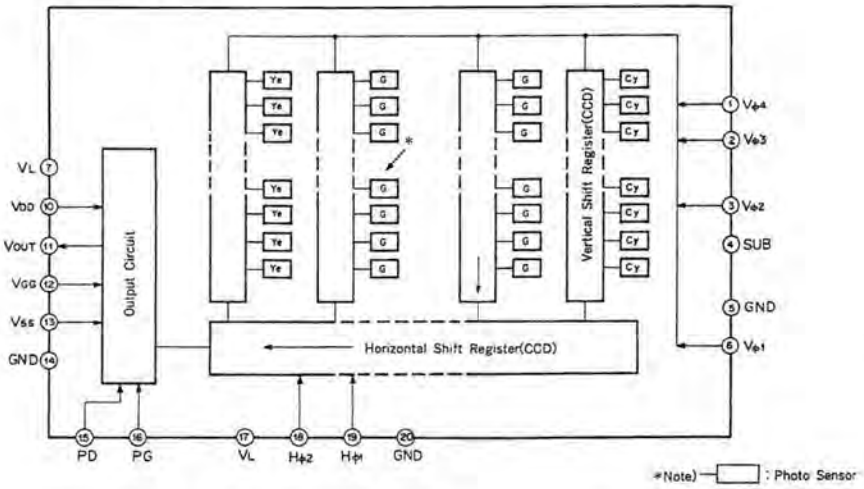


**Pin Configuration and Description**
**(Top View)**




| No. | Symbol | Description | No. | Symbol | Description |
|---|---|---|---|---|---|
| 1 | $V_{\phi 4}$ | Vertical register transfer clock | 11 | $V_{OUT}$ | Signal output |
| 2 | $V_{\phi 3}$ | Vertical register transfer clock | 12 | $V_{GG}$ | Output amplifier gate |
| 3 | $V_{\phi 2}$ | Vertical register transfer clock | 13 | $G_{SS}$ | Output amplifier source |
| 4 | SUB | Substrate (OFD) bias | 14 | GND | GND |
| 5 | GND | GND | 15 | PD | Pre-charge drain bias |
| 6 | $V_{\phi 1}$ | Vertical register transfer clock | 16 | PG | Output reset clock |
| 7 | $V_L$ | Protection transistor bias | 17 | $V_L$ | Protection transistor bias |
| 8 | NC | | 18 | $H_{\phi 2}$ | Horizontal register transfer clock |
| 9 | NC | | 19 | $H_{\phi 1}$ | Horizontal register transfer clock |
| 10 | $V_{DD}$ | Output amplifier drain supply | 20 | GND | GND |

**Imaging Device Function Block**



**SONY** **CXD1030M**

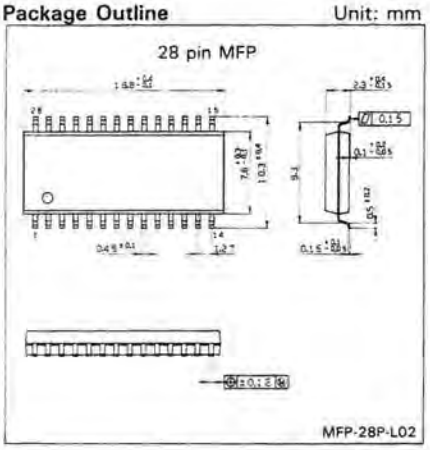
## Sync. Signal Generator for Camera

### Description

The CXD1030M is a sync. signal generator for video cameras.

### Package Outline

Unit: mm




### Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption (Standard NTSC: 25 mW; PAL: 30 mW)
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync.

### Function

Sync. signal generator

### Structure

Silicon gate CMOS IC

### Application

Video • Camera

### Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | $V_{SS}$* − 0.3 to 7.0 | V |
| • Input voltage | $V_I$ | $V_{SS}$* − 0.3 to $V_{DD}$ + 0.3 | V |
| • Output voltage | $V_O$ | $V_{SS}$* − 0.3 to $V_{DD}$ + 0.3 | V |
| • Operating temperature | $T_{opr}$ | − 20 to + 75 | °C |
| • Storage temperature | $T_{stg}$ | − 55 to + 150 | °C |

* $V_{SS}$ = 0V

### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 4.50 to 5.50 | V |
| • Operating temperature | $T_{opr}$ | − 20 to + 75 | °C |

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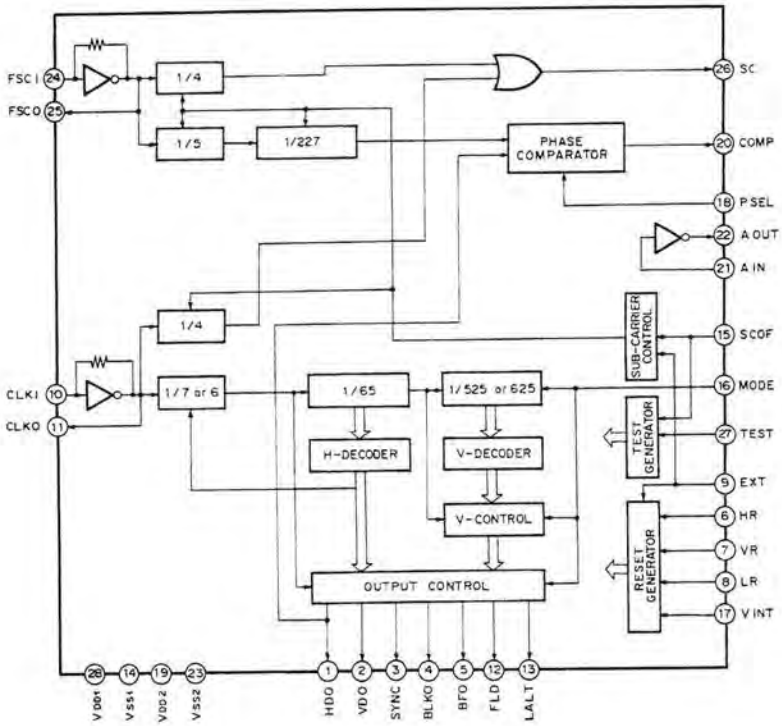
## Block Diagram







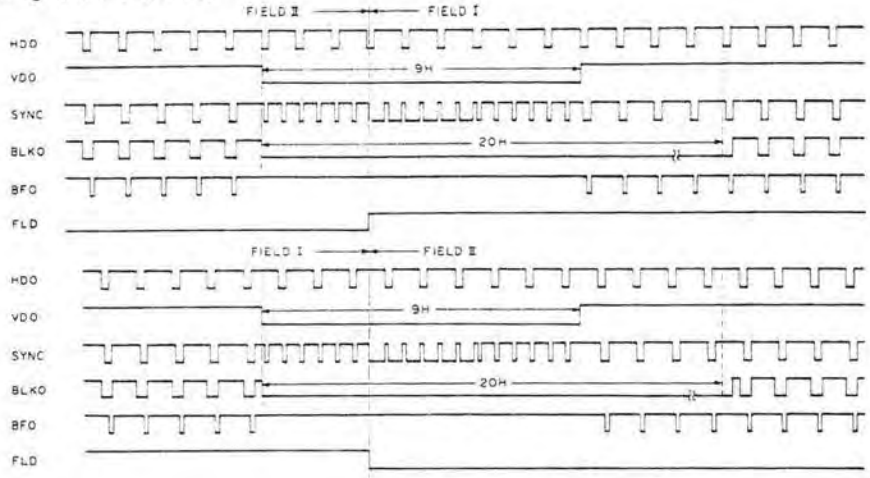

## Pin Configuration (Top \

1 pin indication

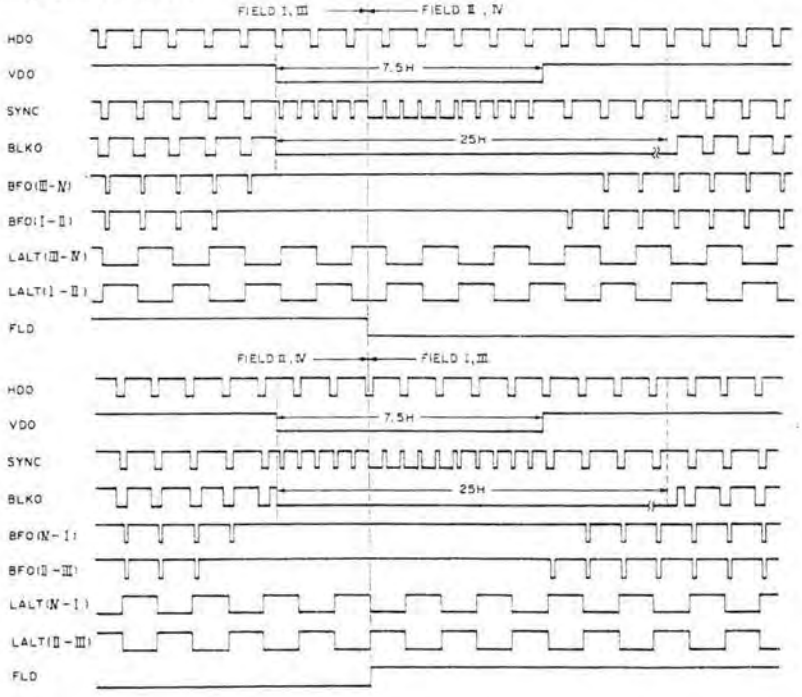
## Pin Description

| No. | Symbol | I/O |
|---|---|---|
| 1 | HDO | O |
| 2 | VDO | O |
| 3 | SYNC | O |
| 4 | BLKO | O |
| 5 | BFO | O |
| 6 | HR | I |
| 7 | VR | I |
| 8 | LR | I |
| 9 | EXT | I |
| 10 | CLKI | I |
| 11 | CLKO | O |
| 12 | FLD | O |
| 13 | LALT | O |
| 14 | $V_{SS1}$ | – |
| 15 | SCOF | I |
| 16 | MODE | I |
| 17 | VINT | I |
| 18 | PSEL | I |
| 19 | $V_{DD2}$ | – |
| 20 | COMP | O |
| 21 | AIN | I |
| 22 | AOUT | O |
| 23 | $V_{SS2}$ | – |
| 24 | FSCI | I |
| 25 | FSCO | O |
| 26 | SC | O |
| 27 | TEST | I |
| 28 | $V_{DD1}$ | – |

## Timing Chart V (NTSC)



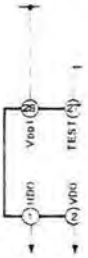

## Timing Chart V (PAL)



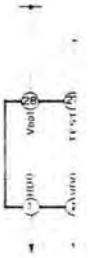





## Application Circuits
## NTSC (Internal mode



## PAL (Filter configura



## PAL (Filter configur

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# CXD1035BQ-Z

## CCD Camera Scanning System Timing Signal Generator

**Description**

CXD1035BQ-Z is a CMOS type LSI developed for use with the scanning system of both ICX022AK (NTSC) and ICX024AK (PAL).

This IC is employed in conjunction with either CXD1030M or CXD1158M (synchronized signal generator).

48pin QFP (Plastic)

**Features**

- Generates drive pulses for imagers (ICX022AK, ICX024AK).
- Generates signal processing pulse for color cameras.
- Switchover of NTSC/PAL modes is possible.
- Blemish compensation is possible (through usage of external ROM).

**Structure**

Silicon gate CMOS IC

**Absolute Maximum Ratings (Ta=25°C, Vss=0V)**

| | | | | | |
|---|---|---|---|---|---|
| • Supply voltage | $V_{DD}$ | Vss−0.5 | to | 6.0 | V |
| • Input voltage | $V_I$ | Vss−0.5 | to | $V_{DD}$+0.5 | V |
| • Output voltage | $V_O$ | Vss−0.5 | to | V | V |
| • Operating temperature | Topr | −25 | to | +85 | °C |
| • Storage temperature | Tstg | −40 | to | +125 | °C |
| • Allowable power dissipation | $P_D$ | | 500 | | mW |

**Recommended Operating Conditions**

| | | | | | |
|---|---|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 4.75 | to | 5.25 | V |
| • Operating temperature | Topr | −20 | to | +75 | °C |

E89Z23-YA



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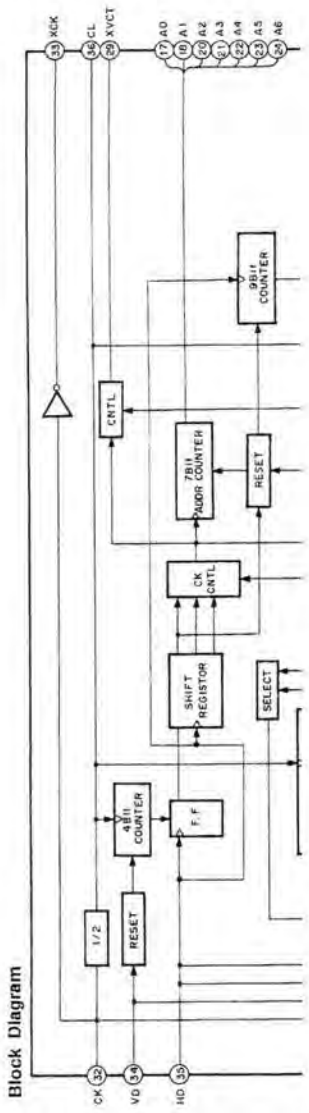
Block Diagram



# )1035BQ-Z

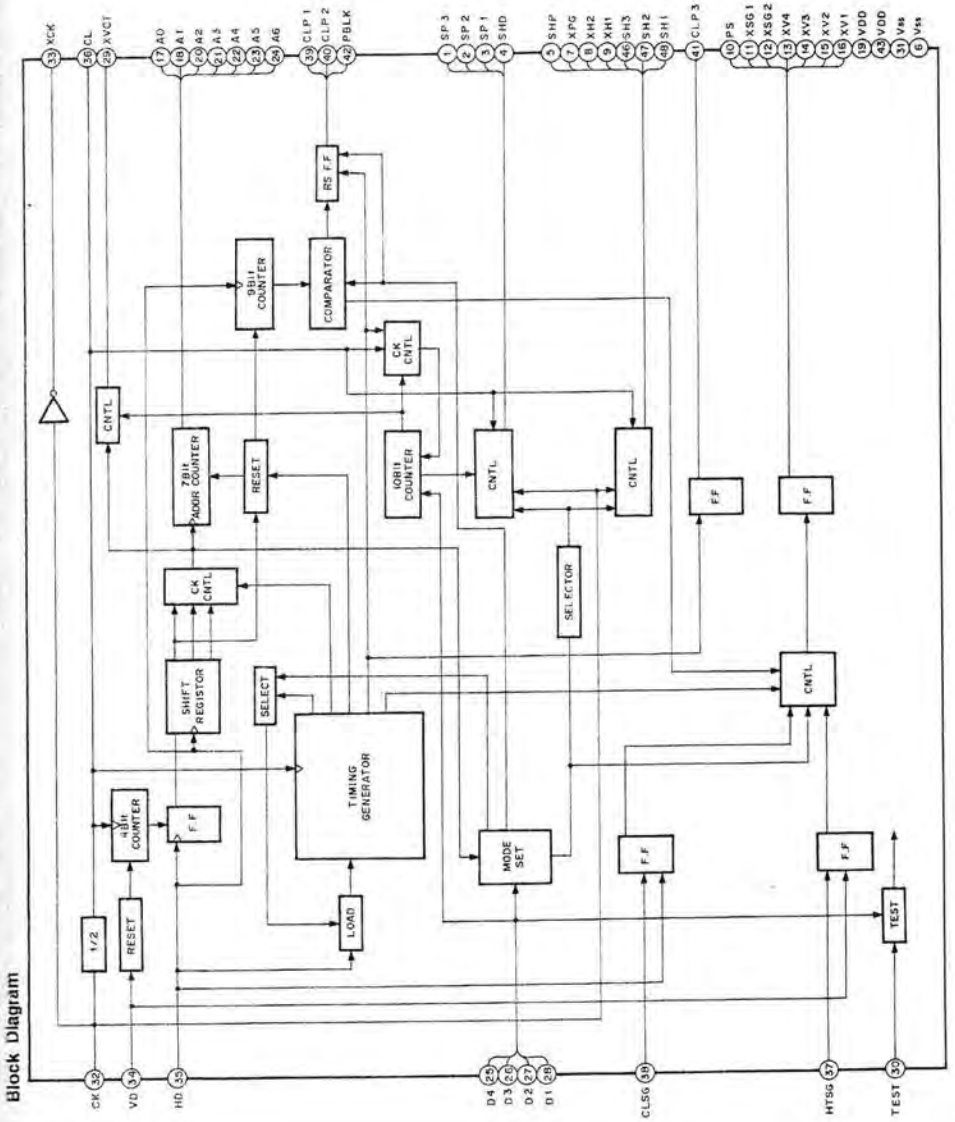
ignal Generator

pin QFP (Plastic)

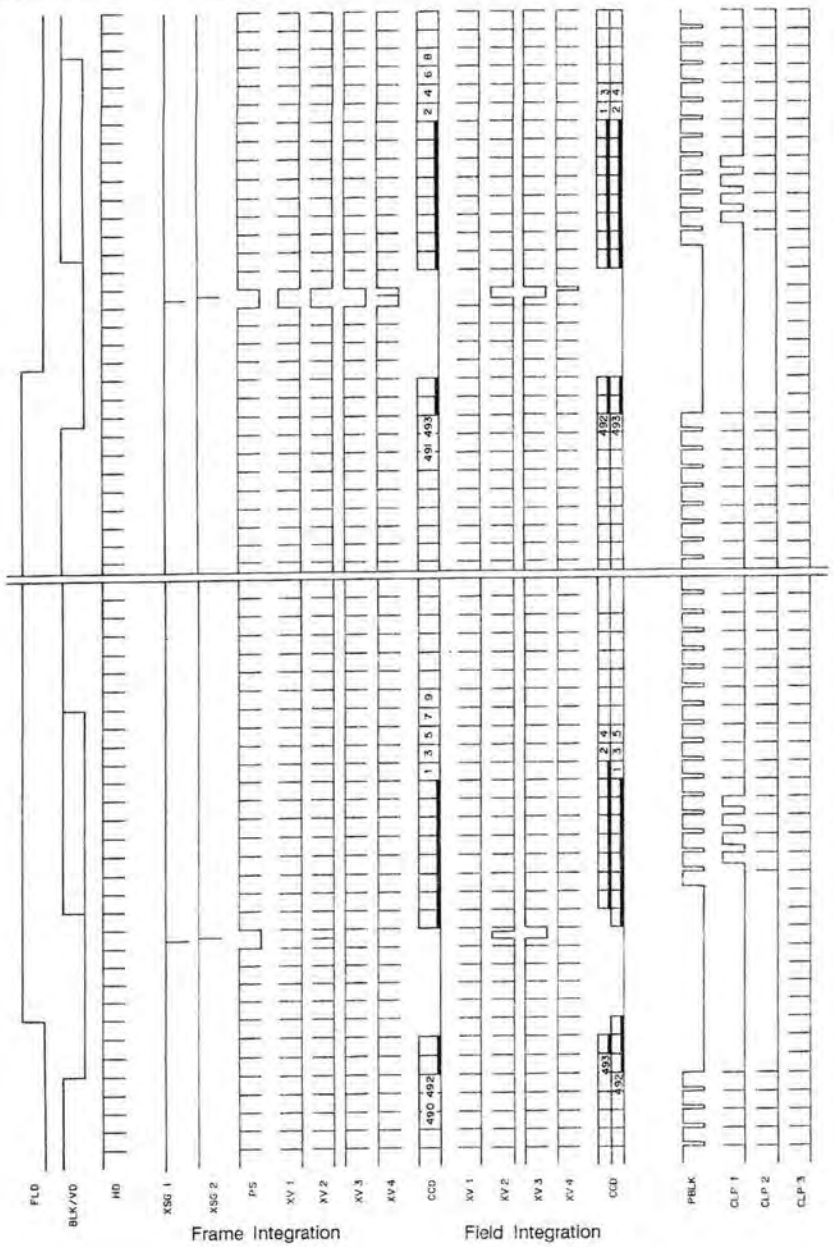
E89Z23-YA



Block Diagram

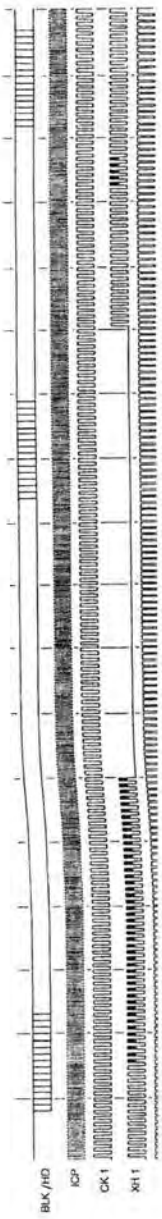


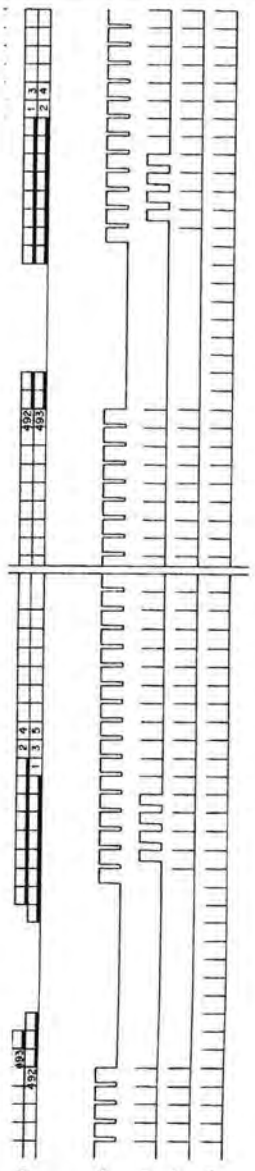
NTSC V Direction






NTSC H Direction

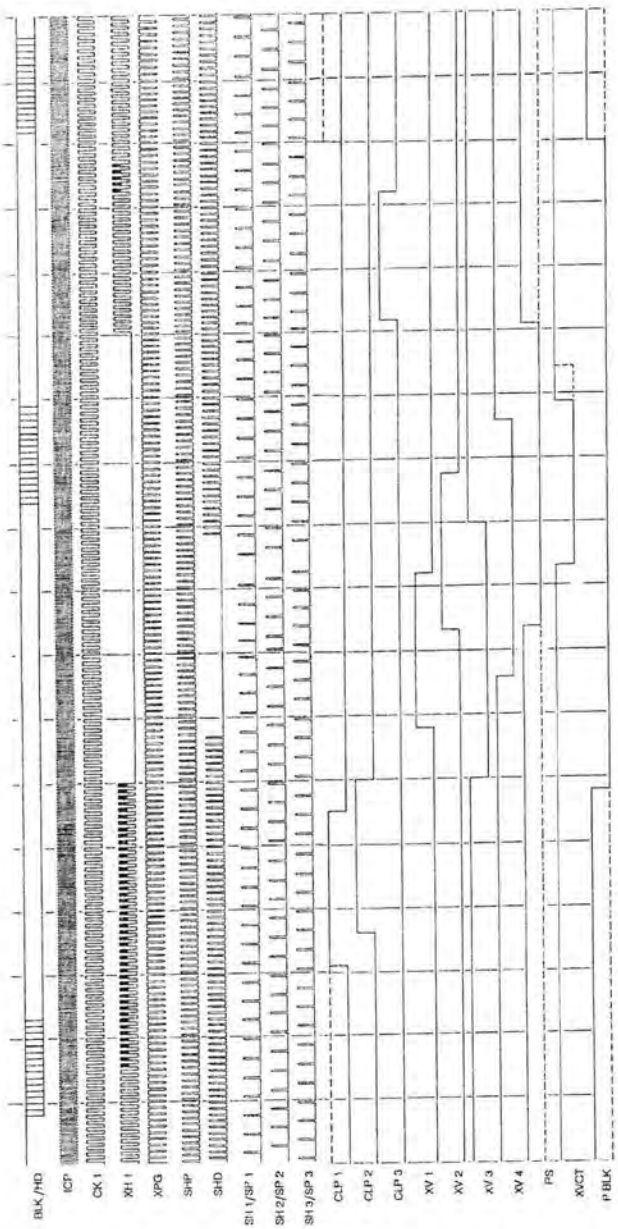









NTSC H Direction



SONY

# CXA1065M

## Vertical clock driver for CCD imagers

### Description

The CXA1065M is a bipolar IC developed to drive the vertical shift register of CCD imagers (ICX022 etc.).

It is composed of seven drivers that can drive large capacitors with wide voltage amplitude. A suppressing function of coupling between phases reduces blooming and smear to make this IC ideal for vertical clock driving of CCD imaging devices.

### Features

- Almost all functions required for vertical clock driving of CCD imager are provided.
- Negative voltage source is not needed.
- Suppressing function of coupling between phases.
- Wide output amplitude — Output voltage amplitude is almost equal to supply voltage.
- Wide operating voltage range — 5.5 to +25 V
- Low power consumption with the built-in power-saving circuit — 116 mW Typ. when the ICX022 equivalent circuit load is driven.

### Structure

Silicon monolithic IC

### Absolute Maximum Ratings (Ta = 25°C)

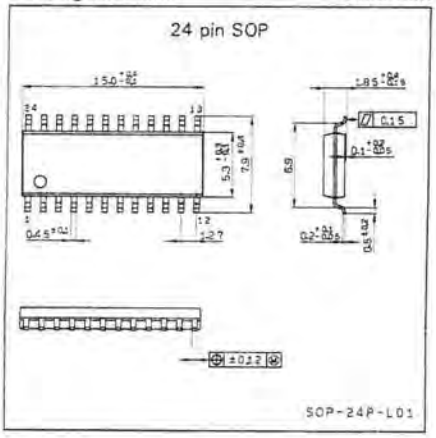
| | | | |
|---|---|---|---|
| • Supply voltage | $V_{cc}1$ | 6 | V |
| | $V_{cc}2$-1 | 27 | V |
| | $V_{cc}2$-2 | 27 | V |
| | $V_{cc}2$-3 | 27 | V |
| | $V_{cc}2$-4 | 27 | V |
| | $V_{cc}3$ | 27 | V |
| | $V_{cc}4$ | 27 | V |
| • Operating temperature | $T_{opr}$ | −20 to +75 | °C |
| • Storage temperature | $T_{stg}$ | −55 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 560 | mW |

### Recommended Operating Conditions

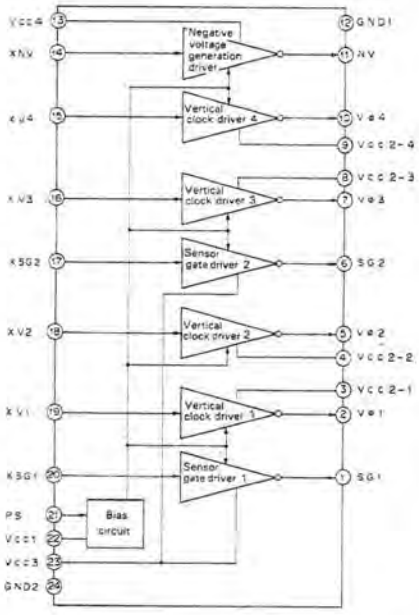
| | |
|---|---|
| $V_{cc}1$ | 4.5 to 5.5 V |
| $V_{cc}2$-1 | 5.5 to 25 V |
| $V_{cc}2$-2 | 5.5 to 25 V |
| $V_{cc}2$-3 | 5.5 to 25 V |
| $V_{cc}2$-4 | 5.5 to 25 V |
| $V_{cc}3$ | 5.5 to 25 V |
| $V_{cc}4$ | 5.5 to 25 V |

### Package Outline

Unit: mm




### Block Diagram



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Pin Configuration (Top Vie


| No. | Symbol | |
|---|---|---|
| 1 | SG1 | Sensor |
| 2 | Vφ1 | Vertical |
| 5 | Vφ2 | Vertical |
| 6 | SG2 | Sensor |
| 7 | Vφ3 | Vertical |
| 10 | Vφ4 | Vertical |
| 11 | NV | Negativ |
| 3 | Vcc2-1 | Vertica |
| 4 | Vcc2-2 | Vertica |
| 8 | Vcc2-3 | Vertica |
| 9 | Vcc2-4 | Vertica |
| 13 | Vcc4 | Negati |
| 23 | Vcc3 | Sensor |
| 12 | GND1 | GND |
| 24 | GND2 | |

# SONY CXB0026AM

## CCD Driver

### Description

CXB0026AM is a special version of CXB0026M with the following improvements:

1) High frequency operation ability.
2) Improved output voltage amplitude (voltage usage ratio).

Other specifications match those of CXB0026M.

### Features

- High frequency operation ability.
- Improved output voltage amplitude.
- TTL compatible input.
- High output current drive.
- 2.0 mW low consumption when input at low level.

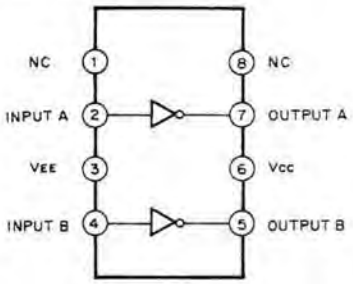
### Structure

Bipolar silicon monolithic IC

### Absolute Maximum Ratings (Ta=25°C)

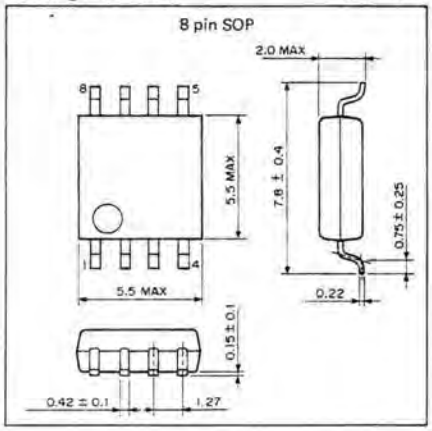
| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC-EE}$ | 22 | V |
| • Input current | $I_I$ | 100 | mA |
| • Input voltage | $V_I$ | $V_{EE}$+5.5 | V |
| • Instant output current | Iopk | ±1.5 | A |
| • Junction temperature | $T_J$ | +150 | °C |
| • Operating temperature | Ta | 0 to 70 | °C |
| • Storage temperature | Tstg | −65 to 150 | °C |
| • Allowable power dissipation (Ta=70°C, PC Board Mount) | $P_D$ | 400 | mW |

### Pin Configuration




### Package Outline

Unit: mm

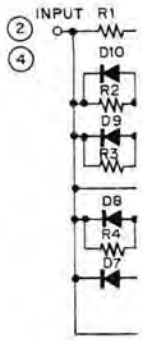



70847A-ST



SONY

### Equivalent Circuit




### Electrical Characteristics

Ta=0 to

| Item |
|---|
| H level input voltage<br>$V_O=V_{EE}$+1.0 Vdc |
| H level input current<br>$V_I-V_{EE}$=2.4 Vdc,<br>$V_O=V_{EE}$+1.0 Vdc |
| L level input<br>$V_O=V_{CC}$−1.0 Vdc |
| L level input current<br>$V_I-V_{EE}$=0 Vdc, $V_O=V_{CC}$−1.0 |
| Output voltage at L level in<br>$V_I-V_{EE}$=0.4 Vdc |
| Output voltage at H level ir<br>$V_I-V_{EE}$=2.4 Vdc |
| Supply current at ON (1 cir<br>$V_{CC}-V_{EE}$=20 Vdc,<br>$V_I-V_{EE}$=2.4 Vdc |
| Supply current at OFF (1 ci<br>$V_{CC}-V_{EE}$=20 Vdc, $V_I-V_{EE}$=C |

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# CXD1141M

## Timing setting for Electronic Shutter (CCD imager)

### Description

The CXD1141M developed for CCD cameras is an LSI that sets the timing of electronic shutters.

### Features

- Compatible with variable shutters (1/60 to 1/10000 sec)
- Compatible with flickerless
- Compatible with NSTC/PAL
- Mode setting compatible with serial/parallel

### Function

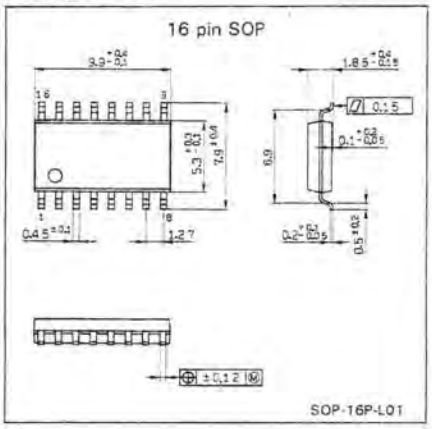
Sets the timing of electronic shutters.

### Structure

Silicon gate CMOS

### Package Outline

Unit: mm




### Absolute Maximum Ratings (Ta = 25°C)

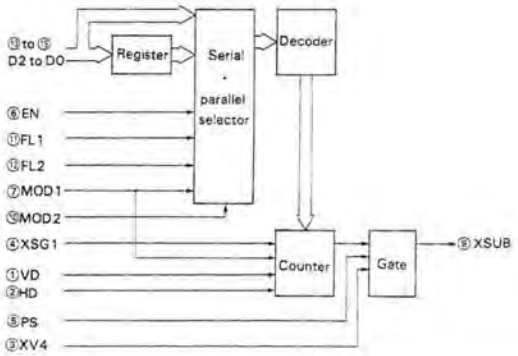
| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | $V_{SS}-0.5^*$ to $+7.0$ | V |
| • Input voltage | $V_{IN}$ | $V_{SS}-0.5^*$ to $V_{DD}+0.5$ | V |
| • Output voltage | $V_O$ | $V_{SS}-0.5^*$ to $V_{DD}+0.5$ | V |
| • Operating temperature | Topr | $-20$ to $+75$ | °C |
| • Storage temperature | Tstg | $-55$ to $+150$ | °C |

* Vss = 0V

### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 4.5 to 5.5 (5.0V Typ.) | V |
| • Operating temperature | Topr | $-20$ to $+75$ | °C |

### Block Diagram




70620-YA



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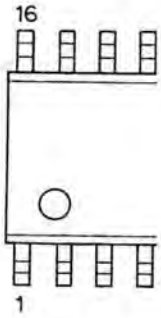
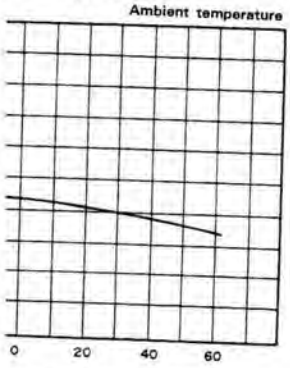
### Pin Configuration and Descript



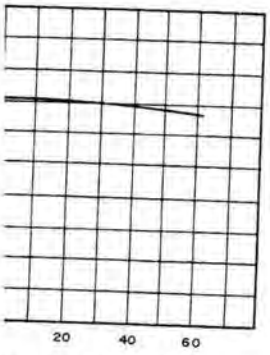

| No. | Symbol | I/O | |
|---|---|---|---|
| 1 | VD | I | Ver |
| 2 | HD | I | Hor |
| 3 | XV4 | I | Ver |
| 4 | XSG1 | I | Ser |
| 5 | PS | I | Pov |
| 6 | EN | I | Ena |
| 7 | MOD1 | I | Mo |
| 8 | Vss | – | GNI |
| 9 | XSUB | O | Elec |
| 10 | MOD2 | I | Mo |
| 11 | FL1 | I | Mo |
| 12 | FL2 | I | Mo |
| 13 | D2 | I | Shu |
| 14 | D1 | I | Shu |
| 15 | D0 | I | Shu |
| 16 | $V_{DD}$ | – | +5 |

ency response vs
Ambient temperature




Ambient temperature (°C)

DC voltage vs Ambient temperature




Ambient temperature (°C)

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# CXA1337Q-Z/R

## Processing system of a CCD Video Cameras

### Description

CXA1337Q-Z/R is designed to extract signals from the CCD output of stripe CCD cameras using signal processing.
This bipolar IC executes correlated double sampling, AGC and color separation.

### Features

- Through the double sampling function it can inhibit low band noise in CCD signals.
- A wide coverage AGC amplifier enhances the camera sensitivity.
- Has output effective for image making such as : Iris adjustment output and High brightness detection output.

### Structure

Bipolar silicon monolithic IC

### Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 10 | V |
| • Operating temperature | Topr | −20 to +75 | °C |
| • Storage temperature | Tstg | −55 to +150 | °C |
| • Allowable power dissipation | PD | 600 | mW (QFP) |
| | | 950* | mW (VQFP) |

*When mounted on the glass epoxy board 40 mm x 40 mm t = 0.8 mm

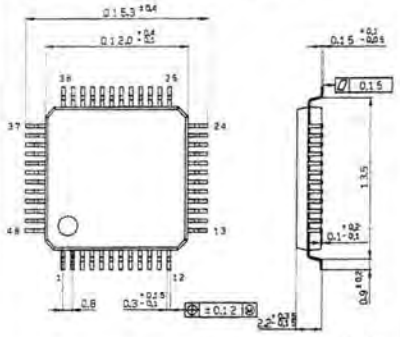
### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 4.75 to 5.25 | V |

### Package Outline

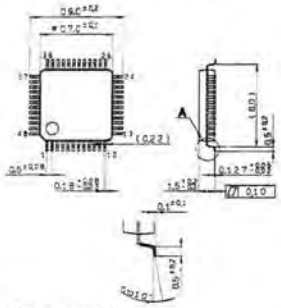
Unit: mm

CXA1337Q-Z 48 pin QFP (Plastic)



QFP-48P-L04

CXA1337R 48 pin VQFP (Plastic)



Detailed diagram of A.
Note) Dimension with * mark shows the status without residual resin.

VQFP-48P-L04

80502-YA

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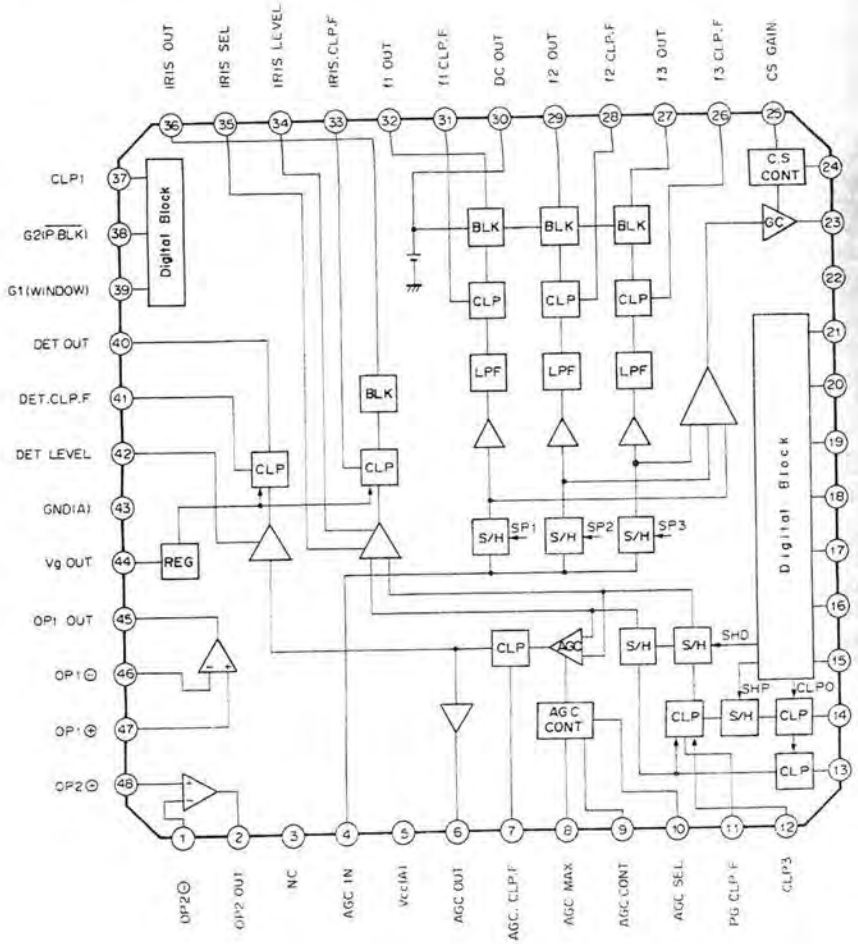
CXA1337

## Pin Description




SONY

Description and Equivalent Circ

| | Symbol | Standard DC |
|---|---|---|
| | OP2⊖ | 0.7 to 3.5V |
| | OP2 OUT | 1 to 4V |
| | N.C. | |
| | AGC IN | 1.8 V |
| | Vcc (A) | 5V |

SONY

# CXA1339Q-Z/R

## CCD Camera Processor

### Description

CXA1339Q-Z and CXA1339R are processor ICs for CCD color cameras. These execute color coding, white balance, γ compensation, HUE control and other signal processing to color separated input signals. γ compensated R-Y, B-Y and YH, YL-YH signals are also shaped.

### Features

- The built-in color coding circuit makes it compatible with both types of CCD color filters, complementary color or primary color.
- Realizes high resolution through the adoption of YL-YH, and YH's Y signal processing.
- Compatible with negative/positive inversion.
- White balance is compatible with both automatic and one push button.
- Control pins have preset function.

### Absolute Maximum Ratings (Ta=25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 7 | V |
| • Operating temperature | Topr | −20 to −75 | °C |
| • Storage temperature | Tstg | −65 to −150 | °C |
| • Allowable power dissipation | Pd | 600 | mW |

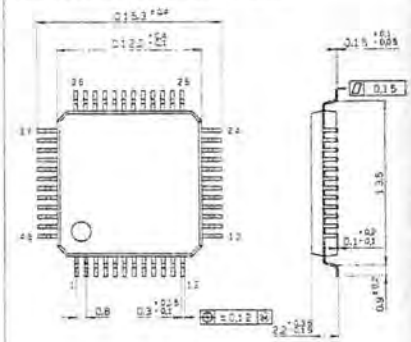
### Recommended Operating Condition

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 5±0.25 | V |

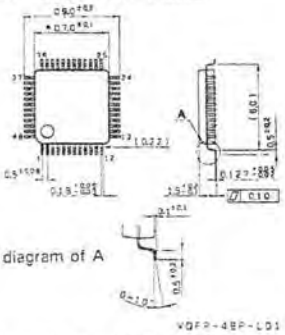
### Package Outline

Unit: mm

CXA1339Q-Z 48 pin QFP (Plastic)



CXA1339R 48 pin VQFP (Plastic)



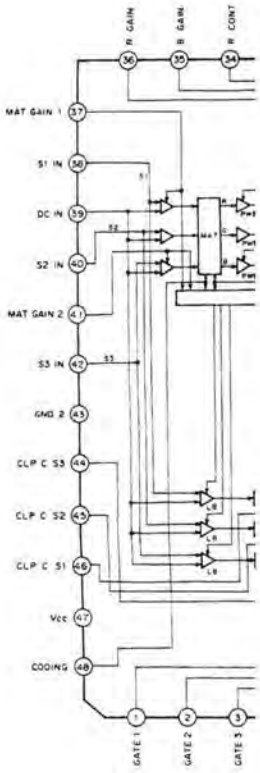
Detailed diagram of A



**Note)** Dimensions marked with * does not include residual resin.

80706-ST

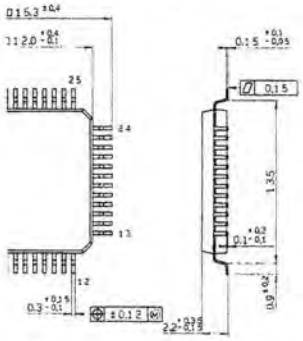
### Block Diagram



# 1339Q-Z/R

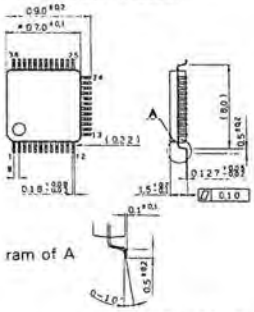
utline Unit: mm

48 pin QFP (Plastic)



QFP-48P-L0

48 pin VQFP (Plastic)



ram of A

VQFP-48P-L01

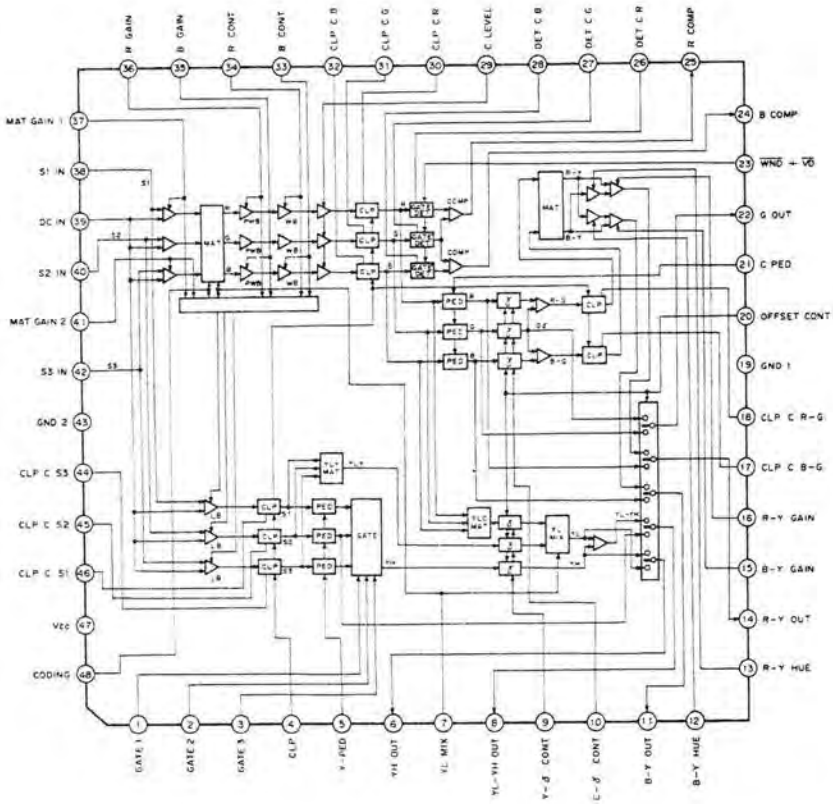
sions marked with *

not include residual resin.

80706-ST



## Block Diagram



SONY

# CXA1270N

## IC for Vertical Direction Outline Compensation

**Description**

CXA1270N is a bipolar IC developed for vertical outline compensation of video camera. It contains all the required functions for vertical outline compensation in a single chip. Also, being a small package, this IC is most suitable for the use in video camera.

20pin VSOP (Plastic)

**Features**

- Low power consumption
- Usable both in 2H type and 1H type.
- Executes low level noise clip.
- Controlable output level.

**Structure**

Bipolar silicon monolithic IC

**Applications**

Video camera

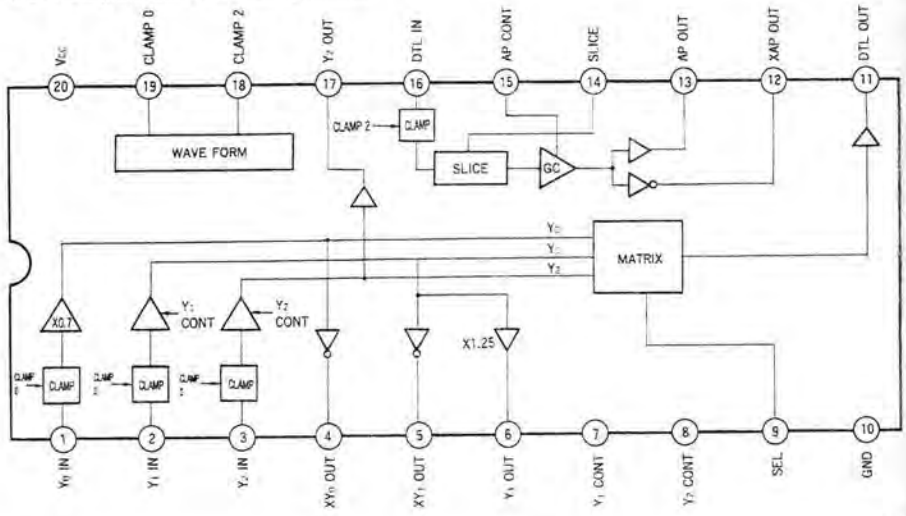
**Absolute Maximum Ratings (Ta=25°C)**

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC}$ | 10 | V |
| • Storage temperature | $T_{stg}$ | −55 to +150 | °C |
| • Operating temperature | $T_{opr}$ | −20 to +75 | °C |
| • Allowable power dissipation | $P_D$ | 375 | mW |

**Recommended Operating Condition**

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC}$ | 4.75 to 5.25 | V |

**Block Diagram and Pin Configuration**




E89633-4BP



SONY

**Pin Description and Equivalent Circ**

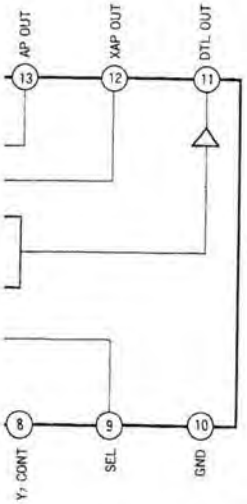
| Pin No. | Symbol | Pin voltage | |
|---|---|---|---|
| 1 | $V_0$ IN | 2.8V (Black level) | |
| 2 | $Y_1$ IN | 2.8V (Black level) | ①② |
| 3 | $Y_2$ IN | 2.8V (Black level) | ③ |
| 4 | $XY_0$ OUT | 2.1V (Black level) | |
| 5 | $XY_1$ OUT | 2.0V (Black level) | |
| 6 | $Y_1$ OUT | 2.4V (Black level) | |
| 7 | $Y_1$ CONT | 1.5V to 3.5V (Outside) | |
| 8 | $Y_2$ CONT | 1.5V to 3.5V (Outside) | ⑦⑧ |
| 9 | SEL | Low 0V<br>High 5V | ⑨ |
| 10 | GND | | |
| 11 | DTL OUT | 2.9V | |

# CXA1270N

tion

pin VSOP (Plastic)

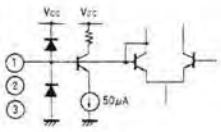
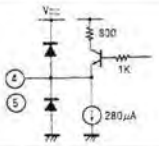
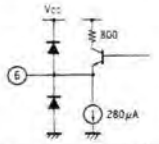
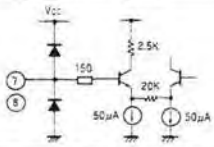
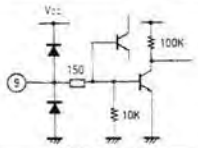
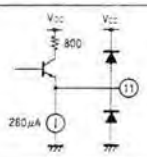
monolithic IC




E89631-HP



**Pin Description and Equivalent Circuit** $V_{CC}$=5V

| Pin No. | Symbol | Pin voltage | Equivalent Circuit | Description |
|---|---|---|---|---|
| 1 | $V_0$ IN | 2.8V (Black level) |  | Y signal input pin (500Vp-p [Typ.] ) |
| 2 | $Y_1$ IN | 2.8V (Black level) | | Y signal input pin (1H delay) (150mVp-p [Typ.] ) |
| 3 | $Y_2$ IN | 2.8V (Black level) | | Y signal input pin (2H delay) (150mVp-p [Typ.] ) |
| 4 | $XY_0$ OUT | 2.1V (Black level) |  | $Y_0$ $A_{mp}$ inverse output pin |
| 5 | $XY_1$ OUT | 2.0V (Black level) | | $Y_1$ $A_{mp}$ inverse output pin |
| 6 | $Y_1$ OUT | 2.4V (Black level) |  | $Y_1$ $A_{mp}$ output pin |
| 7 | $Y_1$ CONT | 1.5V to 3.5V (Outside) |  | $Y_1$ $A_{mp}$ gain control pin |
| 8 | $Y_2$ CONT | 1.5V to 3.5V (Outside) | | $Y_2$ $A_{mp}$ gain control pin |
| 9 | SEL | Low 0V<br>High 5V |  | Switching pin of 2H mode and 1H mode<br>High (5V)=2H DL mode<br>Low (0V)=1H DL mode |
| 10 | GND | | | GND pin |
| 11 | DTL OUT | 2.9V |  | DETAIL signal output |

SONY

# CXA1072Q-Z/R

## Camera Signal Processing

### Description

CXA1072Q-Z and CXA1072R are encoder ICs for CCD color cameras.
Luminance and color difference signals are input to be output as composite video signals.
Combined use with system for CCD color cameras.

### Features

- Built-in auto carrier balance (carrier balance adjustment unnecessary).
- Compatible with both NTSC/PAL
- Compatible with Negative/Positive.
- Low consumption (200 mW) (150 mW in B/W mode)
- Low noise

### Structure

Bipolar silicon monolithic IC.

### Application

CCD color camera

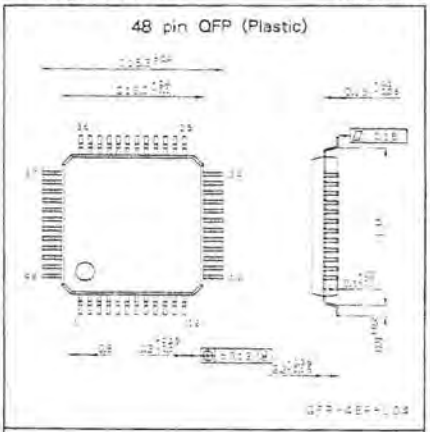
### Function

- Set-up level control
- White clip level control
- White fader/black fader
- View finder output
- Character signal (superimpose)
- Sub carrier modulation
- Burst level control
- PAL mode
- Sub carrier output
- Sharpness level control
- Negative mode
- Return video input
- Auto carrier balance
- HUE control
- Sync level control
- Chroma suppress Y, chroma suppress AGC

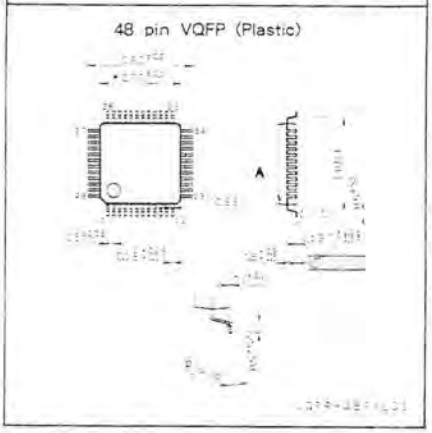
### Package Outline

Unit: mm

48 pin QFP (Plastic)



48 pin VQFP (Plastic)



### Absolute Maximum Ratings (Ta=25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 7 | V |
| • Operating temperature | Topr | −20 to +75 | °C |
| • Storage temperature | Tstg | −55 to +150 | °C |
| • Allowable power dissipation | PD | 600 | mW |

### Recommended Operating Condition

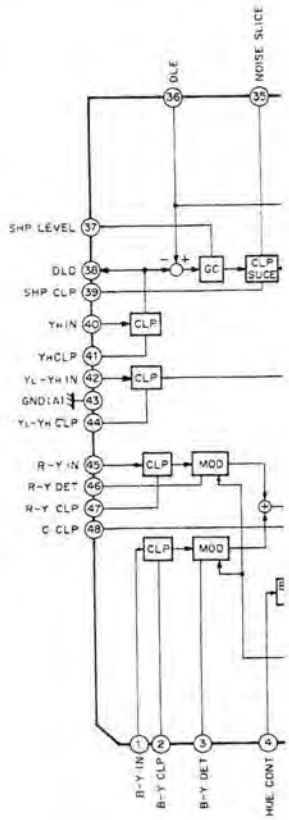
| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 4.75 to 5.25 | V |

70813A-ST



SONY

### Block Diagram and Pin Confi



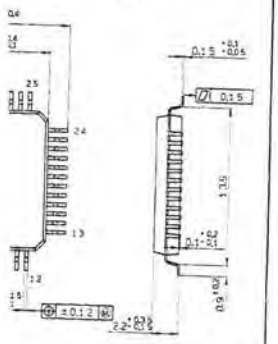

### Abbreviations

| | |
|---|---|
| CLP | Clamp |
| DET | Detecter |
| CONT | Control |
| BF | Burst Frag |
| BLK | Blanking |
| N/P | Nega/Posi |
| LALT | Line Alternate |
| CSY | Chroma Suppres Y |

72Q-Z/R

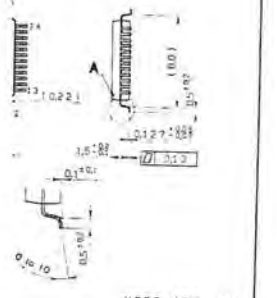
ıe Unit: mm

pin QFP (Plastic)



QFP-48P-L04

VQFP (Plastic)



VQFP-48P-L01

a=25°C)

| | | |
|---|---|---|
| cc | 7 | V |
| opr | −20 to +75 | °C |
| stg | −55 to +150 | °C |
| ) | 600 | mW |

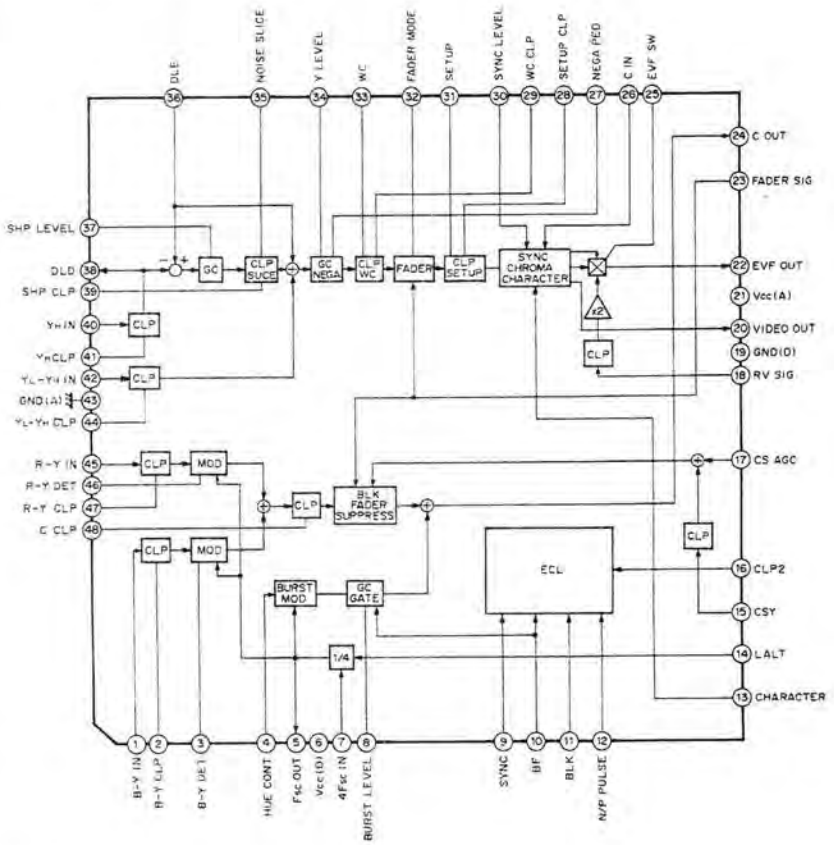
ition

| | | |
|---|---|---|
| :c | 4.75 to 5.25 | V |

70813A-ST



## Block Diagram and Pin Configuration




## Abbreviations

| | | | |
|---|---|---|---|
| CLP | Clamp | RV | Return Video |
| DET | Detecter | EVF | Electric View Finder |
| CONT | Control | CIN | Chroma Input |
| BF | Burst Frag | PED | Pedestal |
| BLK | Blanking | WC | White Clip |
| N/P | Nega/Posi | DLD | Delay Line Drive |
| LALT | Line Alternate | DLE | Delay Line End |
| CSY | Chroma Suppres Y | SHP | Sharpness |

APPENDIX KKK

PROCEEDINGS REPRINT

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*Reprinted from*

# Camera and Input Scanner Systems

27–28 February 1991
San Jose, California


Volume 1448

# A High-Performance Digital Color Video Camera

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Image Acquisition Products Division, Eastman Kodak Company, Rochester, New York 14650-2015

## ABSTRACT

Typical one-chip color cameras use analog video processing circuits. An improved digital camera architecture has been developed using a dual-slope A/D conversion technique, and two full custom CMOS digital video processing ICs, the "CFA processor" and the "RGB post-processor". The system uses a 768 x 484 active element interline transfer CCD with a new "field-staggered 3G" color filter pattern and a "lenslet" overlay, which doubles the sensitivity of the camera. The digital camera design offers improved image quality, reliability, and manufacturability, while meeting aggressive size, power, and cost constraints. The CFA processor digital VLSI chip includes color filter interpolation processing, an optical black clamp, defect correction, white balance, and gain control. The RGB post-processor digital IC includes a color correction matrix, gamma correction, two-dimensional edge-enhancement, and circuits to control the black balance, lens aperture, and focus.

## 1. INTRODUCTION

A significant amount of signal processing is needed to obtain high-quality color video images from a one-chip color CCD sensor. A wide variety of color filter array (CFA) patterns can be used to provide color images.[1] In current single-sensor color cameras and camcorders, the video signal processing is accomplished with analog circuits.[2-5] The constraints of analog video processing places practical limitations on the sophistication of the image processing which can be implemented in such systems. This constrains the choice of CFA patterns that can be used, and compromises image quality.

Digital processing offers many system advantages, but can result in large, expensive, and power-hungry cameras, unless digital VLSI techniques are used. Digital processing has been employed in a commercially available three-sensor camera,[6] and numerous digital designs for two-sensor[7] and single-sensor[8-10] cameras have been described in the literature. The first operational one-chip color CCD imaging system using full custom VLSI digital processors has been reported previously.[11,12] This paper describes the application of these VLSI video processing ICs in a higher performance camera system, using a newly developed CCD image sensor with an improved color filter array pattern, and a dual-slope A/D conversion technique.

Figure 1 shows a simplified block diagram of the digital color camera. The camera lens focuses the image onto the color CCD image sensor. The sensor output signal is digitized at a 14.318 MHz sample rate. The digitized signal from the CCD sensor is processed by two full-custom CMOS ICs, the "CFA Processor", and the "RGB Post-Processor". The processing is pipelined, and operates at the same pixel rate as the image sensor, so that a framestore is not required. The ICs have been designed to operate with a variety of image sensors and color filter options. To minimize the chip areas, the signal processing has been carefully designed to eliminate the need for multipliers and to reduce the amount of line delay memory required.

## 2. IMAGE SENSOR

The sensor is a high-performance silicon charge-coupled device (CCD) with an interline transfer architecture and 2:1 interlaced readout. The device is built with an advanced true two-phase, two-polysilicon, NMOS CCD technology. The p+npn- photodetector elements operate in a fully depleted mode. Therefore, charge from the photodiodes is completely transferred to the vertical CCDs (VCCD), eliminating the image lag seen with conventional np photodiodes. A p-well vertical overflow drain structure allows antiblooming protection. A close proximity refractory metal lightshield greatly reduces image smear. The active area is 8.9 mm (H) x 6.6 mm (V), and the total chip size is 9.9 mm (H) x 7.7 mm (V).

0-8194-0547-7/91/$4.00

Figure 2 is a functional block diagram of the sensor, which consists of 371,712 active photodiodes, 768 vertical (parallel) CCD shift registers, one horizontal (serial) CCD shift register and one output amplifier. Both registers incorporate two-level polysilicon and true two-phase buried channel CCD technology,[13] as shown in Fig. 3. The pixels are arranged in a 768 (H) x 484 (V) array in which an additional 12 columns and 5 rows of light shielded pixels are added as a dark reference. The pixel architecture is shown in Fig. 4. An image is acquired when incident light, in the form of photons, falls on the array of photodiodes and creates electron-hole pairs within the silicon substrate. This charge is collected locally by the formation of potential wells created at each photodiode site. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and nonlinearly dependent on wavelength. When the photodiode charge capacity is reached, excess electrons are discharged to the substrate, to prevent blooming.

The accumulated or integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transported from the photodiodes to the vertical shift registers by applying a large positive voltage to one of the vertical clocks. This reads out every other row of photodiodes, thus transferring one of the two interlaced fields into the vertical CCD registers. The charge is then transported from the vertical CCD registers in a line-by-line or parallel fashion to the horizontal CCD register. Finally, the horizontal CCD register transports this 'line' of charge in a pixel-by-pixel or serial fashion to the output amplifier. The remaining field is clocked out in a similar fashion by applying a positive voltage to the other vertical clock phase, thus completing interlaced readout of one frame. Both the horizontal and vertical shift registers use traditional complementary clocking for charge transport. Transfer to the horizontal CCD begins when ØV2 is brought high and ØV1 is brought low, causing charge from the ØV1 and ØV2 gates to transfer a line of charge into the horizontal shift register. The sequence ends when ØV2 is brought low while the horizontal CCD reads out the first line of charge.

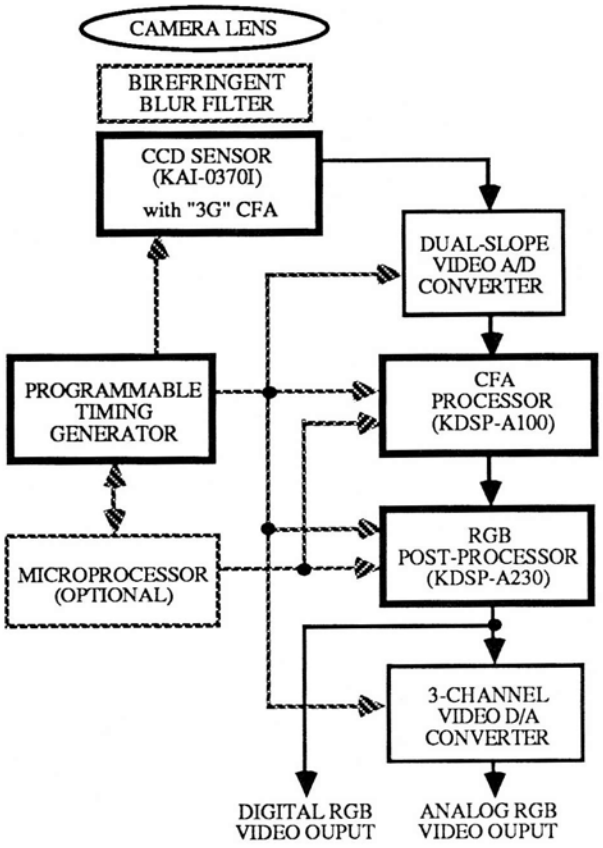


Fig. 1 Digital Camera Block Diagram

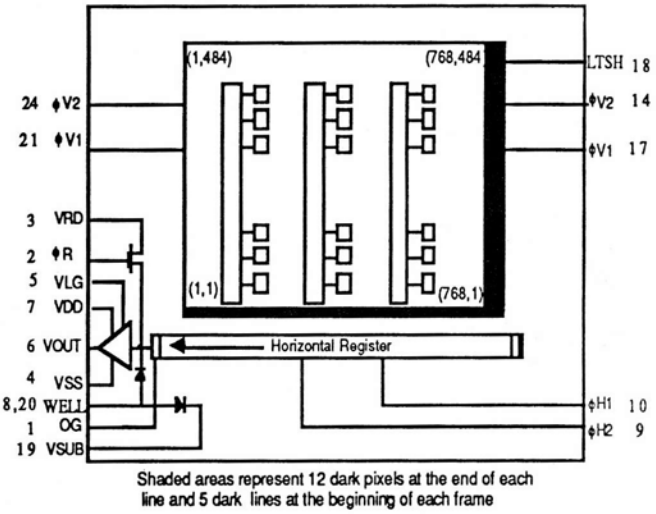


Fig. 2 CCD Sensor Block Diagram

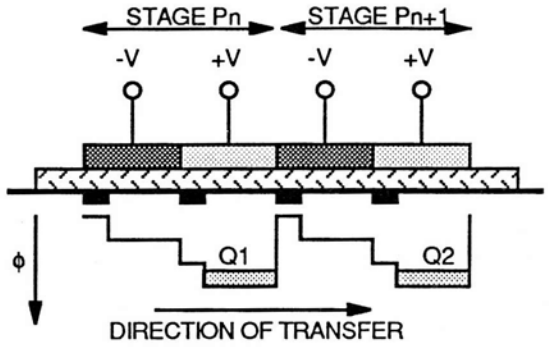


Fig. 3 True Two-Phase CCD Cross Section

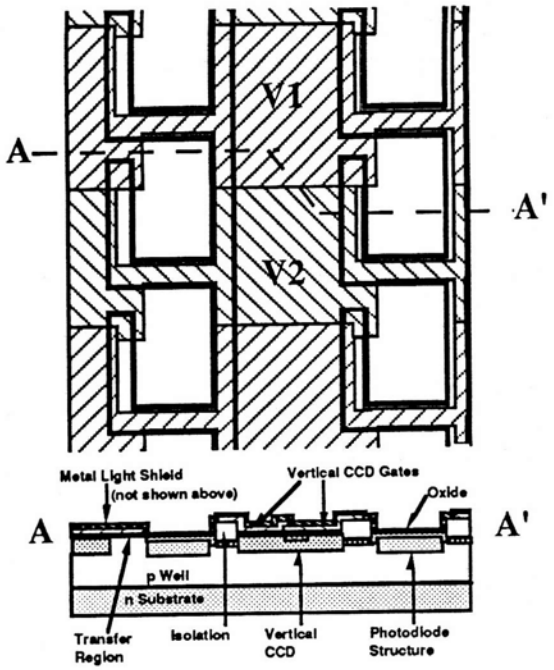


Fig. 4 CCD Pixel Architecture

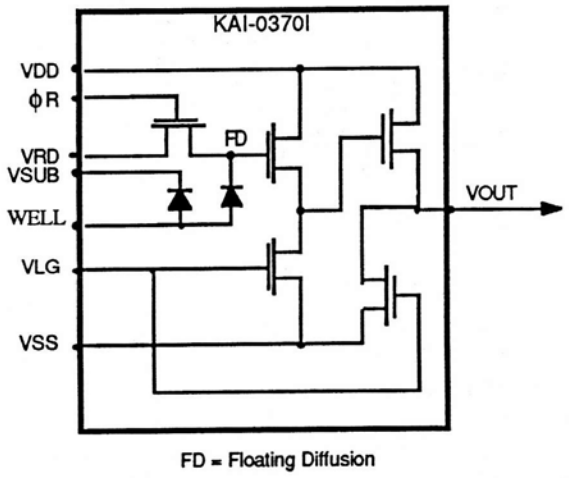


Fig. 5 CCD Output Schematic

A schematic of the output structure is shown in Fig. 5. On each falling edge of ØH2, a charge packet is dumped over the output gate (OG in Fig. 2) onto the output node or floating diffusion (FD in Fig. 5). The potential of the floating diffusion varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression

$$\Delta V_{fd} = \Delta Q / C_{fd}, \qquad (1)$$

where $\Delta V_{fd}$ is the change of the floating diffusion voltage, $\Delta Q$ is the charge transferred onto the floating diffusion, and $C_{fd}$ is the capacitance of the floating diffusion. The translation from electrons to voltage is called the output sensitivity or charge-to-voltage conversion. After the charge has been sensed off-chip, the reset clock (ØR) removes the charge from the floating diffusion via the reset drain (VRD). This in turn returns the floating diffusion potential to the reference level determined by the reset drain voltage. A two-stage source-follower amplifier is used to provide the video output signal (VOUT).

### 3. COLOR FILTER ARRAY

The image sensor is overlayed with the new "field-staggered 3G" color mosaic filter pattern shown in Fig. 6. The CFA contains 75% green (G) photosites and 25% red (R) and blue (B) photosites. By devoting most of the photosites to luminance, the scene is sampled in a manner compatible with the human visual system, which is more sensitive to high spatial frequency luminance variations than to high spatial frequency chrominance variations[14]. When the proper image processing is used to reconstruct RGB values for each photosite,[15,16] the "3G" CFA pattern can provide images that are sharper, yet have reduced color aliasing, compared to images from other stripe or mosiac CFA patterns. Because of the complexity of the required reconstruction processing, digital signal processing techniques are more appropriate than analog processing circuits. A birefringent blur filter[17,18] helps to eliminate aliasing and provides color co-incidence between the chrominance samples and the adjacent luminance samples.

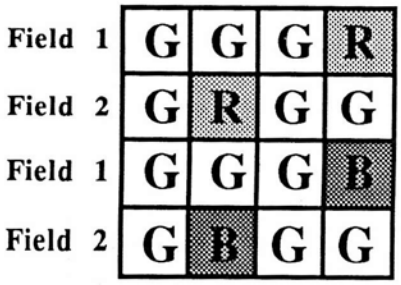


Fig. 6 Field Staggered 3G CFA

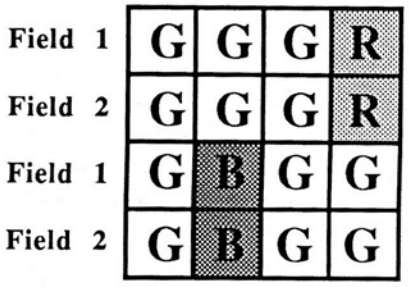


Fig. 7 Line Staggered 3G CFA

The newly developed "field-staggered 3G" CFA is an improvement on the "line-staggered 3G" CFA shown in Fig. 7, which was used in earlier cameras.[12] In interlaced video applications, every second line of the CCD sensor is read out during field 1, while the remaining lines are read out during field 2. The color filter pattern must be designed to operate properly with this interlaced readout. If, for example, red photosites were located only on every second (odd) line of the sensor, while blue photosites were located only on the remaining (even) lines, red would then be sampled only during field 1, and blue would be sampled only during field 2. The resulting image would exhibit a severe 30 Hz yellow-cyan hue flicker, which would produce an unacceptable level of visual discomfort,[19] unless a chrominance field store were used.

In order to accommodate interlaced readout, the "line-staggered 3G" CFA in Fig. 7 is arranged so that each line is repeated twice, thus the field 1 and field 2 sampling is identical. This means that the red and blue sampling occurs only in every fourth column of pixels in the horizontal direction. The locations at which red and blue are sampled are offset in the horizontal direction by 2 pixels. The "field-staggered 3G" CFA in Fig. 6 is arranged so that the lines of field 2 are shifted horizontally by two pixels relative to the lines of field 1. This allows red and blue to be sampled at every second column of pixels in the horizontal direction. This creates a more checkerboard-like chrominance sampling pattern that provides improved chrominance resolution in the horizontal direction.[20] Because the two digital processing ICs were designed with flexibility in mind, the new "field-staggered 3G" CFA can be accommodated with only a minor change in the external timing signals that control the CFA processor IC.

The image sensor includes a lenticular array, fabricated on top of the CFA, which is integrated above the photosensors.[21] These "lenslets" are an array of convex lenses formed above each photosite, as shown in Fig. 8. The lenslets focus the light away from the opaque light shields and into the center of the photodiodes. This increases the sensitivity by a factor of more than two, since most of the photons which would normally hit the light shields and be "wasted" are now collected by the photodiodes. This also slightly decreases aliasing and reduces smear. A photomicrograph of the pillow-shaped lenses which form the lenslet overlay are shown in Photo 1.

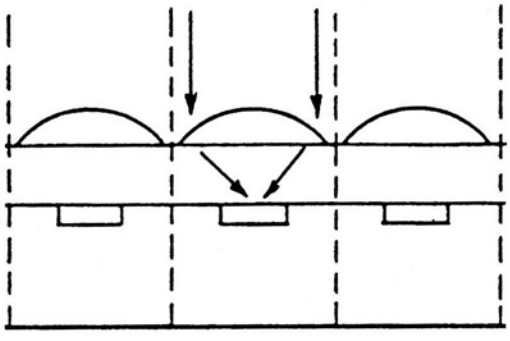

Fig. 8 Lenslet Structure

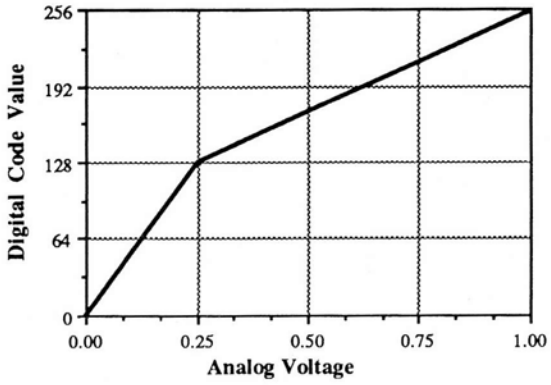


Fig. 9 Dual-Slope A/D Characteristic

## 4. A/D CONVERSION

The sensor output is processed by a conventional clamp / sample-and-hold circuit that implements correlated double sampling.[22] This circuit forms a continuous analog video signal, while eliminating the noise associated with resetting the CCD floating diffusion output and suppressing low frequency noise such as the 1/f noise from the on-chip source follower amplifiers. The processed sensor output signal is digitized with a commercially available 8 bit parallel "flash" A/D converter,[23] which allows access to the mid-point of the resistor ladder. The voltage on the mid-point ladder pin has been set to provide the conversion characteristic shown in Fig. 9. This technique provides the equivalent of a 10-bit digital conversion at low signal levels, and a 7-bit digital conversion at high signal levels. The dual-slope quantizer is designed to reduce the quantization distortion in the gamma-corrected output signal relative to the quantizaton distortion using a linear 8-bit quanitizer. The digitized sensor signal is input to the "CFA processor".

## 5. CFA PROCESSOR IC

A simplified block diagram of the functions performed by the CFA processor chip[24] is shown in Fig. 10. The first on-chip operation is an optical black reference clamp. The dark current of CCD image sensors is very dependent on the operating temperature. The purpose of the black reference clamp is to subtract off the average dark current value of the sensor. The digital implementation is more stable and less expensive than an analog implementation, but slightly reduces the useful operating range of the A/D converter. The sensor defect concealment allows defective photosites to be concealed, by substituting the values of the previous horizontally adjacent pixels of the same color. Next, the chip incorporates a novel architecture, which interpolates the missing green (luminance) pixels using a linear quantization space finite impulse response (FIR) filter, and then reconstructs the missing red and blue pixels by interpolating the chrominance to luminance ratios in a logarithmic quantization space. This technique greatly reduces color edge artifacts, compared to linearly interpolating the red and blue values without utilizing the green signal.[25]

A more detailed diagram of the CFA processor implementation is shown in Fig. 11. The digitized pixel inputs (PIXIN(10)) from the A/D converter can be either a linearly quantized signal with a maximum of 10 bits, or a nonlinearly quantized signal with a maximum of 8 bits. The FORCE(2) control lines allow the input to be clipped to white or black values, in order to handle A/D overflow conditions or provide input image blanking. The chip includes an 8 bit-to-10 bit ROM look-up table (LUT), which is selected when the nonlinear A/D is used, and can be mask programmed to convert the 8-bit dual-slope characteristic shown in Fig. 9 to a 10-bit linear quantization chracteristic. The black reference clamp works by summing 512 pixel values from "black" photosites located in a line at the top of the image, using a hard-wired shift to obtain the average, and subtracting the average value from the rest of the image pixel values. Defective pixels are concealed using multiplexers controlled by the DEF(2) signals to substitute values from the appropriate pixels delays.

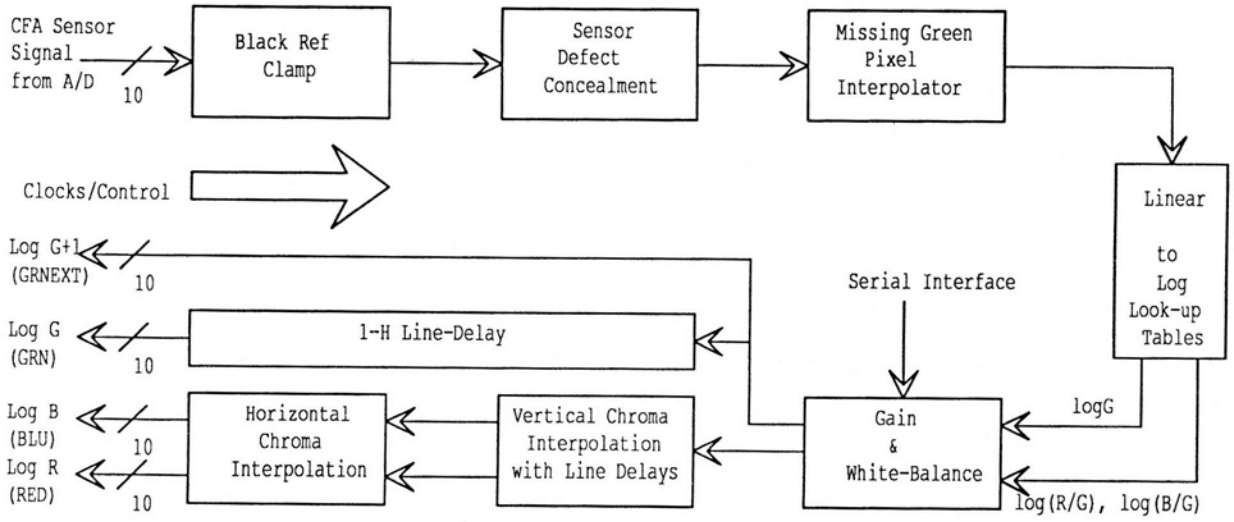


**Fig. 10 CFA Processor Functions**

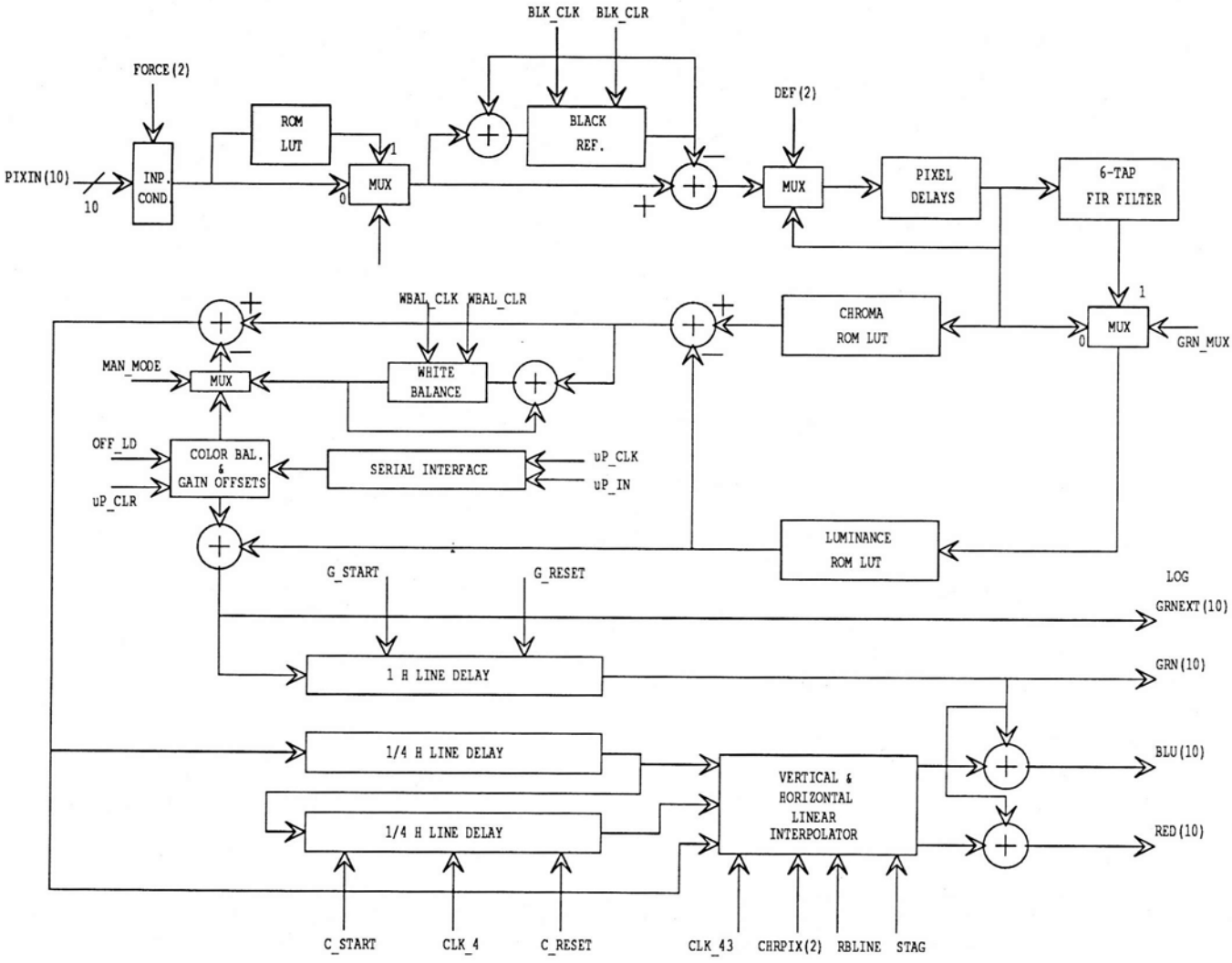


**Fig. 11 CFA Processor Implementation**

Values for the green signal at spatial locations corresponding to red and blue photosites are calculated using a 7-tap FIR interpolation filter. The filter impulse response is given by

$$y = \sum_{i=-3}^{+3} a_i x_i \qquad (2)$$

where $a_i$ are the co-efficients and $x_i$ are the "known" horizontally adjacent green pixel values centered about the "missing green" (red or blue) pixel locations. The filter is designed so that the point spread function of the missing green elements equals the point spread function of the green photosites.[16] The center ($a_0$) co-efficient equals zero and the filter is symmetric, so only three fixed co-efficient multiplications are required. The multiplications are implemented using hardwired shift and add or shift and subtract circuits, so that the entire filter requires only ten adders, an enormous area savings compared to multipliers.

The combination of the optical pre-filter and the missing green interpolation filter provides nearly perfect color co-incidence between the red or blue value and the interpolated green value at the same red or blue photosite. This allows the blue-to-green and red-to-green color ratios to be accurately determined. If the coarsely sampled red and blue records were independently interpolated, very disturbing false color artifacts would occur at luminance edge transitions. However, by linearly interpolating the blue-to-green and red-to-green color ratios, the colored edge artifacts can be almost completely eliminated.

The data is demultiplexed into green and line sequential red/blue channels and transformed using on-chip luminance and chroma ROMs programmed to provide logarithmic curveshapes. The blue-to-green and red-to-green ratios are formed by subtracting the log space signals, since the difference of two logarithmically quanitized signals equals the log of the ratio of the signals. The CFA processor chip includes a gain control circuit and a white balance circuit, which can operate automatically or under microprocessor control. These operate by adding log space offset values, rather than by using multipliers. The gain control works by adding or subtracting a value from the log green signal. This "gain offset value" is input to the CFA processor via a simple two-wire serial interface from a microprocessor, using data line uP_IN and clock line uP_CLK. Two "color balance offset values", which are added to the log R/G and log B/G values to obtain proper white balance, can also be input via the serial interface. Alternatively, proper white balance can be obtained using the on-chip white balance circuit, which averages the log R/G and log B/G signals when signaled by the WBAL_CLK and WBAL_CLR lines as the camera images a white card, and then subtracts the average values from the normal image.

The log color difference signals are linearly interpolated first in the vertical direction using on-chip line delays, and then in the horizontal direction using hardwired shift and add circuits. The linear interpolation circuits use a polyphase structure based on the commutative model.[26] Implementing the vertical interpolation before the horizontal interpolation reduces the size of the two red/blue line delays by a factor of four. The linearly interpolated log R/G and the log B/G signals are summed with the delayed log G signal to provide log R and log B values for each pixel of the array. These red and blue signals contain low spatial frequency color information and high spatial frequency luminance detail information derived from the green channel. The undelayed log G signal is also output and is used in the RGB post-processor edge enhancement circuit.

A photomicrograph of the CFA processor is shown in Photo 2. The chip is 10 mm x 10 mm with 94,000 transistors, and dissipates 330 mW at 5 volts. Both the CFA processor and the RGB post-processor chips were designed and fabricated in-house using a 2-micron CMOS single-poly, double metal process, and are packaged in standard 84-pin packages. The largest circuit block on the CFA processor is the green 1-H line delay, which is required to spatially align the green pixel data with the vertically interpolated red and blue data.

## 6. RGB POST-PROCESSOR IC

The logarithmically quantized 10-bit RGB outputs of the CFA processor are connected to the inputs of the second VLSI chip, the "RGB post-processor".[27] A simplified block diagram of the functions performed by this chip are shown in Fig. 12, and a more detailed diagram of the chip architecture is shown in Fig. 13. The logarithmically quantized RGB data from the CFA processor is first converted to linearly quantized data by three ROM look-up tables, prior to black level correction and matrixing. The average picture levels (APLs) for red, green, and blue are computed by three accumulators, and output to a microprocessor via a two-wire serial output interface, using data output line uP_OUT and clock line uP_OUT_CLK. The microprocessor can input RGB black level offset values, via data input line uP_IN and clock line uP_IN_CLK, to correct for lens flare or to adjust for user preferences.

A mask-programmable 3 x 3 color correction matrix is used to improve the color reproduction by correcting the camera responsivities properly for the display phosphor chomaticities. Figure 14 shows the measured color sensitivities of the CCD camera prior to matrixing. Notice that the CCD responsivity at any wavelength must always be positive, since a negative response to light is physically impossible. Figure 15 shows the optimum camera sensitivities for CRT displays incorporating SMPTE C phosphors with a D65 white point.[28]

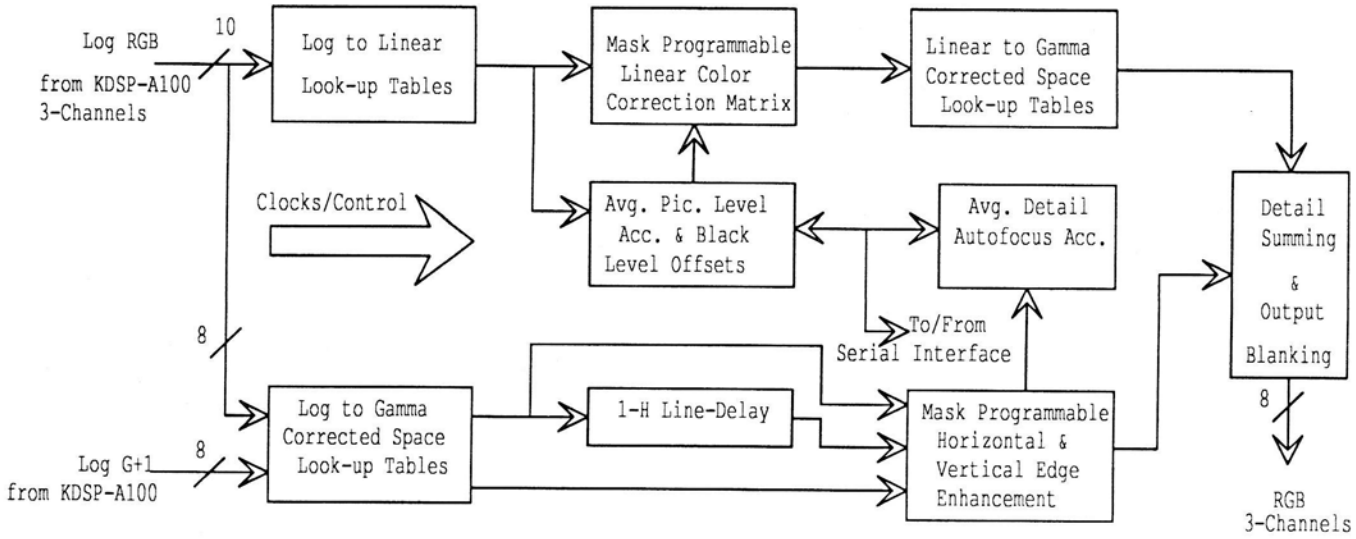


**Fig. 12 RGB Post-Processor Functions**

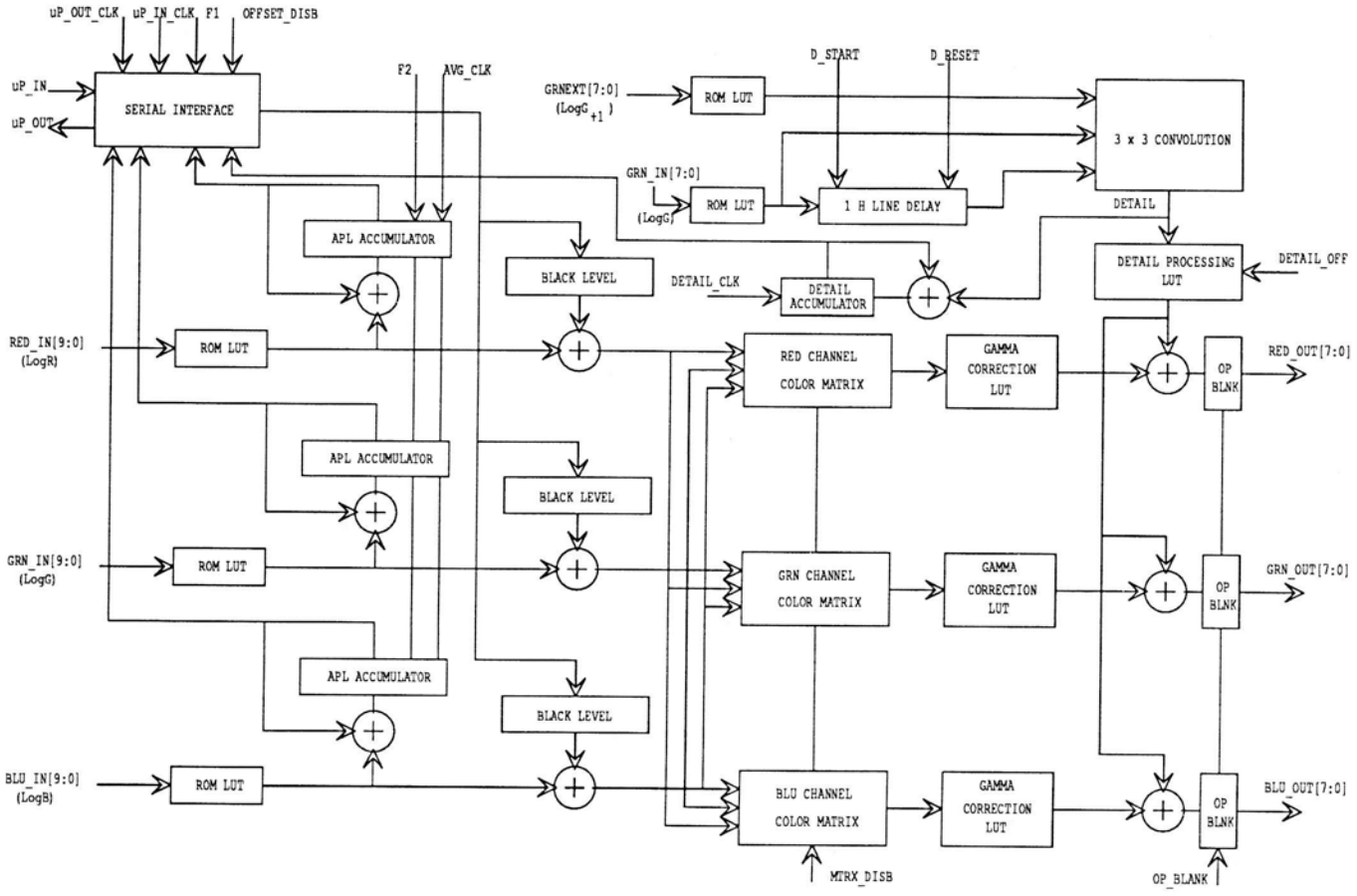


**Fig. 13 RGB Post-Processor Implementation**

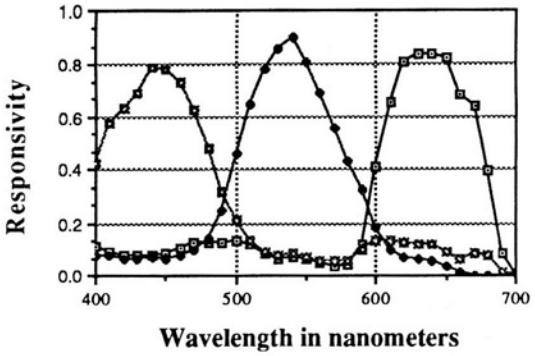


Fig. 14 CCD Camera Color Responsivities

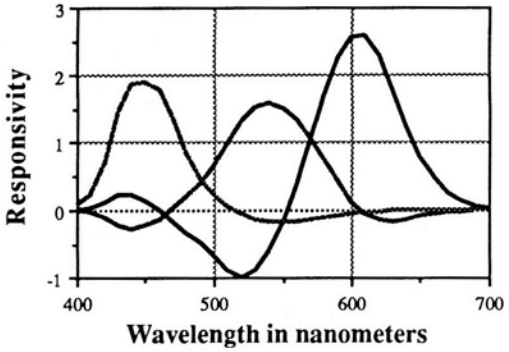


Fig. 15 Optimum Camera Responsivities

In order to achieve the required negative camera sensitivities, the 3 x 3 matrix shown below can be used

$$\begin{aligned} R_o &= a_{11} R_i + a_{12} G_i + a_{13} B_i \\ G_o &= a_{21} R_i + a_{22} G_i + a_{23} B_i \\ B_o &= a_{31} R_i + a_{32} G_i + a_{33} B_i. \end{aligned} \quad (3)$$

$R_i$, $G_i$ and $B_i$ are the linearly quantized, interpolated signals from the CFA processor, and $R_o$, $G_o$, and $B_o$ are the color corrected matrix outputs. The co-efficients $a_{ij}$ depend on the color-mixture functions of the phosphors used in the television display, and the responsivities of the RGB signals prior to matrixing, which includes the lens, infrared blocking filter, and color sensor.[29] Using the matrix listed below, the color responsivities of the camera can be corrected to appear as shown in Fig. 16

$$\begin{aligned} R_o &= 1.75 R_i - 0.19 G_i - 0.56 B_i \\ G_o &= -0.03 R_i + 1.25 G_i - 0.22 B_i \\ B_o &= -0.12 R_i - 0.38 G_i + 1.50 B_i. \end{aligned} \quad (4)$$

The negative off-diagonal matrix terms significantly increase the color saturation of the image. The matrix is implemented using cascaded metal-mask programmable shift and add or subtract (MPSAS) circuit modules. The red channel of the matrix is shown in Fig. 17. The green and blue channels have an identical form, but a different input signal mapping. Cascading the MPSAS modules as shown allows sufficient co-efficient accuracy to be maintained while using a minimum number of adders.

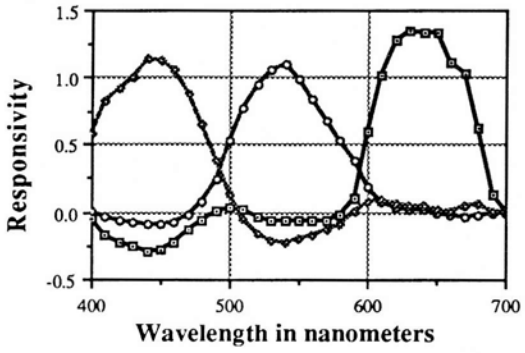


Fig. 16 Matrixed Camera Responsivities

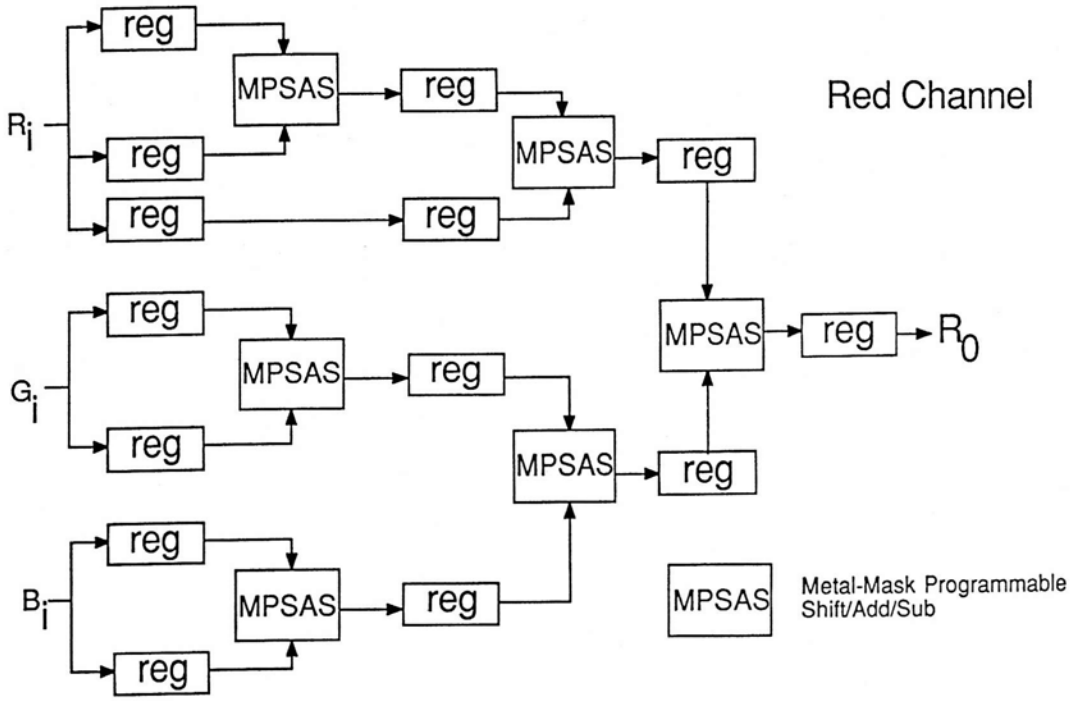


**Fig. 17 Red Channel Matrix Implementation**

The matrixed RGB signals are gamma-corrected using three on-chip ROM look-up tables, which are programmed using the SMPTE 240-M opto-electronic transfer equation[30]

$$C_{out} = 1.1115\ C_{in}^{0.45} - 0.1115 \text{ for } C_{in} >= 0.0228 \quad (5)$$
$$C_{out} = 4.0\ C_{in} \text{ for } C_{in} < 0.0228$$

where $C_{in}$ is the input code value normalized between zero and one, and $C_{out}$ is the normalized output code value.

The RGB post-processor includes the novel edge-enhancement circuit[31] shown in Fig. 18. The vertical and horizontal high frequency edge "details" are extracted from the green channel, processed, and added back to the red, green, and blue video signals. This technique improves the subjective "crispness" of the image.[32] The unmatrixed green signal is used by the edge enhancement circuit to keep from introducing slight noise and artifacts into the detail channel as a result of matrixing. The chip includes an on-chip green signal line delay and makes use of the line delays on the CFA processor to provide symmetric three-line vertical edge enhancement. The vertical "detail" signal, which carries the high frequency edge information from the "-0.5 +1 -0.5" vertical filter, is horizontally filtered before being summed with the horizontal "-1 +2 -1" detail signal, in order to prevent double enhancement of diagonal edges. The horizontal details receive more boost than the vertical details, in order to compensate for the horizontally oriented optical pre-filter.

The horizontal and vertical detail signals are summed and processed by the detail processing ROM look-up table curve shown in Fig. 19. Low-level detail signals, which typically correspond to noise, are clipped to zero. Higher amplitude details are amplified, and very large edge signals are gradually suppressed to prevent over-enhancement. The detail signal is extracted and processed using a "lightness" type quantization characteristic, so that uniform sharpening occurs throughout the luminance range.[33]

A photomicrograph of the RGB post-processor chip is shown in Photo 3. The chip is 11.5 mm x 11.2 mm, with 115,000 transistors. The digital RGB output signals from the post-processor are converted to analog video signals using an off-the-shelf triple D/A converter.

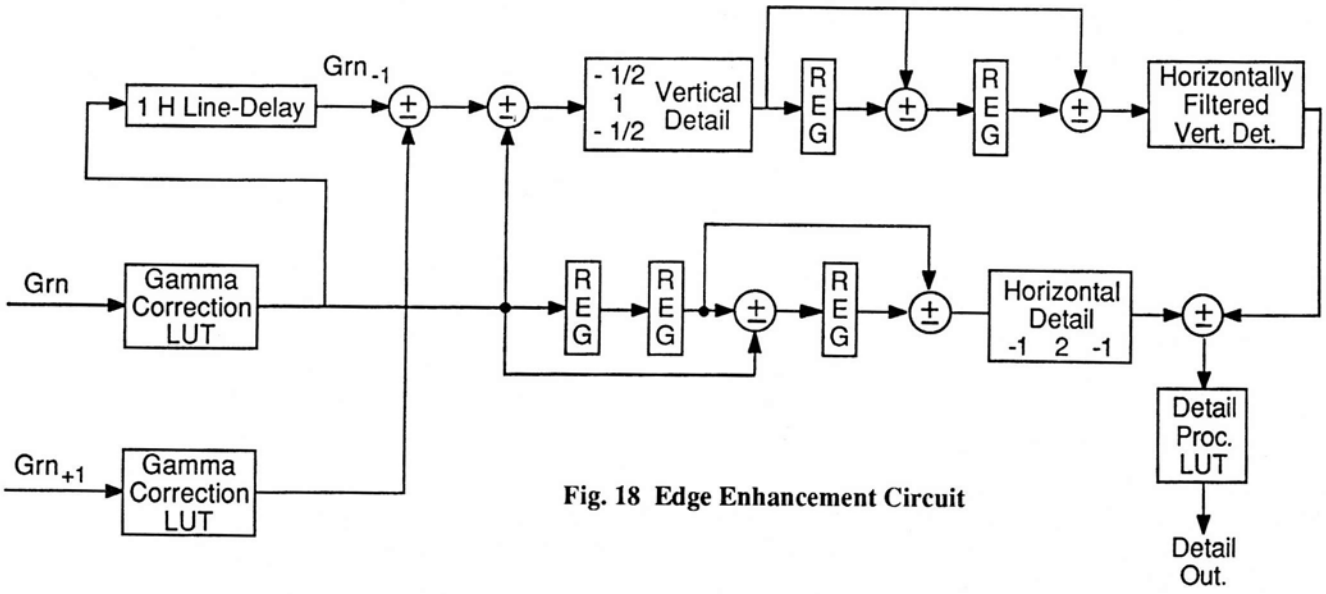


**Fig. 18 Edge Enhancement Circuit**

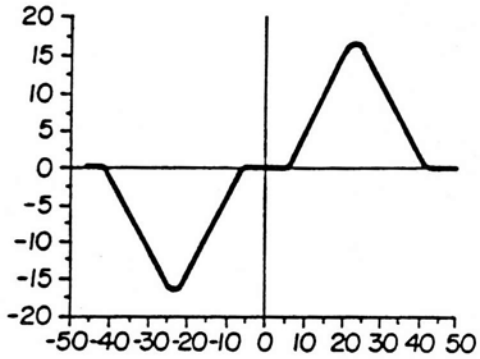


**Fig. 19 Detail Processing LUT**

## 7. SYSTEM DESIGN

All of the digital camera circuits, including the sensor and the two DSP chips, are controlled by a custom Programmable Timing Generator IC.[34] The chip is based on three custom EPROM NOR-planes, and incorporates pixel and line counters, 16 state-variable flip-flops, and 28 output flip-flops. A PC-based timing generation program allows the timing to be quickly developed or modified. The chip, which is 6.5 mm x 7.5 mm, was fabricated in a 1.6-micron CMOS process that includes n-channel EPROM transistors.

The CFA processor and RGB post-processor ICs were developed using software "emulation" rather than by constructing large hardware prototypes composed of off-the-shelf digital devices. This reduced the development time and allowed a large number of image processing options to be tested. The output of a single-chip color image sensor was digitized and stored in a custom image memory with a very flexible architecture. Images were loaded into an image processing computer, where the processing algorithms, chip architectures, and data path word lengths were optimized. Still images and short image sequences were then loaded back into the custom image memory and displayed on a video monitor.

The design of the chips was done entirely with a silicon compiler tool set, except for the ROMs and line delays which were designed using conventional tools and imported into the compiler environment. The data paths are designed with simple ripple-carry adders and dynamic registers. All data-path cells were obtained from internally developed parameterized generators.

Although the present prototype cameras use sensors with 768 horizontal pixels and a clock rate of 14.3 MHz, the CFA processor and RGB post-processor chips have been tested at clock frequencies between 1 and 15 MHz, making the chips suitable for NTSC and PAL video standards, as well as lower frequency still camera systems. The chips include resettable line delays to support sensors with a smaller number of photosites per line, and can be used with interlaced or progressive scan sensors.

## 8. SUMMARY

An operational digital camera has been developed using a high-performance image sensor incorporating lenslets and two full custom VLSI video processor chips. Photo 4 shows an black-and-white photograph from a color monitor display of an image from the digital CCD camera. Digital video processing offers higher image quality compared to analog approaches, and provides reliable, manufacturable, drift-free systems. The CMOS VLSI digital circuits offer real-time video operation while meeting the size, power, and cost constraints of one-chip cameras, and providing the flexibility needed for many different applications.

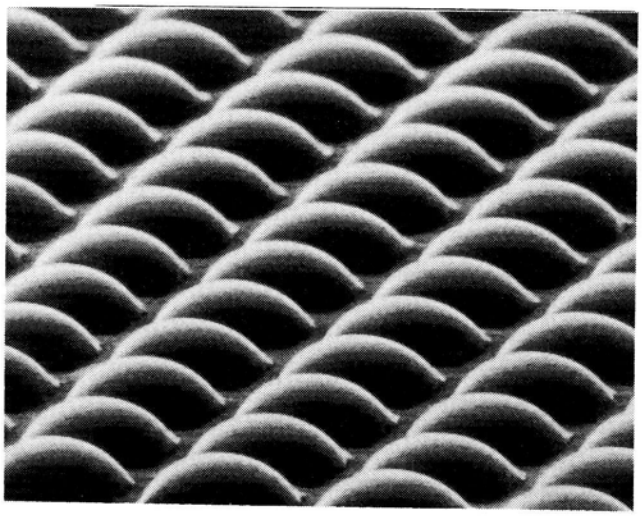

**Photo 1 Lenslets**

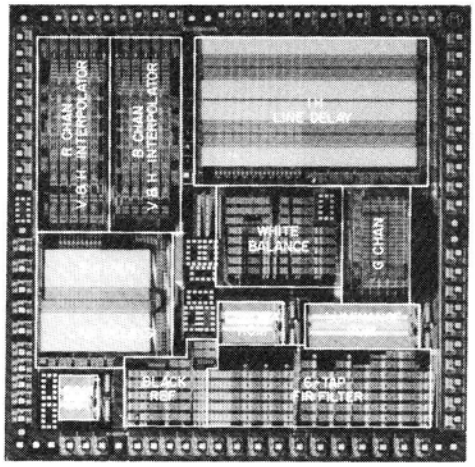


**Photo 2 CFA Processor Layout**

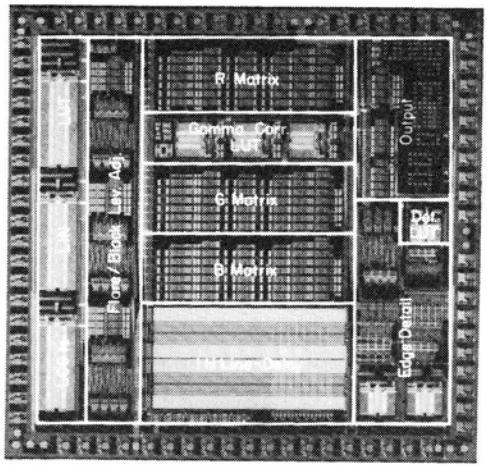


**Photo 3 RGB Post-Processor Layout**

**Photo 4 Monitor Photo of Camera Output**

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US007057657B1

(12) **United States Patent**
**Ishihara et al.**

(10) **Patent No.: US 7,057,657 B1**
(45) **Date of Patent: Jun. 6, 2006**

(54) **SOLID-STATE IMAGE PICKUP APPARATUS CAPABLE OF READING OUT IMAGE SIGNALS WHILE THINNING THEM DOWN HORIZONTALLY AND SIGNAL READING METHOD THEREFOR**

(75) Inventors: **Atsuhiko Ishihara**, Asaka (JP); **Tomohiro Sakamoto**, Miyagi (JP)

(73) Assignee: **Fuji Photo Film Co., Ltd.**, Kanagawa (JP)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/431,875**

(22) Filed: **Nov. 2, 1999**

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
***H04N 5/335*** (2006.01)

(52) **U.S. Cl.** ..... **348/312**; 348/322; 348/220.1

(58) **Field of Classification Search** ..... 348/312, 348/311, 315, 317, 319, 322, 324, 362, 272, 348/273, 279, 294, 350, 220.1, 222.1, 229.1, 348/333.01, 333.09, 333.11; 250/208.1
See application file for complete search history.

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*Primary Examiner*—Aung Moe
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

In a solid-state image pickup apparatus, an image pickup section includes a color separating section having color filters assigned to three primary colors for separating colors of light incident from a desired scene. The color filters assigned to the color G are arranged in stripes. A system controller controls an output of a drive signal generating section for each of an all pixel read mode and a photometry control mode in response to the stroke of a shutter release operation. In the photometry control mode, the image pickup device is supplied with drive signals in response to a horizontal timing signal fed from a timing signal generator and a control signal fed from the system controller. The image pickup device thus reads out only the signal charges representative of the color G in this mode, thereby especially implementing the signal charge reading at a doubled speed.

**20 Claims, 6 Drawing Sheets**

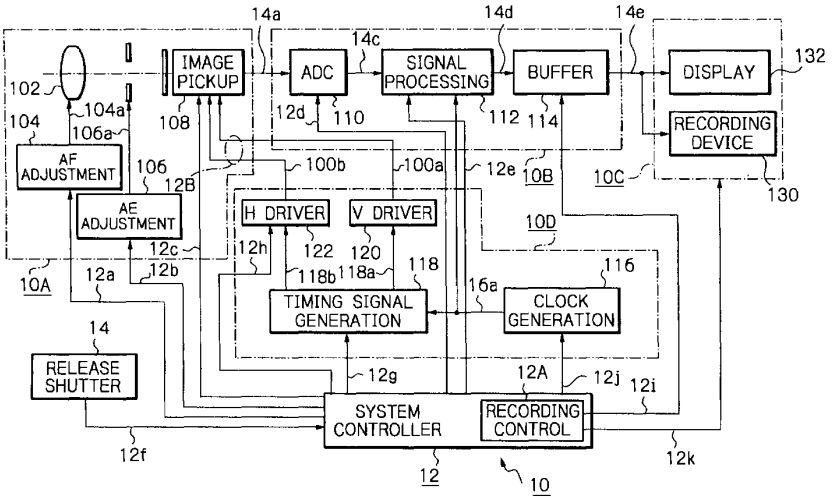


*Fig. 1*

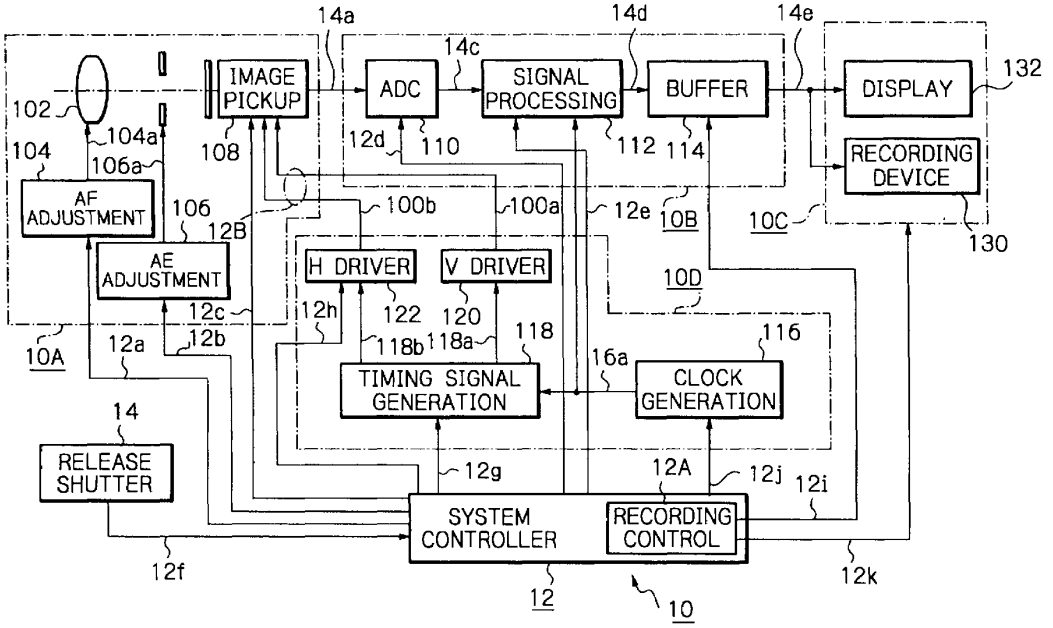

14a
14d
14e
14c
IMAGE PICKUP
ADC
SIGNAL PROCESSING
BUFFER
DISPLAY
132
102
104a
108
12d
110
112
114
RECORDING DEVICE
104
106a
AF ADJUSTMENT
106
12B
100b
100a
12e
10B
10C
130
AE ADJUSTMENT
H DRIVER
V DRIVER
10D
12c
12h
122
120
118
116
10A
12a
12b
118b
118a
16a
TIMING SIGNAL GENERATION
CLOCK GENERATION
14
RELEASE SHUTTER
12g
12A
12j
12i
SYSTEM CONTROLLER
RECORDING CONTROL
12f
12k
12
10

*Fig. 2*

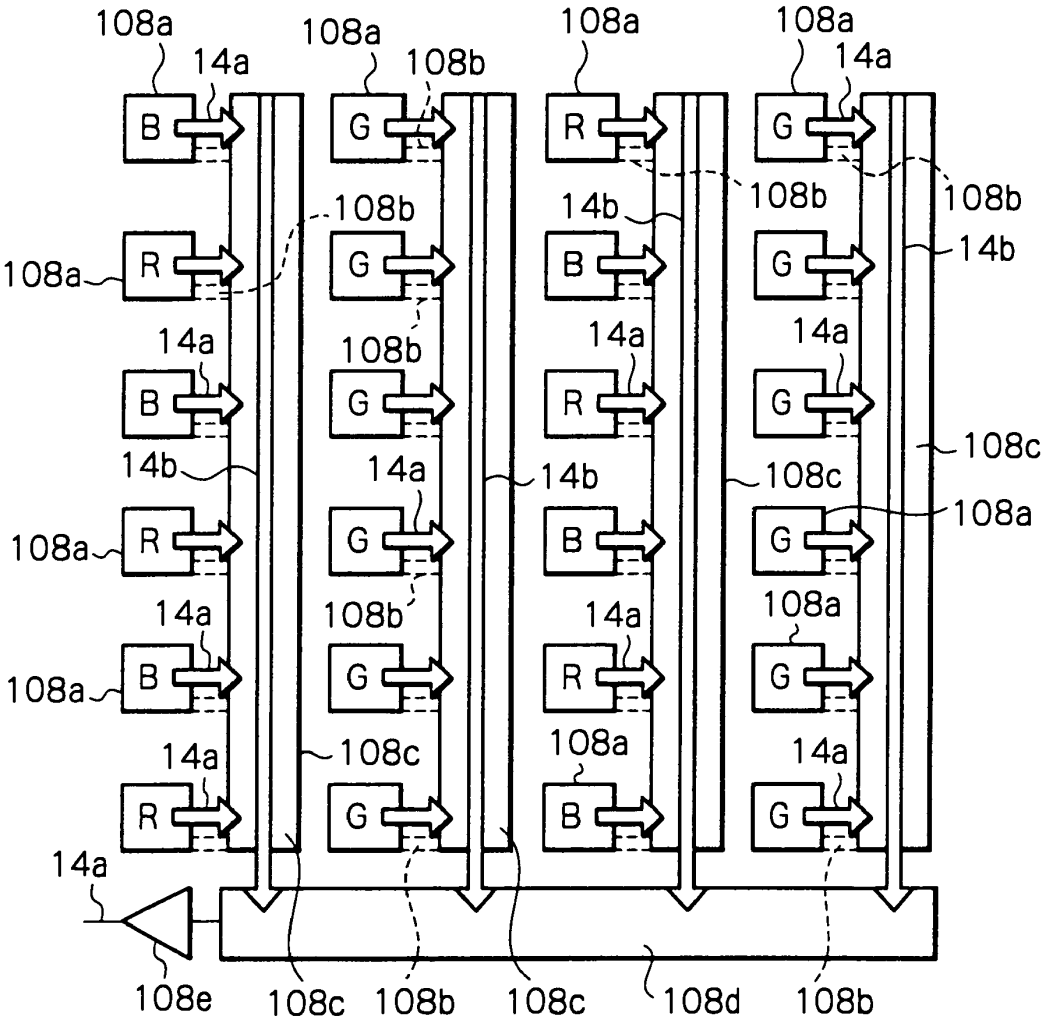


Fig. 3

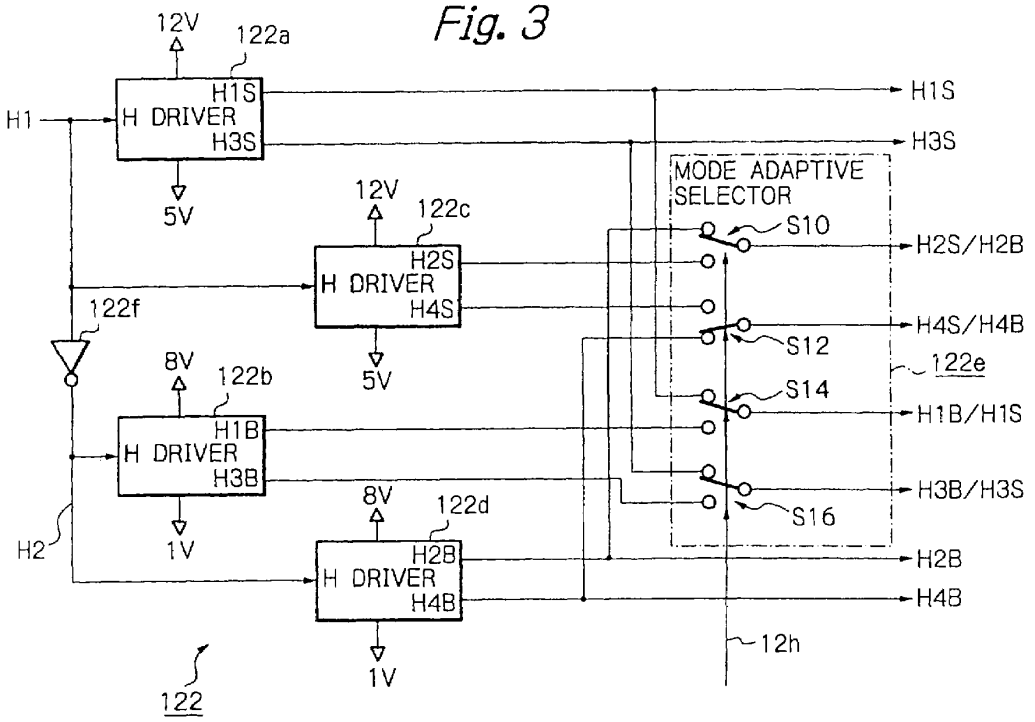
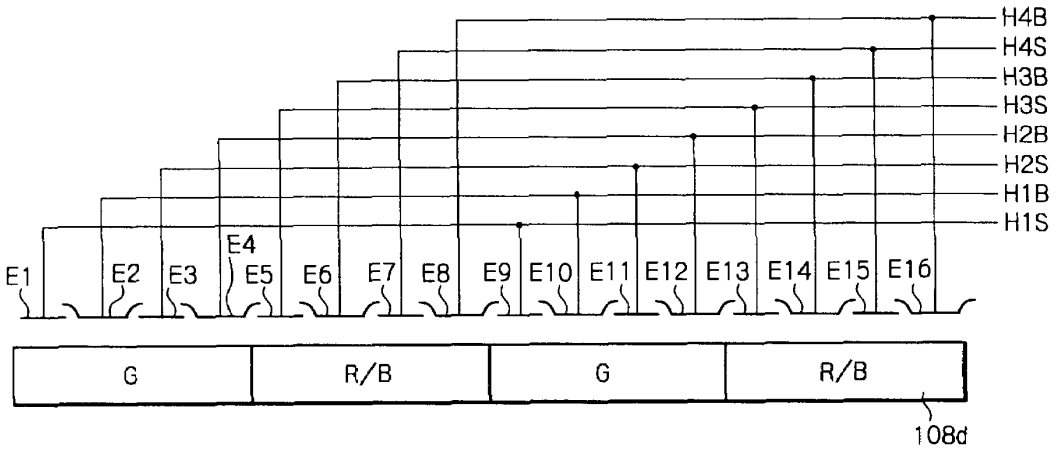

12V
122a
H1S
H DRIVER
H3S
5V
H1
12V
122c
H2S
H DRIVER
H4S
5V
122f
8V
122b
H1B
H DRIVER
H3B
1V
H2
8V
122d
H2B
H DRIVER
H4B
1V
122
MODE ADAPTIVE SELECTOR
S10
S12
S14
S16
122e
12h
H1S
H3S
H2S/H2B
H4S/H4B
H1B/H1S
H3B/H3S
H2B
H4B

*Fig. 4*


H4B
H4S
H3B
H3S
H2B
H2S
H1B
H1S
E1
E2
E3
E4
E5
E6
E7
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E11
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E14
E15
E16
G
R/B
G
R/B
108d

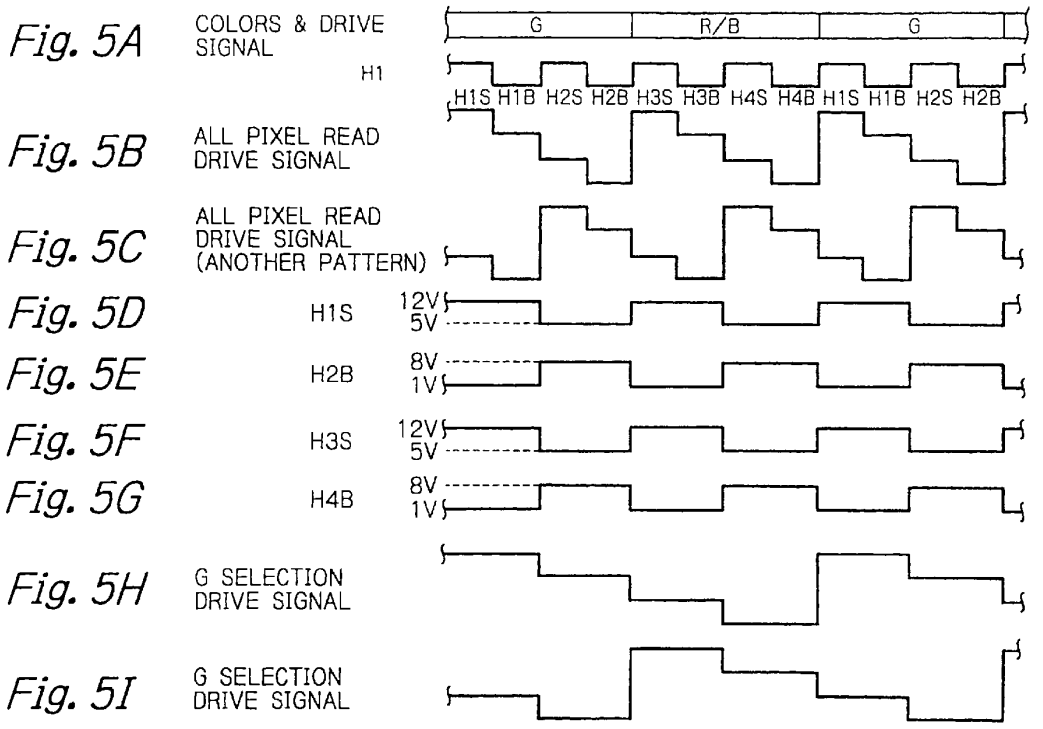
Fig. 5A
COLORS & DRIVE SIGNAL
G
R/B
G
H1
H1S H1B H2S H2B H3S H3B H4S H4B H1S H1B H2S H2B
Fig. 5B
ALL PIXEL READ DRIVE SIGNAL
Fig. 5C
ALL PIXEL READ DRIVE SIGNAL (ANOTHER PATTERN)
Fig. 5D
H1S
12V
5V
Fig. 5E
H2B
8V
1V
Fig. 5F
H3S
12V
5V
Fig. 5G
H4B
8V
1V
Fig. 5H
G SELECTION DRIVE SIGNAL
Fig. 5I
G SELECTION DRIVE SIGNAL

Fig. 6A

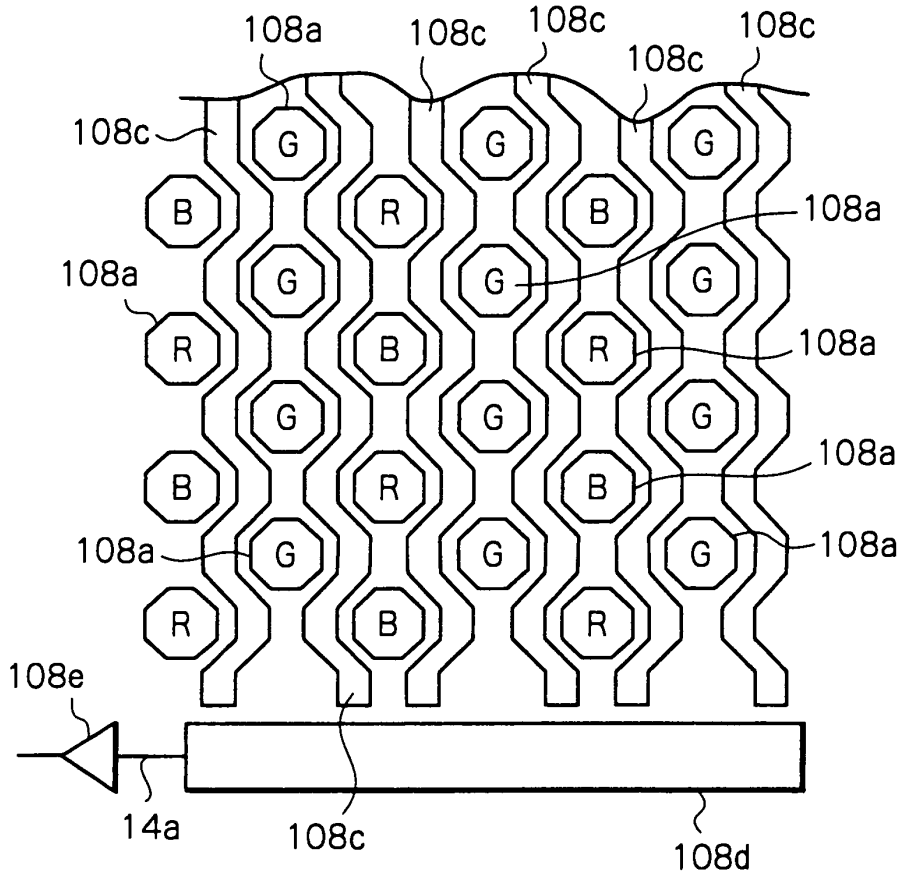


Fig. 6B

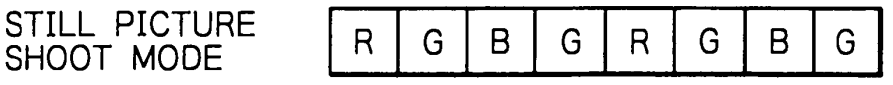


Fig. 6C

# SOLID-STATE IMAGE PICKUP APPARATUS CAPABLE OF READING OUT IMAGE SIGNALS WHILE THINNING THEM DOWN HORIZONTALLY AND SIGNAL READING METHOD THEREFOR

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a solid-state image pickup apparatus capable of reading out images signals while thinning them down in the horizontal direction, and a signal reading method therefor. More particularly, the present invention relates to a solid-state image pickup apparatus capable of processing image signals representative of, e.g., a scene picked up and outputting the processed image signals while using the image signals for a control purpose. The present invention is desirably applicable to, e.g., a digital still camera, image input apparatus or similar imaging apparatus of the type automatically adjusting a focus and an exposure with image signals representative of a scene picked up.

2. Description of the Background Art

An imaging apparatus of the type described includes an image pickup section having CCDs (Charge Coupled Devices) or similar photosensitive devices each forming a single pixel or cell. Today, the number of pixels required of the image pickup section is increasing to meet the increasing demand for higher image quality. This, however, increases a period of time necessary for image signals to be read out of the image pickup section.

Japanese patent laid-open publication No. 136244/1998, for example, teaches an electronic image pickup apparatus capable of reducing the above period of time for driving an image pickup section. The image pickup apparatus taught in this document implements the display of a movie with a drive frequency of less than 20 MHz despite that it uses an image sensor having about 1,000,000 CCDs. Specifically, the apparatus uses color filters arranged in a Bayer pattern in combination with the CCD image sensor. In a high speed mode, the apparatus drives the image pickup section in such a manner as to output one line of image signals every three lines, i.e., to thin down the lines in the vertical direction. This is successful to read image signals at a high speed with a low drive frequency. Particularly, when automatic focus (AF) adjustment, automatic white balance (AWB) adjustment and automatic exposure (AE) adjustment are effected during movie display, control data is required frame by frame. In this case, the apparatus selects a mode for adding three consecutive lines of signals and outputting the resulting sum. In this manner, to reduce the signal reading time, the apparatus thins down the lines in the vertical direction. For the AF, AWB and AE adjustment, the apparatus adds up three consecutive lines of signal charges in order to produce a control signal, i.e., reads all of the three primary colors R (red), G (green) and B (blue) separated by the color filters and then combines them.

As for the generation of control data for AE and AF, a luminance signal plays an important role, as well known in the art. In addition, in a solid-state image pickup apparatus, only the color G contributes to the generation of a luminance signal, as also generally accepted. For photometry, therefore, only the color G may be read out in order to promote effective signal reading. However, it is difficult with the Bayer arrangement to read only the color G because the colors R, G and B exist together in an array.



## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a solid-state image pickup apparatus capable of reading only the color G and eventually reducing a period of time necessary for signal charges to be transferred in the horizontal direction, and a signal reading method therefor.

A solid-state image pickup apparatus of the present invention includes an image pickup section. The image pickup section includes a color separating section having color filters assigned to three primary colors R, G and B for separating colors of light incident from a desired scene. The color filters assigned to the color G are arranged in stripes. A plurality of photosensitive cells are arranged bidimensionally in one-to-one correspondence to the color filters each for transforming light output from a particular color filter to a corresponding signal charge. A plurality of vertical transfer paths each have transfer elements vertically arranged for vertically transferring signal charges fed from the adjoining photosensitive cells. A horizontal transfer path perpendicular to the vertical transfer paths has transfer elements horizontally arranged for transferring the signal charges fed from the vertical transfer paths. Signal reading circuitry shifts the signal charges from the photosensitive cells to the vertical transfer paths. Charge sweeping circuitry sweeps out needless ones of the signal charges stored in the photosensitive cells. A mode selecting section selects, when the operation for reading the signal charges out of the image pickup section is represented by a mode, either one of an all pixel read mode for reading the signal charges from all of the photosensitive devices and a particular pixel read mode for reading only the signal charges representative of the color G. A drive signal generating section feeds horizontal and vertical drive signals to the image pickup section, and provides the horizontal drive signals with a period shorter in the particular pixel read mode than in the all pixel read mode. A controller controls the drive signal generating section in a particular manner in each of the all pixel read mode and particular pixel read mode.

## BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention will become more apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. **1** is a block diagram schematically showing a solid-state image pickup apparatus embodying the present invention;

FIG. **2** is a schematic block diagram showing a specific configuration of an image pickup section included in the illustrative embodiment;

FIG. **3** is a schematic block diagram showing a specific configuration of an H (horizontal) driver also included in the illustrative embodiment;

FIG. **4** is a diagram showing a relation between electrodes arranged on a horizontal transfer path included in the image pickup section of FIG. **2** and horizontal drive signals applied thereto;

FIGS. **5**A–**5**I are timing charts representative of a specific relation between drive signals fed from the H driver of FIG. **3** in a still picture shoot mode and a photometry control mode available with the illustrative embodiment;

FIG. **6**A is a view showing another specific configuration of the image pickup section;

FIG. **6**B shows color signals R, G and B read out of the image pickup section of FIG. **6**A in a specific sequence; and

FIG. **6**C shows the color signals G read out of the image pickup section of FIG. **6**A in the photometry control mode.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Briefly, to read image signals at a high speed, the present invention replaces the conventional thinning of lines in the vertical direction with thinning in the horizontal direction. For this purpose, in accordance with the present invention, a color pattern output from a color separating section and horizontal drive signals output from a drive signal generating section are fed to an image pickup section in order to implement a particular pixel read mode different from the conventional all pixel read mode. It is to be noted that structural elements not relevant to the understanding of the present invention are not shown or described, and that reference numerals attached to various signals correspond to reference numerals designating connection lines on which the signals appear.

Referring to FIG. **1** of the drawings, a solid-state image pickup apparatus embodying the present invention is shown and implemented as a digital still camera by way of example. As shown, the digital still camera, generally **10**, is generally made up of an image pickup section **10**A, a signal processing section **10**B, a signal output section **10**C, a drive signal generating section **10**D, a system controller **12**, and a release shutter **14**. The image pickup section **10**A includes a lens **102**, an AF adjustment **104** including a focusing mechanism, not shown, an AE adjustment **106** including a stop mechanism, not shown, and an image pickup **108**. If desired, a shutter mechanism, not shown, may be positioned in front of the image pickup **108** in the direction light incidence in order to fully intercept light.

The lens **102** focuses incident light representative of a scene on the photosensitive surface of the image pickup **108**. The AF adjustment **104** moves the lens **102** to an optimal position matching with information output from the focusing mechanism and representative of a range between a desired subject and the camera **10**. At this instant, the system controller **12** processes the range information and determines the optimal position of the lens **102**. More specifically, the system controller **12** feeds a control signal **12***a* to the AF adjustment **104**. In response, the AF adjustment **104** drives its focusing mechanism with a drive signal **104***a* so as to move the lens **102** to an optimal focal position.

The system controller **12** includes an exposure control circuit, not shown, for calculating the photometric value of the scene including the subject. The AE adjustment **106** adjusts, under the control of the exposure control circuit, an iris diaphragm included in the stop mechanism, thereby restricting an incident beam to an optimal quantity. In the illustrative embodiment, photometry is implemented by part of image signals. The system controller **12** calculates an exposure and feeds a control signal **12***b* representative of the exposure to the AE adjustment **106**. In response, the AE adjustment **106** delivers a drive signal **106***a* to each of the stop mechanism and shutter mechanism for setting up an optimal exposure indicated by the control signal **12***b*.

FIG. **2** shows a specific configuration of the image pickup **108**. As shown, the image pickup **108** has photosensitive cells or photoelectric transducers **108***a* arranged bidimensionally in rows and columns. The photosensitive cells **108***a* each transform incident light to a corresponding electric signal or signal charge. Color filters for color separation, not shown, each are positioned in front of a particular photosensitive cell **108***a* in the direction of light incidence. The color filters are implemented as a single plate and arranged such that, e.g., three primary colors R, G and B separated by the filters are selectively input to the photosensitive cells **108***a*, as indicated by letters R, G and B in FIG. **2**. The arrangement of the colors R, G and B shown in FIG. **2** is generally referred to as a G vertical stripe, RB full checker pattern.



The image pickup **108** receives a control signal **12***c* from the system controller **12** and receives drive signals **12**B from the drive signal generating section **10**D which will be described later specifically. The photosensitive cells **108***a* are implemented by CCDs. As shown in FIG. **2**, transfer gates or signal read gates **108***b* each are connects between one photosensitive cell **108***a* and a vertical transfer path **108***c* adjoining the cell **108***a*, preventing a signal charge **14***a* stored in the cell **108***a* from leaking. Specifically, the transfer gates **108***b* transfer signal charges **14***a* stored in the associated photosensitive cells **108***a* to the vertical transfer paths **108***c* adjoining the cells **108***a* in response to field shift pulses not shown. The field shift pulses are fed to the transfer gates **108***b* via electrodes not shown.

The drive signals **12**B fed from the drive signal generating section **10**D to the image pickup **108**, as mentioned earlier, are made up of vertical drive signals **100***a* and horizontal drive signals **100***b* which will be described specifically later. Each vertical transfer path **108***c* sequentially transfers, in accordance with the vertical drive signals **100***a*, the signal charges **14***a* read out of the adjoining photosensitive cells **108***a* via the transfer gates **108***b* in the direction of columns, i.e., vertically as indicated by arrows **14***b* in FIG. **2**. As shown in FIG. **2**, the signal charges **14***a* transferred vertically downward along the transfer paths **108***c* are handed over to a horizontal transfer path **108***d*. The horizontal transfer path **108***d* transfers the signal charges **14***a* horizontally to the signal processing section **10**B via an amplifier **108***e* in accordance with the horizontal drive signals **100***b*.

As shown in FIG. **1**, the signal processing section **10**B includes an ADC (Analog-to-Digital Converter) **110**, a signal processing **112**, and a buffer **114**. The ADC **110** converts the analog image signals, or signal charges, **14***a* output from the image pickup **108** to digital image data **14***c* in accordance with a control signal **12***d* fed from the system controller **12** and a clock signal, not shown, fed from a clock generation **116** which will be described specifically later. The signal processing **112** executes white balance correction, gamma correction, aperture correction and other conventional correction with the digital data **14***c* input thereto from the ADC **110**. Subsequently, the signal processing **112** processes the corrected digital data in accordance with either one of two different modes selected via the release shutter **14**. The two modes are a still picture shoot mode for storing at least a still picture picked up in a recording device **130** included in the signal output section **10**C, and a photometry control mode or preshooting mode for simply controlling the AE mechanism and AF mechanism of the image pickup section **10**A.

The system controller **12** feeds a control signal **12***e* representative of the above still picture shoot mode or the photometry control mode currently selected on the camera **10** to the signal processing **112**. In the still picture shoot mode, the corrected image data **14***d* are subjected to compression or similar preselected modulation under the control of the system controller **12**. In the photometry control mode, the image signals **14***a* are read out of the image pickup **108** at a rate, e.g., two times higher than the conventional reading rate under the control of the system controller **12**. In addition, the image signals **14***a* are thinned down in the

vertical direction, so that they can be displayed on a display **132** also included in the signal output section **10**C. The compression or similar modulation effected by the image processing **112** in the still picture shoot mode transforms the image signals **14***a* to video signals capable of being written to the recording device **130**. The signal processing **112** delivers only the image data **14***d* to be displayed or recorded to the buffer **114**.

The system controller **12** controlling the entire camera **10** receives a signal **12***f* from the release shutter **14** and determines which of the still picture shoot mode and photometry control mode is selected by the operator. The system controller **12** controls the drive signal generating section **10**D on the basis of the result of the above decision. The system controller **12** includes a record control **12**A. The record control **12**A controls the buffer **114** and the recording device **130** of the signal output section **10**C in accordance with a timing signal output from the system controller **12**.

The drive signal generating section **10**D includes a clock generation **116** and a timing signal generation **118**. The system controller **116** feeds a control signal **12***j* to the clock generation **116** and causes it to generate a synchronizing signal **16***a*. The synchronizing signal **16***a* is derived from an original oscillation clock causing the camera **10** to operate with an NTSC (National Television System Committee) system or a PAL (Phase Alternation by Line) system. The synchronizing signal **16***a* is fed from the clock generation **116** to the signal processing **112** and timing signal generation **118**. In addition, the clock generation **116** delivers a particular clock to each of the ADC **110** and buffer **114** as a sampling signal or a write/read enable signal.

The timing signal generation **118** outputs, in accordance with the synchronizing signal **16***a*, various timing signals including a vertical timing signal **118***a* and a horizontal timing signal **118***b* as well timing signals, not shown, for effecting a field shift and a line shift. The vertical timing signal **118***a* and horizontal timing signal **118***b* are respectively applied to a V (vertical) driver **120** and an H (horizontal) driver **122** for driving the vertical transfer paths **108***c* and horizontal transfer path **108***d*, FIG. **2**. The V driver **120** and H driver **122** respectively output the previously mentioned drive signals **100***a* and **100***b* in accordance with the timing signals **118***a* and **118***b*. Generally, the vertical drive signals **100***a* output from the V driver **120** are switched in accordance with the mode selected in order to adjust the signal reading rate. The timing signal generation **118** additionally outputs timing signals, not shown, for controlling the AF adjustment **104** and AE adjustment **106**.

When the system controller **12** delivers a control signal **12***g* indicative of the photometry control mode to the timing signal generation **118**, the generation **118** causes the substrate voltages, i.e., overflow-drain (OFD) voltages of the photosensitive devices **108***a* assigned to the colors R and B to rise. This will be described more specifically later. Generally, the signal reading rate is adjusted also by the vertical drive signals **100***a* output from the V driver **120** in accordance with the mode selected.

In the illustrative embodiment, not only the V driver **120** but also the H driver **122** are switched in accordance with the mode selected. FIG. **3** shows a specific configuration of the H driver **122**. As shown, the H driver **122** is made up of four H drivers **122***a*, **122***b*, **122***c* and **122***d* and a mode adaptive selector **122***e*. Voltages of 12 V and 5 V are applied to the H drivers **122***a* and **122***c*, respectively. The outputs of the H drivers **122***a* and **122***c* are dependent on the level of a horizontal timing signal H**1** input to the H drivers **122***a* and **122***c*. The horizontal timing signal H**1** corresponds to the horizontal timing signal **118***b*, FIG. **1**; the label H**1** is used to adequately show the feature of the signal. Voltages of 8 V and 1 V are applied to the H drivers **122***b* and **122***d*, respectively. An inverter **122***f* inverts the horizontal timing signal H**1** to thereby output an inverted horizontal timing signal H**2** and feeds the signal H**2** to the H drivers **122***b* and **122***d*. The outputs of the H drivers **122***b* and **122***d* are dependent on the level of the horizontal timing signal H**2**. It follows that the outputs H**1**S and H**3**S of the H driver **122***a* and the outputs H**2**S and H**4**S of the H driver **122***c* each have an amplitude between 12 V to 5 V, and that the outputs H**1**B and H**3**B of the H driver **122***b* and the outputs H**2**B and H**4**B of the H driver **122***d* each have an amplitude between 8V to 1V.

The system controller **12** feeds a control signal **12***h* to the H driver **122** in accordance with the mode selected. The H driver **122** causes the mode adaptive selector **122***e* to output a signal level dependent on the control signal **12***h*. Specifically, the mode adaptive selector **122***e* has four switches S**10**, S**12**, S**14** and S**16**. The control signal **12***h* causes the selector **122***e* to select output signals H**2**S and H**4**S of the H driver **122***c* and the output signals H**1**B and H**3**B of the H drivers **122***b* in the still picture shoot mode or select the output signals H**1**S and H**3**S of the H driver **122***a* and the output signals H**2**B and H**4**B of the H driver **122***d* in the photometry control mode. FIG. **3** shows settings of the switches S**10**, S**12**, S**14** and S**16** matching one of such two conditions, the photometry control modes for reading only the color G. The eight signals H**1**S–H**4**S and H**1**B–H**4**B each are fed to two of sixteen electrodes E**1**–E**16** shown in FIG. **4**. The electrodes E**1**–D**16** each are associated with a particular transfer element of the horizontal transfer path **108***d*, FIG. **2**.

Referring again to FIG. **1**, the buffer **114** included in the signal processing section **10**B has a function of amplifying the video signal **14***d* output from the signal processing **112** to a preselected amplitude and a function of adjusting a period of time at the time of recording as well as other functions. The buffer **114** outputs a video signal **14***e* representative of an image to the signal output section **10**C in accordance with a control signal **12***i* output from the record control **12**A of the system controller **12**.

The recording device **130** of the signal output section **10**C includes a semiconductor memory applicable to, e.g., a memory card, an optical recording medium, a magnetoptical recording medium or similar recording medium not shown. The recording device **130** records the video signal **14***e* in the recording medium in accordance with a control signal **12***k* output from the record control **12**A. The recording device **130** is capable of reading the video signal **14***e* out of the recording medium and display it on the display **132**, as desired. If the recording medium is removable from the recording device **130**, then the medium may be removed and mounted to an apparatus for reproducing a video signal or printing out an image.

The illustrative embodiment allows the operator to press the release shutter **14** stepwise to either one of two positions, i.e., a half-pressed position and a full-pressed position. In the half-pressed position, the release shutter **14** selects the photometry control mode and sends the signal **12***f* representative of the mode to the system controller **12**. In the full-pressed position, the release shutter **14** provides the system controller **12** with an image pickup timing while sending the signal **12***f* representative of the still picture shoot mode to the system controller **12**. Further, if the power supply to the release shutter **14** is set up and if a monitor

switch, not shown, mounted on the camera **10** is turned on, the system controller **12** causes the display **132** to operate in a movie mode.

The operation of the digital camera **10** having the above configuration will be described hereinafter. First, the operator intending to shoot a desired scene presses the release shutter **14** to the half-pressed position assigned to the photometry control mode. In this stage of operation, among the color signals R, G and B produced by the image pickup **108**, only the color signal G is read out under the control of the system controller **12**. This is effected at a high speed in accordance with the drive signals **12**B, as will be described specifically later. The resulting image signals **14***a* output from the image pickup **108** are fed to the signal processing section **10**B in accordance with the control signal **12***c* output from the system controller **12**. The signal processing section **10**B digitizes the image signals **14***a* and delivers the resulting image data **14***c* to the system controller **12** as photometry data via a signal line not shown.

The system controller **12** performs calculation with the above photometry data so as to produce the control signals **12***a* and **12***b* for AF adjustment and AE adjustment, respectively. The control signals **12***a* and **12***b* are respectively fed to the AF adjustment **104** and AE adjustment **106**, as stated earlier. In response, the AF adjustment **104** and AE adjustment **106** each perform particular adjustment by use of the respective mechanism. The AF adjustment and AE adjustment are repeated so long as the photometry control mode is selected.

The operator presses the release shutter **14** deeper to the full-pressed position assigned to the still picture shoot mode at any desired time for shooting the scene. In response, the release shutter **14** feeds the signal **12***f* for recording the scene to the system controller **12**. As a result, the image pickup section **10**A picks up light incident from the scene in the same manner as in the photometry control mode. In the still picture shoot mode, however, the image pickup **108** executes processing for outputting all of the three color signals R, G and B. This is, of course, done by drive signals different from the drive signals used in the photometry mode. The resulting image signals **14***a* are digitized by the ADC **110** and then fed to the signal processing **112** as the digital data **14***c*. The signal processing **112** processes the digital data **14***c* in such a manner as to further extend their frequencies to the high frequency side. Subsequently, the signal processing **112** executes compression and other conventional processing with the digital data **14***c* and delivers the processed data to the signal output section **10**C via the buffer **114**. In the still picture shoot mode, the signal output section **10**C writes the input image data in the recording device **132** in accordance with the control signal **12***k* output from the record control **12**A. The recording device **132** is, of course, capable of reading the recorded image data in accordance with the control signal **12***k*, as stated previously.

The drive signal generating section **10**D is so constructed as to adapt to both of the photometry mode and still picture shoot mode, as stated earlier. Reference will be made to FIGS. **3** and **5**A–**5**I for describing the operation of the H driver **122**. As shown in FIG. **3**, the horizontal timing signal H**1** is applied to the H drivers **122***a* and **122***c* while the horizontal timing signal H**2** is applied to the H drivers **122***b* and **122***d*.

In the still picture shoot mode, the image pickup **108** receives the previously mentioned OFD voltages for determining the signal charge storing capacities of the photosensitive cells **108***a*, and a transfer gate timing signal, not shown, for effecting the field shift of signal charges from the photosensitive cells **108***a* to the vertical transfer paths **108***c* via the transfer gates **108***b*. Specifically, the signal charges **14***a* stored in the photosensitive cells **108***a* are transferred to the associated vertical transfer paths **108***c* in response to the transfer gate timing signal. The vertical transfer paths **108***c* sequentially transfer the signal charges **14***a* toward the horizontal transfer path **108***d* in synchronism with the vertical drive signals **100***a* fed from the V driver **120** to their transfer elements. The signal charges **14***a* reached the ends of the vertical transfer paths **108***c* are handed over to the horizontal transfer path **108***d*.

Thereafter, the horizontal timing signal H**1** is fed to the horizontal transfer path **108***d*.

In the still picture shoot mode, the signal charges are sequentially input to the horizontal transfer path **108***d* in the order of G, R/B, G, R/B, G and so forth by way of example, as shown in FIG. **5**A. FIG. **5**A shows the R, G and B color pattern **10** at its upper portion and the horizontal drive signal H**1** at its lower portion. As shown, the horizontal timing signal H**1** having a preselected period is fed to read the signal charges **14***a* out of the horizontal transfer path **108***d* by four-phase drive. At the same time, to read out all of the pixels, the H driver **122** combines the horizontal timing signal H**1** of FIG. **5**A and the inverted horizontal timing signal H**2**, not shown, and delivers the combined drive signals to the image pickup **108**, as shown in FIGS. **5**B (drive signal) and **5**C (another pattern).

Consequently, the signal charges **14***a* advance one step in the horizontal direction for one period of the above drive signals.

The photometry control mode for reading out only the color G by use of the G vertical stripe, RB full checker pattern will be described hereinafter. In this mode of operation, the drive signal generating section **10**D raises, among OFD voltages fed to the image pickup **108**, the OFD voltages for the photosensitive cells **108***a* assigned to the colors R and B. As a result, all the signal voltages derived from the colors R and B are swept out to the substrates. At the same time, the drive signal generating section **10**D feeds an OFD voltage allowing an expected amount of signal charge to be stored to the photosensitive cells **108***a* assigned to the color G. In addition, at the time of field shift following the shot, the transfer gate timing signal is fed only to the transfer gates **108***b* associated with the color G. Consequently, only signal charges derived from the color G appear on the vertical transfer paths **108***c*. These signal charges **14***a* are transferred to the horizontal transfer path **108***d*, as stated previously.

In the illustrative embodiment, the above signal charges representative of the color G and existing on the horizontal transfer path **108***d* may advance two steps at a time for one period of the drive signals, as follows. In the photometry control mode, no signal charges exist in the transfer elements of the horizontal transfer path **108***d* originally expected to form R/B packets. Such transfer elements are regarded as elements belonging to G regions. Then, the range of each step of the drive signals remaining at a given voltage is doubled. Stated another way, the signals H**1**S and H**2**B may, in principle, be considered to represent the same state.

The mode adaptive selector **122***e* selects, based on the above concept, the signals H**1**S, H**2**B, H**3**S and H**4**B in place of the signals H**1**B, H**2**S, H**3**B and H**4**S, respectively, under the control of the control signal **12***h*. Consequently, the drive signals H**1**S, H**2**B, H**3**S and H**4**B related to each other as shown in FIGS. **5**D–**5**G are output. At this instant, the drive signals cause the color G selectively obtained, as shown in

FIGS. **5**H and **5**I, to advance two steps corresponding to eight electrodes at a time. That is, the drive signals double the amount of movement by a single drive, compared to the previous all pixel reading. Translating the amount of movement into a period of time, it will be seen that the drive signals have a period only one half of the period of the drive signals fed at the time of all pixel reading. By so transferring the signal charges **14***a* by two steps at a time, it is possible to thin down the image signals to one half in the horizontal direction. As a result, despite the G vertical stripe, RB full checker pattern, only the signal charges **14***a* derived from the color G are read out of the image pickup **108** in half an amount, compared to the amount read out in the still picture shoot mode.

If the above horizontal thinning operation is effected at a two times higher speed, the signal charges **14***a* will be read out at a two times higher speed. This is successful to reduce the horizontal reading period to one-fourth of the horizontal reading period particular to full pixel reading.

By the unique drive scheme described above, image data for photometry control are output at a high speed on the basis of the signal charges **14***a* derived from the color G. The system controller **12** performs calculation with such image data and then executes AF adjustment and AE adjustment described previously. Considering the ever increasing number of pixels, this kind of scheme is particularly desirable when, e.g., AF adjustment uses only a luminance signal. As for AF adjustment using only a luminance signal, the camera **10** is capable of doubling the conventional photometry control speed.

The above embodiment has concentrated on the G vertical stripe, RB full checker pattern in implementing the rapid read-out of the signal charges **14***a* in the photometry control mode. Also available for the rapid reading of the signal charges **14***a* from the horizontal transfer path **108***d* is a so-called honeycomb type G square lattice, RB full checker or checker pattern. This type of pattern has been proposed to solve a problem that the sensitivity or area of the individual photosensitive cell, for example, decreases due to the increasing number of pixels. Specifically, in the honeycomb type pattern, pixels adjoining each other are shifted from each other by half a pitch in the horizontal and vertical directions.

The honeycomb type G square lattice, RB full checker pattern is shown in FIG. **6**A specifically. As shown, the photosensitive devices or cells **108***a* assigned to the colors R, G and B each are shifted by half a pitch from adjoining ones with respect to the center. The honeycomb pattern is the combination of a pattern in which the G cells **108***a* form a square and a full checker pattern in which the R cells **108***a* and B cells **108***a* each diagonally face each other. In this pattern, too, the G cells **108***a* are arranged in vertical arrays or columns not including the R cells **108***a* or the B cells **108***a*. By using this relation effectively, it is possible output the R, G and B color signals to the horizontal transfer path **108***d* in the still picture shoot mode, as shown in FIG. **6**B, or output only the G color signals to the path **108***d* in the photometry control mode, as shown in FIG. **6**C. In FIG. **6**B, the color signals R, G and B appear on the path **108***d* in the order of R, G, B, G, R, G, B and so forth. In FIG. **6**C, only the color signals G appear every other pixel. When the signals G of FIG. **6**C are read out, or horizontally transferred, at a rate double the rate of the horizontal timing signal assigned to the still picture shoot mode, the total reading time is reduced by the intervals between the color signals G.

As stated above, at least in an application in which the photosensitive cells with the color G are arranged in the vertical direction, i.e., in the direction of columns, signal charges of necessary color or colors can be read out in either one of the still picture shoot mode and photometry control mode. That is, the signal charges can be selectively read out even when the number of pixels increases. This insures simple, rapid transfer of signal charges with no consideration given to the order of reading. It follows that processing with data derived from signal charges can be executed more rapidly in the photometry control mode than in the still picture shoot mode. Assuming that a digital still camera effects photometry control within a given period of time, the above reduction of reading time successfully reduces the load to actually act on the individual mechanism. In addition, the camera **10** reading the signal charges in the above manner is practicable even with a Bayer pattern.

The entire disclosure of Japanese patent application No. 315510/1998 filed on Nov. 6, 1998 and including the specification, claims, accompanying drawings and abstract of the disclosure is incorporated herein by reference in its entirety.

While the present invention has been described with reference to the illustrative embodiment, it is not to be restricted by the embodiment. It is to be appreciated that those skilled in the art can change or modify the embodiment without departing from the scope and spirit of the present invention.

What is claimed is:

**1**. A solid-state image pickup apparatus comprising:

an image pickup section including:

a color separating section including color filters assigned to three primary colors R (red), G (green) and B (blue) for separating colors of light incident from a desired scene, the color filters assigned to the color G being arranged in vertical stripes;

a plurality of photosensitive cells arranged bidimensionally in one-to-one correspondence to said color filters each for transforming light output from a particular color filter to a corresponding signal charge;

a plurality of vertical transfer paths, each one offset from each vertical column of said plurality of photosensitive cells, each comprising transfer elements arranged in a vertical direction for vertically transferring signal charges fed from adjoining ones of said plurality of photosensitive cells;

a horizontal transfer path perpendicular to said plurality of vertical transfer paths and comprising transfer elements arranged in a horizontal direction for transferring the signal charges fed from said plurality of vertical transfer paths;

a plurality of signal reading circuits, one for each one of said plurality of photosensitive cells, for shifting the signal charges from said plurality of photosensitive cells to said plurality of vertical transfer paths, offset from said plurality of photosensitive cells; and

charge sweeping circuitry for sweeping out needless ones of the signal charges stored in said plurality of photosensitive cells;

a mode selecting section for selecting, when an operation for reading the signal charges out of said image pickup section is represented by a mode, either one of an all pixel read mode for reading the signal charges from all of said plurality of photosensitive cells and a particular pixel read mode for reading only the signal charges representative of the color G;

a drive signal generating section for feeding horizontal and vertical drive signals to said image pickup section, and providing said horizontal drive signals with a period shorter in said particular pixel read mode than in said all pixel read mode; and

a controller for controlling said drive signal generating section in a particular manner in each of said all pixel read mode and said particular pixel read mode.

**2**. An apparatus in accordance with claim **1**, wherein said color separating section has any one of

a G stripe pattern,

a G stripe, RB checker pattern, and

a G stripe, RB full checker pattern in which the color G is arranged in a square lattice while the colors R and B each are diagonally arranged at opposite sides of the color G.

**3**. The apparatus in accordance with claim **1**, wherein the color filters assigned to the colors R and B being arranged diagonally with respect to the color filters assigned to the color G.

**4**. The apparatus in accordance with claim **3**, wherein each of said plurality of photosensitive cells being shifted in position by half a pitch from adjoining ones of said photosensitive cells.

**5**. The apparatus in accordance with claim **1**, wherein said mode selecting section generating a different phase of the horizontal drive signal selected from a plurality of signal levels in response to a horizontal timing signal fed from said drive signal generating section and a control signal fed from said controller.

**6**. The apparatus in accordance with claim **1**, wherein said drive signal generating section includes a horizontal signal driver, wherein the horizontal signal driver includes:

a first plurality of horizontal line drivers configured to output a first set of horizontal output signals based on a horizontal timing signal; and

a second plurality of horizontal line drivers configured to output a second set of horizontal output signals based on an inverted horizontal timing signal,

wherein said horizontal signal driver is configured to output said horizontal drive signals based on said first and second set of horizontal output signals.

**7**. The apparatus in accordance with claim **6**, wherein

a voltage of each said first set of horizontal output signals is one of a first high voltage and a first low voltage,

a voltage of each said second set of horizontal output signals is one of a second high voltage and a second low voltage, and

an order of voltages from highest to lowest is first high voltage, second high voltage, first low voltage, and second low voltage.

**8**. The apparatus in accordance with claim **6**, wherein said horizontal signal driver is configured to output said horizontal drive signals based on

all of said first and second set of horizontal output signals in all pixel read mode, and

a subset of said first set of horizontal output signals and a subset of said second set of horizontal output signals in particular pixel read mode.

**9**. A signal reading method for a solid-state image pickup apparatus including an image pickup section including a color separating section having color filters assigned to three primary colors R, G and B for separating colors of light incident from a desired scene, plurality of photosensitive cells arranged bidimensionally in one-to-one correspondence to said color filters each for transforming light output from a particular color filter to a corresponding signal charge, and charge sweeping circuitry for sweeping out needless ones of signal charges stored in said plurality of photosensitive cells, said image pickup section transferring the signal charges of said plurality of photosensitive cells in a vertical direction, offset from vertical columns of said plurality of photosensitive cells, and then in a horizontal direction; said signal reading method comprising the steps of:

(a) selecting, when an operation for reading the signal charges out of said image pickup section is represented by a mode, either one of an all pixel read mode for reading the signal charges from all of said plurality of photosensitive cells and a particular pixel read mode for reading only the signal charges representative of the color G;

(b) generating drive signals for driving said image pickup section in accordance with said all pixel read mode or said particular pixel read mode selected thereby generating a different phase of a horizontal drive signal being generated in response to a control signal fed for said all pixel read mode or said particular pixel read mode selected;

(c) storing, in said particular pixel read mode, the signal charges derived from the color G in response to said drive signals while sweeping out the signal charges derived from the colors R and B;

(d) effecting a field shift of only the signal charges stored;

(e) vertically transferring, the signal charges derived from the color G and subjected to the field shift; and

(f) horizontally transferring the signal charges vertically transferred at a period shorter than a period of time necessary for the signal charges to be read out in said all pixel read mode.

**10**. A method in accordance with claim **9**, wherein step (b) comprises:

(g) generating first drive signals for storing, in said particular pixel read mode, the signal charges derived from the color G while sweeping out the signal charges derived from the colors R and B;

(h) generating second drive signals for effecting the field shift;

(i) generating third drive signals for vertically transferring the signal charges subjected to the field shift; and

(j) generating drive signals for horizontally transferring the signal charges vertically transferred at a period shorter than a period of time necessary for the signal charges to be read out in said all pixel read mode.

**11**. The method in accordance with claim **10**, wherein said step (j) comprises:

(k) generating a first set of horizontal output signals based on a horizontal timing signal;

(l) generating a second set of horizontal output signals based on an inverted horizontal timing signal; and

(m) outputting said drive signals for horizontally transferring the signal charges based on said first and second set of horizontal output signals.

**12**. The method in accordance with claim **11**, wherein

a voltage of each said first set of horizontal output signals is one of a first high voltage and a first low voltage,

a voltage of each said second set of horizontal output signals is one of a second high voltage and a second low voltage, and

an order of voltages from highest to lowest is first high voltage, second high voltage, first low voltage, and second low voltage.

13. The method in accordance with claim 11, wherein said step (m) comprises outputting said horizontal drive signals based on

all of said first and second set of horizontal output signals in all pixel read mode, and

a subset of said first set of horizontal output signals and a subset of said second set of horizontal output signals in particular pixel read mode.

14. The method in accordance with claim 9, wherein the color filters are assigned to the color G being arranged in vertical stripes, the color filters assigned to the colors R and B are arranged diagonally with respect to the color filters assigned to the color G, and each of the plurality of photosensitive cells are shifted in position by half a pitch from adjoining ones of the photosensitive cells, wherein in the step (e), the signal charges derived from the color G are vertically transferred in a path offset from said vertical column of said plurality of photosensitive cells.

15. A solid-state image pickup apparatus comprising:

an image pickup section including:

a color separating section including color filters assigned to three primary colors R (red), G (green) and B (blue) for separating colors of light incident from a desired scene, the color filters assigned to the color G being arranged in stripes;

a plurality of photosensitive cells arranged bidimensionally in one-to-one correspondence to said color filters each for transforming light output from a particular color filter to a corresponding signal charge;

a plurality of vertical transfer paths each comprising transfer elements arranged in a vertical direction for vertically transferring signal charges fed from adjoining ones of said plurality of photosensitive cells;

a horizontal transfer path perpendicular to said plurality of vertical transfer paths and comprising transfer elements arranged in a horizontal direction for transferring the signal charges fed from said plurality of vertical transfer paths;

signal reading circuitry for shifting the signal charges from said plurality of photosensitive cells to said plurality of vertical transfer paths; and

charge sweeping circuitry for sweeping out needless ones of the signal charges stored in said plurality of photosensitive cells;

a mode selecting section for selecting, when an operation for reading the signal charges out of said image pickup section is represented by a mode, either one of an all pixel read mode for reading the signal charges from all of said plurality of photosensitive cells and a particular pixel read mode for reading only the signal charges representative of the color G;

a drive signal generating section for feeding horizontal and vertical drive signals to said image pickup section, and providing said horizontal drive signals with a period shorter in said particular pixel read mode than in said all pixel read mode; and

a controller for controlling said drive signal generating section in a particular manner in each of said all pixel read mode and said particular pixel read mode,

said mode selecting section generating a different phase of the horizontal drive signal selected from a plurality of signal levels in response to a horizontal timing signal fed from said drive signal generating section and a control signal fed from said controller;

each of said horizontal drive signals output from said drive signal generating section comprising:

first horizontal drive signals different in phase from each other and used as one unit in said all pixel read mode and equal in number to electrodes to which said drive signals are fed in said all pixel read mode; and

second horizontal drive signals different in phase from each other and used as one unit in said particular pixel read mode and two times greater in number than the electrodes used in said all pixel read mode.

16. An apparatus in accordance with claim 15, wherein said second horizontal drive signals have a period which is substantially equal to one half of a period of said first horizontal drive signals.

17. The solid-state image pickup apparatus of claim 15, wherein each of the plurality of the vertical transfer paths is offset from each vertical column of said plurality of photosensitive cells.

18. The solid-state image pickup apparatus in accordance with claim 15, wherein said drive signal generating section includes a horizontal signal driver, wherein the horizontal signal driver includes:

a first plurality of horizontal line drivers configured to output a first set of horizontal output signals based on a horizontal timing signal; and

a second plurality of horizontal line drivers configured to output a second set of horizontal output signals based on an inverted horizontal timing signal,

wherein said horizontal signal driver is configured to output said horizontal drive signals based on said first and second set of horizontal output signals.

19. The solid-state image pickup apparatus in accordance with claim 18, wherein

a voltage of each said first set of horizontal output signals is one of a first high voltage and a first low voltage,

a voltage of each said second set of horizontal output signals is one of a second high voltage and a second low voltage, and

an order of voltages from highest to lowest is first high voltage, second high voltage, first low voltage, and second low voltage.

20. The solid-state image pickup apparatus in accordance with claim 18, wherein said horizontal signal driver is configured to output said horizontal drive signals based on

all of said first and second set of horizontal output signals in all pixel read mode, and

a subset of said first set of horizontal output signals and a subset of said second set of horizontal output signals in particular pixel read mode.

* * * * *

# THE EBS-1
# AN EPROM-BASED SEQUENCER ASIC

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## Abstract

A custom EPLD with a pipelined architecture and several unique features has been built. It is based around three custom EPROM NOR-plane cores, surrounded by both standard and custom cells.

## Introduction

When building large state-machine systems, it is frequently necessary to include a large number of components such as counters, registers, MSI chips and delay lines in addition to PLD devices. In many applications, this is prohibitive owing to size, power, performance and economic constraints; thus, we have built an ASIC (Fig. 1) that replaces all of these components. This ASIC requires a single 5-volt 60 mA supply and was built with a 1.6 uM CMOS process that includes n-channel EPROM transistors [1]. Parts with input clock speeds up to 52 MHz have been obtained and used in several systems, and the two wafers probed so far both have yields exceeding 60%. The die size is 80.1K sq mils (517K sq microns).

## Description

The EBS-1 (Fig. 2) contains the equivalent of two large AND-OR EPLDs. It also contains two counters, 16 state-variable flip-flops, a block of dedicated high-speed logic, and a block of externally adjustable delay elements.

The lower EPLD is part of a state machine, which includes 16 state variables. This EPLD provides decoding to control the two counters, the high-speed logic block, and three D flip-flops which drive output pins. The upper EPLD drives output pins via 24 SR and four D flip-flops. Output pins from either EPLD can also be fed back via the eight external input pins to obtain additional state-variable bits.

### High speed logic

The state machine's 1XCLK is derived from the external 4XCLK by the high-speed logic. The 1XCLK period is normally four 4XCLK periods. This may be extended to six 4XCLK periods by the HICCUP signal which is generated by the lower EPLD. Thus the state machine may have a resolution of two 4XCLK periods, even though the fastest clock rate of the state machine is four 4XCLKs.

The high-speed logic also provides nine other signals at the 1XCLK rate. Four of these signals may be either gated on or forced off by the lower EPLD's flip-flops. The remaining five signals have edges that may be smoothly adjusted with external resistors via the internal delay cells in the ANALOG DELAY block. These delay cells use current mirrors to control the pullup currents (and, hence, rise times) of inverters.

The high-speed logic was designed specifically to provide clocks for external CCD shift registers such as are used in solid-state imagers [2]. It may be used for other applications and could be redesigned either for more generic application or for other specific applications such as DRAM control.

### EPROM cores

The EBS-1 contains three EPROM-based wired-NOR cores. One of these cores forms the equivalent of two interleaved AND planes, and the two remaining cores each form the equivalent of OR planes. The net result is two AND-OR EPLDs, each with 50 inputs, 64 minterms, and 52 outputs. The

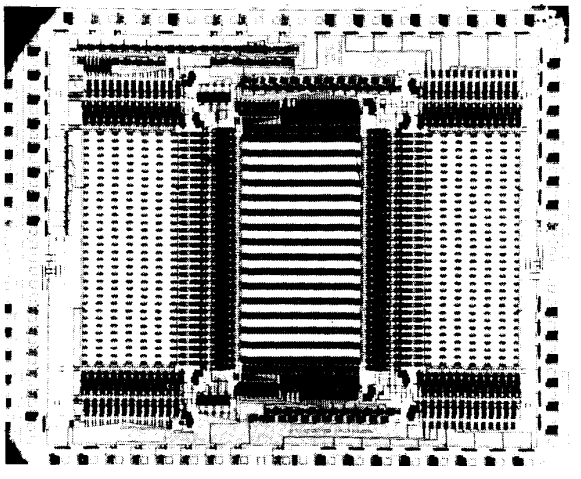

**Fig. 1: EBS-1.1.1 Die Photograph**



CH2584-1/88/0000-0093 $1.00 © 1988 IEEE

inputs to both of these EPLDs are common, but the two EPLDs' minterms and outputs are independent. It should be noted that because these EPLDs are actually formed of NOR planes, the "AND" plane inputs must be interchanged with their complements and the "OR" plane outputs must be complemented in order to provide the equivalent to the traditional AND-OR architecture. To obtain maximum speed, pipeline registers are inserted at all inputs, minterms, and outputs of these EPLDs. Scan-in flip-flops are used for the pipelines, in order to facilitate programming and readback of the EPROM [3].

EPLD circuit

A simplified schematic of an EPLD NOR plane is shown in figure 3. If any word line that intersects an unprogrammed bit line EPROM transistor is high, that transistor will turn on and pull the bit line low, realizing a wired-NOR function. When an EPROM transistor becomes programmed, its threshold voltage becomes too high to allow a word line to ever turn on the EPROM transistor during normal voltage (read) operation. Thus, a given bit line will realize the wired-NOR function of only those intersecting word lines whose EPROM transistors are unprogrammed. The EPROM transistors are programmed in the usual fashion by simultaneously applying high voltages to the gate and drain [4].

Care must be taken to limit the bit line pullup voltage during read operation to no more than 2 volts; otherwise, unwanted programming of the EPROM transistors may occur over extended time periods. Due to the slow rise time, the low pullup voltage, and the relatively high voltage of a bit line with only one EPROM transistor turned on, the difference between a logic 1 and a worst-case logic 0 will be only a few hundred millivolts, requiring differential amplifiers to be used for sensing the states of the bit lines. These sense amplifiers must have a common-mode range that extends below a single EPROM transistor's "on" voltage and must have an accurate reference voltage that tracks both the EPROM "on" voltage as well as the bit line pullup voltage.

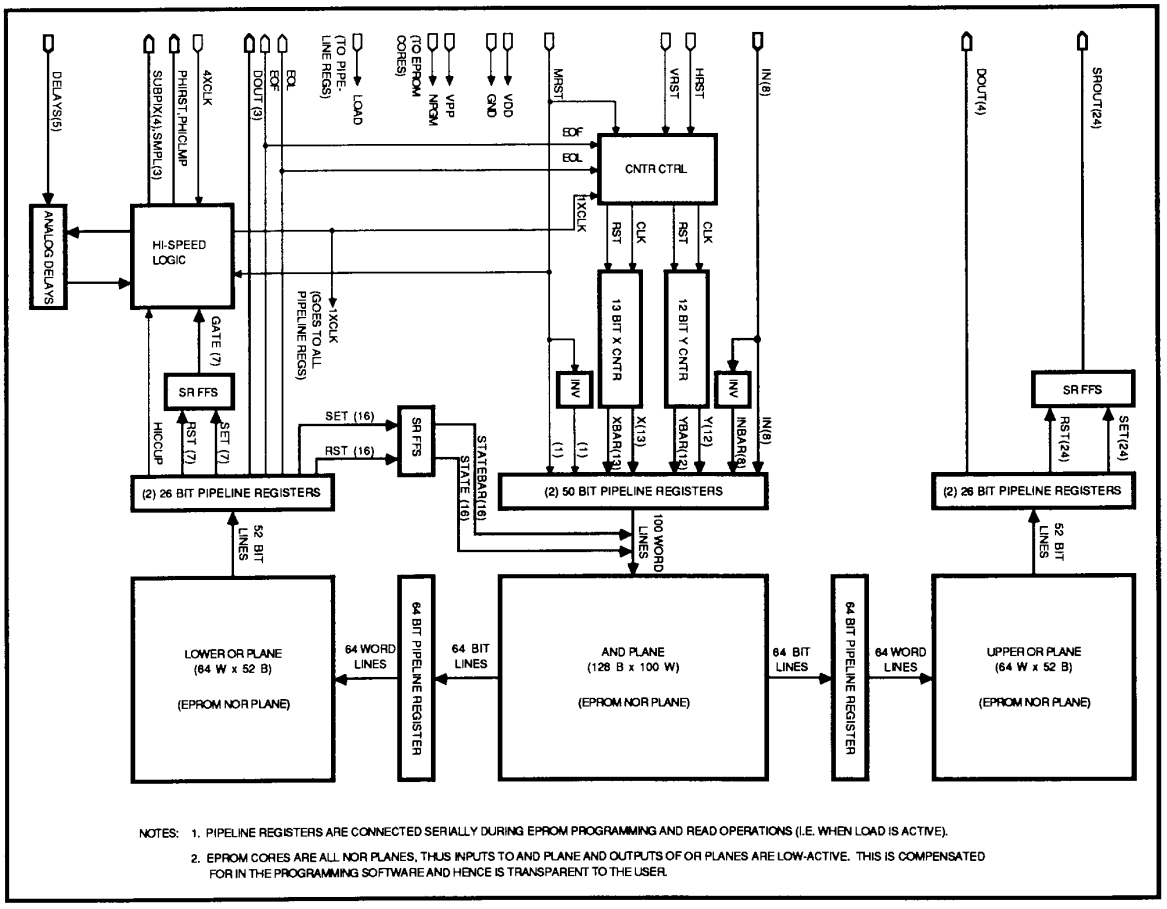


**Fig. 2: EBS-1 Block Diagram**

In EPROM (memory) arrangements, address decoding allows many bit lines to be multiplexed to one sense amplifier; thus, an elaborate design may be used for the sense amplifier. In EPLD arrangements, the outputs of all the bit lines must be sensed simultaneously, requiring a sense amplifier for each bit line. Also, a high voltage driver is required on each bit line for use during programming. Because of this, the bit line pitch is determined by the sense amplifier and high voltage driver pitch rather than by the EPROM transistor pitch. Similarly, the word line pitch is determined by the pitch of the word line drivers. Thus, to minimize die size, word lines are interleaved from opposite sides of each core and bit lines are also interleaved from the two remaining sides of each core, where possible, so that the drivers and sense amplifiers may be placed on all four sides of each core, rather than on just two adjacent sides.

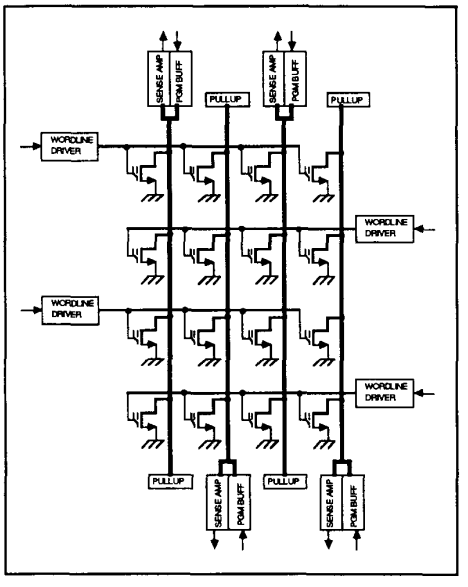


**Fig. 3: EPLD NOR Plane**

## Using the EBS-1

### Programming

The ease in programming the EBS-1 allows rapid and painless implementation of system changes. EBS-1 devices are programmed in minutes with a low-cost PC-compatible programming box and software, and are easily erased in a few minutes with a standard UV EPROM erasing lamp. The data base is in a text format that is easily edited by someone who is familiar with PLDs.

### Voltage Levels

All inputs (except the five delay controls) are standard CMOS inputs. The delay controls are each to be connected through external resistors (10K - 1 Meg ohms) to VSS, with the larger resistor values corresponding to longer delays. All outputs are synchronous to the internal 1XCLK and are standard push-pull CMOS drivers.

For normal operation, VDD and the programming voltage, VPP, are both tied to +5V. However, during programming the programming box supplies +12.5V pulses with controlled rise and fall times to VPP. No other voltages are required to operate or program the EBS, and normal operating current at a 4XCLK rate of 50 MHz is 60 mA (measured).

### Logic Considerations

A master reset input is provided that asynchronously resets both counters, synchronously resets the 1XCLK generator in the high-speed logic, and goes into both EPLDs. Separate reset inputs for the two counters (HRESET and VRESET) are also provided. The counters may also be reset by the EOL and EOF signals that are generated by the lower EPLD. Because the 4XCLK is external and there are three external reset lines (as well as the eight external inputs), it is very simple to synchronize the EBS-1 logic to an external system.

The EPLDs in the EBS-1 differ from common PLDs in that they have internal pipelines. The delays of these pipelines must be considered when using the EBS-1.

### Testing

The EBS-1 makes extensive use of scan-path pipeline registers; thus, it is inherently testable. These registers were required in order to facilitate programming and readback of the EPROM transistors; thus, all of the "OR" plane EPROM transistors are easily tested. Due to an oversight in the scan-path control logic design, in certain cases the "AND" plane is not easily read back, but this will be corrected in any future iterations of the design. The remaining logic to be tested has many connections either to external pins or to the scan-path, and so it is easily tested.

The scan-path is 332 elements long, and each shift of the scan-path requires four test vectors (because each shift clock requires four external 4XCLK cycles); thus, a single load/unload of the scan-path requires 4 x (332 + 1) = 1332 test vectors. Many load/unload sequences must be performed, resulting in a large number of test vectors; therefore, testing is done in three steps.

Pre-programming test. A short test sequence is used at both wafer and package level to test unprogrammed EBS-1 devices. This sequence verifies the I/O cell connectivity and DC parameters, the scan-path, and all of the logic exclusive of the EPROM cores. It also verifies that all bits in the two "OR" planes are initially unprogrammed.

Speed test. This test sequence may be done at both wafer and package level. It programs the

slowest bit lines in both the "AND" plane and the upper "OR" plane, then uses these bit lines in a test that measures the maximum speed at which each EBS-1 will operate. Because only a few bits may be programmed per programming cycle and each cycle takes over 1300 test vectors, this test sequence takes several minutes per device. Other than speed failures, insignificant yield loss occurs with this test; thus, this test may be eliminated if only slower parts are needed and post-programming testing is done later.

Post-programming test. The third testing step (done only on packaged parts) is to program and readback the EPROM cores. This is not done on a tester because of the excessive programming time and number of test vectors required; instead, it is done with a dedicated programming box (which may be used in a ganged configuration) and a personal computer. Again, the AND plane is not easily read back. However, after programming either "golden part", signature analysis [5] or conventional testing methods may be used to verify correct programming.

## Improvements

There are several improvements that could be made in subsequent iterations. The first of these would be to correct the AND plane readout problem, use multiple scan paths, and to connect the 4XCLK directly to the 1XCLK during scan-path shifting. These improvements would greatly improve the programming and test times.

The EPROM cells could be redesigned using approaches such as multiple transistor memory cells or precharge techniques to improve speed as well as to reduce the sensitivity to read current variations. Because the cores are limited by the pitch of the peripheral circuitry, a more complex memory cell should not increase die size. It would also be easy to add a security bit as well as serial number bits to the EPROM. A ROM version of the EPROM cores would be easy to design, and would provide significant cost savings for those high-volume applications where EPROM is not a requirement.

The basic NOR plane core (including the scan-path pipeline registers) could be made available as a standard cell, as either configurable or silicon-compiled cells or as a discrete part. The present EBS-1 design could be modified for specialized applications by customizing the high-speed logic.

## Applications

The range of applications for the EBS-1 is large, such as in system consolidation of several PLDs and EPLDs, in DRAM controllers, and in digital encryption and decryption systems. It is especially useful in all manner of video system controllers and clock generators (the function for which it was originally conceived).

## Conclusions

The EBS-1 has been used successfully in several different video applications and is not limited to any particular television standard. It has potential use in a wide range of other applications. The EBS-1 reduces the time to implement a system change from weeks to just minutes, and it provides an order of magnitude improvement in level of system integration over present EPLDs.

## Acknowledgements

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