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- (54) **DATA INTERLEAVER AND METHOD OF INTERLEAVING DATA**
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- (\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(57) **ABSTRACT**

Interleaving of data symbols comprises permuting rows and columns of a matrix of  $N_r$  rows and  $N_c$  columns, in which data symbols to be interleaved are represented row by row, in accordance with:

Row Permutation	$I_r(k) = [\alpha_r k + f_c(l)] \bmod N_r$
Column Permutation	$I_c(l) = [\alpha_c l + f_r(k)] \bmod N_c$

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- (52) **U.S. Cl.** ..... **714/756; 714/701**
- (58) **Field of Search** ..... **714/756, 755, 714/701, 702**

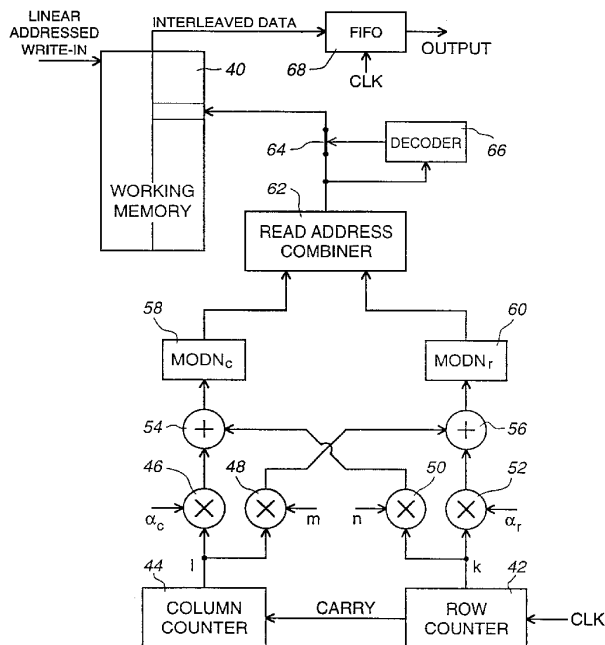
where  $I_r(k)$  represents a data symbol with a row index  $k$ ,  $k$  is an integer from 1 to  $N_r$ ,  $\alpha_r$  is an integer,  $f_c(l)$  is a non-zero function of a column index  $l$ ,  $l$  is an integer from 1 to  $N_c$ ,  $I_c(l)$  represents a data symbol with the column index  $l$ ,  $\alpha_c$  is an integer,  $f_r(k)$  is zero or a function of the row index  $k$ , and  $\bmod N_r$  and  $\bmod N_c$  represent modulo- $N_r$  and modulo- $N_c$  arithmetic respectively, interleaved data symbols being derived from the matrix column by column. A data interleaver comprises a memory for sequentially storing data symbols to be interleaved and a relatively simple circuit for determining read addresses for the interleaved data symbols. The data interleaver is particularly suited for channel interleaving in a 3rd generation CDMA wireless communications system.

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**37 Claims, 2 Drawing Sheets**



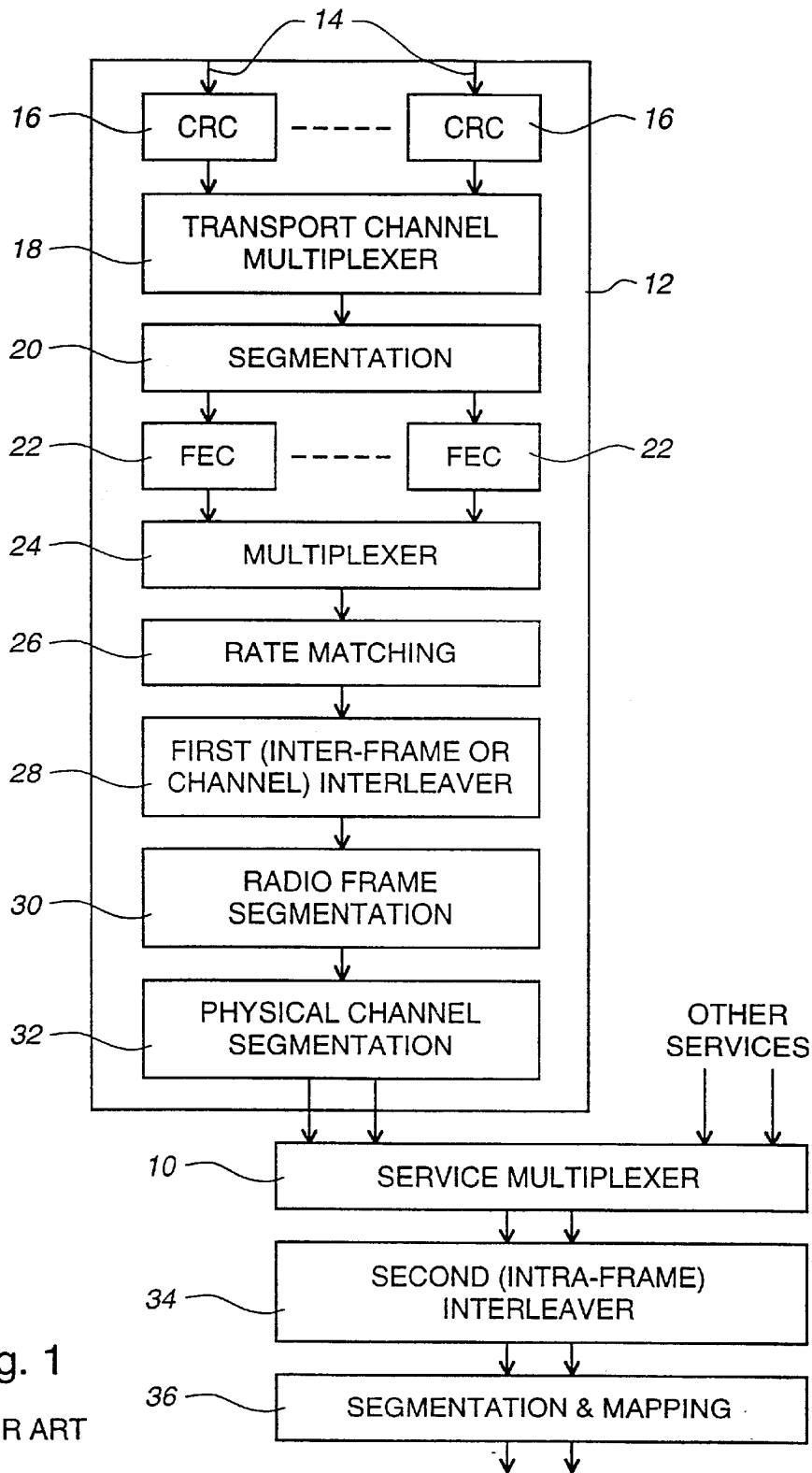


Fig. 1  
PRIOR ART

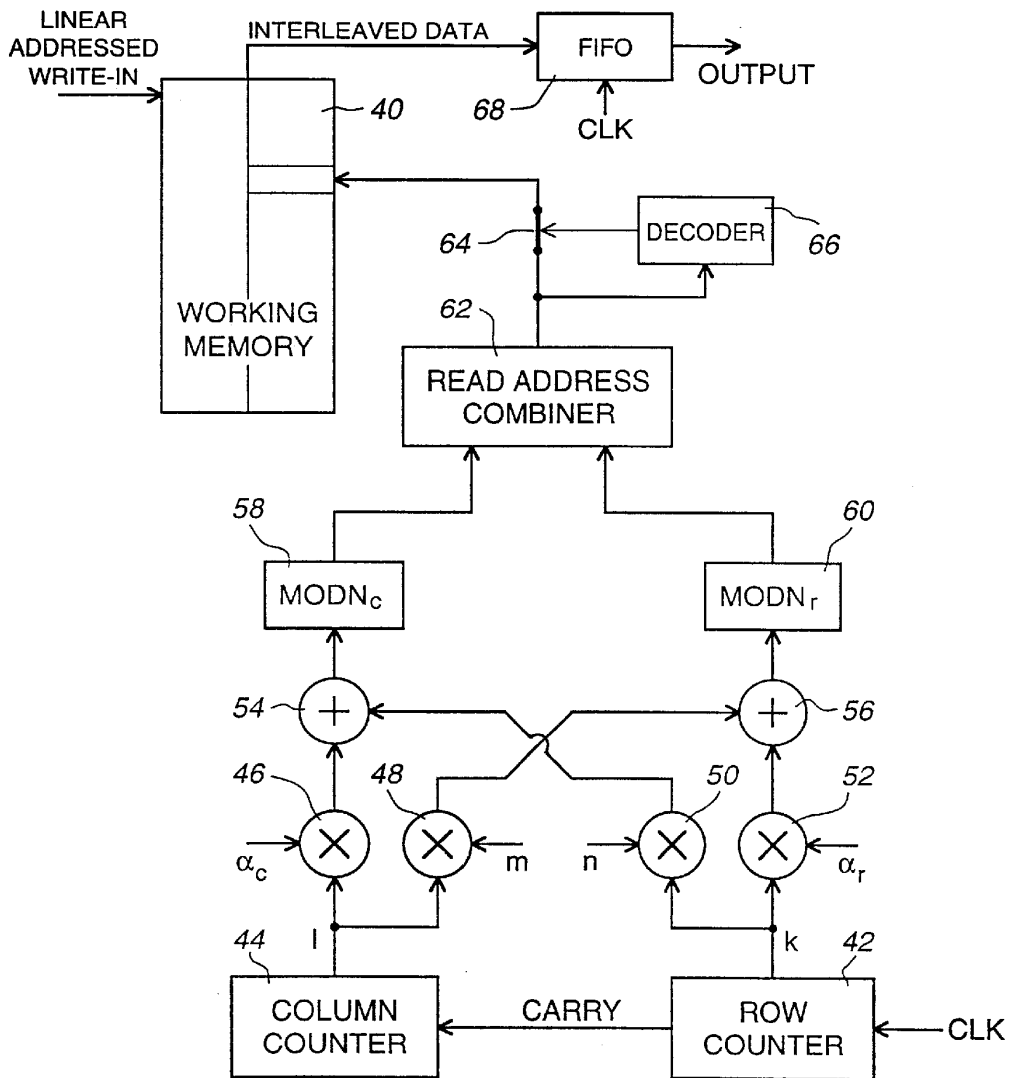


Fig. 2

**DATA INTERLEAVER AND METHOD OF INTERLEAVING DATA**

This invention relates to data interleavers and to methods of interleaving data symbols, and is particularly concerned with a so-called channel interleaver for interleaving data symbols in a communications system.

**BACKGROUND**

It is well known to perform interleaving of data in a communications system using forward error correction (FEC) in order, on deinterleaving, to distribute errors to facilitate their correction. Typically, such interleaving uses a block interleaver to interleave blocks of data. So-called turbo coding (parallel concatenated convolutional coding) uses an interleaver between inputs to two convolutional coders which produce respective parity bits from the input data before and after interleaving. With increasing attention being given to the use of turbo coding, particularly in wireless communications systems, attention has also been given to the form of the interleaver.

So-called 3rd generation CDMA (code division multiple access) wireless communications systems are also being developed which require a channel or inter-frame interleaver which operates to interleave or permute data in blocks corresponding to the radio frame duration, typically 10 ms. For example, a multi-stage block interleaver (MIL) has been proposed for channel (inter-frame) interleaving and for intra-frame interleaving.

However, in such systems the channel interleaver either precedes or follows a rate matching function which serves to match various data rates to the radio frame rate, and which typically involves puncturing (omission) of data symbols. It is necessary to avoid consecutive puncture of adjacent data symbols of coded blocks of data symbols, but the multi-stage interleaver suffers from a problem in this respect. A so-called potential puncturing grid (PPG) concept has been proposed to correct this problem, but the choice of an appropriate PPG depends on variables such as the frame size, number of frames, puncturing rate, and puncturing position.

Accordingly, it would be desirable to provide an interleaver which maximizes the distances by which adjacent punctured data symbols are separated, for arbitrary puncturing rates and puncturing positions, without any PPG.

An object of this invention is to provide an improved data interleaver and method of interleaving data symbols.

**SUMMARY OF THE INVENTION**

According to one aspect, this invention provides a method of interleaving data symbols comprising permuting rows and columns of a matrix of  $N_r$  rows and  $N_c$  columns, in which data symbols to be interleaved are represented row by row, in accordance with:

Row Permutation	$I_r(k) = [\alpha_r k + f_c(l)] \text{ mod } N_r$
Column Permutation	$I_c(l) = [\alpha_c l + f_r(k)] \text{ mod } N_c$

where  $I_r(k)$  represents a data symbol with a row index  $k$ ,  $k$  is an integer from 1 to  $N_r$ ,  $\alpha_r$  is an integer,  $f_c(l)$  is a non-zero function of a column index  $l$ ,  $l$  is an integer from 1 to  $N_c$ ,  $I_c(l)$  represents a data symbol with the column index  $l$ ,  $\alpha_c$  is an integer,  $f_r(k)$  is zero or a function of the row index  $k$ , and  $\text{mod}_{N_r}$  and  $\text{mod}_{N_c}$  represent modulo- $N_r$  and modulo- $N_c$

arithmetic respectively, interleaved data symbols being derived from the matrix column by column.

Preferably  $f_c(l) = ml$  where  $m$  is an integer; for example  $m$  is 1 or is approximately equal to  $N_r/N_c$ . If  $f_r(k)$  is not zero, then preferably  $f_r(k) = nk$  where  $n$  is an integer; for example  $n=1$ . Conveniently  $\alpha_r$  is the largest prime number less than  $N_r/2$ , and  $\alpha_c$  is the largest prime number less than  $N_c/2$ .

The actual number of data symbols to be interleaved need not be exactly equal to  $N_r N_c$  but can be a little less than this, in which case preferably the method further comprises the step of determining one or more matrix positions in which data symbols to be interleaved are not represented, interleaved data symbols not being derived from such determined matrix positions.

The invention also provides a data symbol interleaver arranged for carrying out a method as recited above.

Another aspect of the invention provides a data interleaver comprising: a memory arranged to sequentially store up to  $N_c N_r$  data symbols to be interleaved at respective addresses, where  $N_c$  and  $N_r$  are integers greater than 1; a counter arranged to provide an index 1 from 1 to  $N_c$ , and a counter arranged to provide an index from 1 to  $N_r$  for each value of the index 1; a circuit arranged to determine a first value  $[(\alpha_c l + nk) \text{ mod } N_c]$  and a second value  $[\alpha_r k + m] \text{ mod } N_r$ , where  $\alpha_c$ ,  $\alpha_r$ , and  $m$  are positive integers and  $n$  is a positive integer or zero, and  $\text{mod}_{N_r}$  and  $\text{mod}_{N_c}$  represent modulo- $N_r$  and modulo- $N_c$  arithmetic respectively; and an address combiner arranged to combine the first value as a more significant part and the second value as a less significant part of a read address for reading interleaved data symbols from the memory.

The data interleaver can further comprise an address decoder responsive to at least one read address produced by the address combiner at which a data symbol to be interleaved is not stored in the memory for inhibiting reading from the memory from such address. In this case conveniently the data interleaver further includes a first-in, first-out buffer arranged to buffer interleaved data symbols read from the memory.

The invention further provides a channel interleaver for a communications system including a data rate matching circuit which performs puncturing of data symbols, comprising a data interleaver as recited above.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The invention will be further understood from the following description with reference to the accompanying drawings, in which:

FIG. 1 illustrates a known arrangement for service multiplexing and channel interleaving in a 3rd generation CDMA communications system; and

FIG. 2 illustrates an implementation of an interleaver in accordance with an embodiment of this invention.

**DETAILED DESCRIPTION**

Referring to FIG. 1, there is illustrated a known arrangement for service multiplexing and channel interleaving in a 3rd generation CDMA radio communications system. The arrangement includes a service multiplexer 10 which serves to multiplex together a plurality of data signal streams, referred to as main stream services or QoS (Quality of Service) channels, which are supplied via respective service blocks 12 only one of which is illustrated. Each service block 12 is supplied at inputs 14 with a plurality of constituent input signals, which may for example comprise any of various types of signals such as voice, data, and multi-

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media signals. These input signals may have arbitrary transmission rates, frame sizes, and other parameters. The input signals have CRC (cyclic redundancy check) codes added in blocks 16 and are multiplexed together in a transport channel multiplexer 18. The multiplexed signals are segmented, for encoding, in a segmentation block 20, and the segmented signals are subjected to FEC (forward error correction) coding in FEC blocks 22. The encoded signals are multiplexed in a multiplexer 24 and subjected to rate matching (puncturing (deletion) of redundant symbols or repetition (stuffing) of additional symbols) in a block 26 to match the data rate to the radio communications rate (or so-called air rate) with frames of 10 ms duration. Primarily in order to separate adjacent symbols to reduce the adverse effects of errors due to fading in the radio channel, the data symbols are interleaved in a first interleaver 28, which is referred to as a channel or inter-frame interleaver because it operates to permute blocks each of 10 ms of data symbols. Although in FIG. 1 the interleaver 28 is shown following the rate matching block 26, the positions of these functions may be interchanged. For example, these functions may be in the order shown in FIG. 1 for downlink transmission of signals from a central station, and may be in the reversed order for uplink transmission of signals to the central station.

Following the functions 26 and 28, the resulting rate matched and interleaved signals are segmented for radio frames and physical channels in segmentation blocks 30 and 32 respectively to produce the signals for multiplexing by the multiplexer 10. Signals output by the multiplexer 10 are interleaved by a second interleaver 34 the outputs of which are segmented and mapped to dedicated physical channels in a segmentation and mapping block 36 for communications via a CDMA radio communications path in known manner.

The present invention is directed to implementations of the first interleaver 28, and is particularly concerned with providing an implementation of the first interleaver 28 with a performance that is sufficiently good to enable the second interleaver 34 to be omitted or reduced to a simple shuffling operation. This is desirable in particular because the second interleaver 34 has the potential to degrade the interleaving performed by each first interleaver 28, whereas each first interleaver 28 can be optimized for its particular rate matched data stream and QoS. Alternatively, the second interleaver 34 can also be implemented as an interleaver in accordance with an embodiment of this invention, the parameters of both interleavers being chosen to provide an optimized performance of the overall arrangement.

Accordingly, the first interleaver 28 is implemented as an algebraic interleaver providing a good random spreading property which facilitates straightforward rate matching by puncturing and symbol repetition. Accordingly, the multiple encoded symbol blocks for each QoS channel are mapped into a 2-dimensional matrix and are subjected to linear congruential rules to permute the rows and columns of the matrix to implement the interleaving function. A maximum interleaving depth and time span can be determined by searching a set of best parameters. The interleaver consequently has a relatively simple form without disadvantages of known interleavers, such as requiring large memory sizes for look-up tables or inadequately accommodating the rate matching function.

Although the following description refers to rows and columns of a matrix, it should be understood that this is for convenience and clarity, that the rows and columns can be interchanged without changing the function of the interleaver, and that in practice and as described below the interleaver can operate by equivalent control of read or write

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addressing of memory locations of a linear memory in which data symbols are stored, without any actual movement of the stored data symbols among the memory locations.

An interleaver in accordance with embodiments of this invention operates to implement the following steps:

1. Represent a number  $N_c$  of encoded blocks of data symbols each of length  $N_r$ , data symbols as a matrix of  $N_r$  rows and  $N_c$  columns.
2. Permute the rows and columns of the matrix in accordance with:

Row Permutation	$I_r(k) = [\alpha_r k + f_c(l)] \bmod N_r$
Column Permutation	$I_c(l) = [\alpha_c l + f_r(k)] \bmod N_c$

where  $I_r(k)$  represents a data symbol with a row index  $k$ ,  $k$  is an integer from 1 to  $N_r$ ,  $\alpha_r$  is a row permutation parameter and is an integer,  $f_c(l)$  is a positive function of a column index  $l$ ,  $l$  is an integer from 1 to  $N_c$ ,  $I_c(l)$  represents a data symbol with the column index  $l$ ,  $\alpha_c$  is a column permutation parameter and is an integer,  $f_r(k)$  is a positive function of the row index  $k$ , and  $\bmod n_r$  and  $\bmod n_c$  represent modulo- $N_r$  and modulo- $N_c$  arithmetic respectively.

3. Derive interleaved data symbols from the matrix column by column.

In the row permutation of step 2,  $f_c(l) \neq 0$  to avoid puncturing of consecutive data symbols due to the rate matching. For example, the function  $f_c(l) = ml$  where  $m$  is a constant integer, for example  $m=1$  so that  $f_c(l)=l$ . The column permutation of step 2 can use bit reversal as is known in the art, or the function  $f_r(k)$  can be zero. Alternatively, for example, the function  $f_r(k) = nk$  where  $n$  is a constant integer, for example  $n=1$  so that  $f_r(k)=k$ . It can be appreciated that the order in which the row and column permutations of step 2 are performed is arbitrary, i.e. either the row permutation or the column permutation can be performed first, or both permutations can be performed contemporaneously.

In a first embodiment of the invention described below, for example the parameter  $\alpha_r$  is chosen to be the largest prime number less than  $\lfloor N_r/2 \rfloor$ , the parameter  $\alpha_c$  is chosen to be the largest prime number less than  $\lfloor N_c/2 \rfloor$ ,  $m = \lfloor N_r/N_c \rfloor$ , and  $n=0$ . The symbols  $\lfloor \rfloor$  refer to rounding down to an integer.

In this example,  $N_c=8$ ,  $N_r=10$ ,  $\alpha_r=3$ ,  $\alpha_c=3$ ,  $m=1$ , and  $n=0$ . Thus, in step 1, 80 data symbols, identified by the numbers 1 to 80 in the following tables, in eight 10 ms coded blocks each of 10 coded symbols, are represented row by row in a 10 by 8 matrix with the row index  $k$  and the column index  $l$ , as shown by Table 1:

TABLE 1

		1							
		1	2	3	4	5	6	7	8
k	1	1	2	3	4	5	6	7	8
	2	9	10	11	12	13	14	15	16
	3	17	18	19	20	21	22	23	24
	4	25	26	27	28	29	30	31	32
	5	33	34	35	36	37	38	39	40
	6	41	42	43	44	45	46	47	48
	7	49	50	51	52	53	54	55	56
	8	57	58	59	60	61	62	63	64
	9	65	66	67	68	69	70	71	72
	10	73	74	75	76	77	78	79	80

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