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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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[X] *Additional inventors are being named on the* 1 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

SYSTEM AND METHOD FOR ADAPTING A USB TO PROVIDE POWER FOR CHARGING A MOBILE DEVICE

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[ ] Applicant claims small entity status. See 37 CFR 1.27.
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Respectfully submitted,

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REGISTRATION NO. *(if appropriate)* 39,142

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Number 1 of 1

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention

System and Method for Adapting a USB to Provide Power for Charging a Mobile Device

Inventors

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555255-012-132

TITLE OF INVENTION

System and Method for Adapting a USB to Provide Power for Charging a Mobile Device

FIELD OF INVENTION

This invention relates to rechargeable mobile devices having access to a Universal Serial Bus (USB). In particular, this invention relates to adapting power from the USB for use as a power source by the charging system of the mobile device to re-charge the portable power supply of the mobile device.

BACKGROUND OF THE INVENTION

On one hand, the Universal Serial Bus (USB) is a communications bus for connecting a USB host controller such as a computer to peripheral devices. USB peripheral devices can be differentiated based on how they obtain their power in order to operate while connected. A self-powered peripheral has access to a power supply external to USB, whereas a bus-powered peripheral derives all of its power from the USB.

On the other hand, traditional mobile devices usually have a portable power supply that provides power to the mobile device while it is in service. Some portable power supplies are rechargeable so that when power is depleted and the portable power supply becomes discharged, a charging system can be used to restore the charge in the portable power supply. The charging system obtains power from an alternate power source, such as an AC outlet of a home or office electrical network, in order to recharge the portable power supply.

Certain rechargeable mobile devices use a separate charging system such as a docking cradle. Other rechargeable mobile devices integrate a built-in charging system in order to facilitate recharging the portable power supply while it is still installed in the mobile device.

Recently the hitherto separate fields of USB and mobile devices have collided. Certain rechargeable mobile devices have evolved to access USB capabilities in order to become USB peripherals for the purpose of communicating with USB host controllers such as a computer. In some cases, USB capabilities have been incorporated into the docking cradle, whereas in other cases USB capabilities have been integrated into the rechargeable mobile device itself, in a manner analogous to the location of the traditional charging system.

Traditional rechargeable mobile devices having a USB already have access to two power supplies, specifically a portable power supply and an alternate power supply. Therefore USB capable rechargeable mobile devices traditionally operate as self-powered USB peripherals.

There is a need for a system and method of adapting the charging system of a USB capable rechargeable mobile device to use the power traditionally available on the USB as an alternate power source for recharging the portable power supply of the mobile device thereby eliminating the need for a separate charging and USB interfaces.

BRIEF SUMMARY OF INVENTION

It is an object of the invention to provide a system and method of adapting the charging system of a USB capable rechargeable mobile device to use the power traditionally available on the USB as an alternate power source for recharging the portable power supply of the mobile device.

Traditionally, the alternate power supply is of a much greater power capacity than the portable power supply, so that as much current as is needed can be drawn from the alternate power supply by the charging system in order to re-charge the portable power supply.

However, power traditionally available on the USB is 100mA to 500mA at 5V, which sometimes has to be shared amongst up to 127 self-powered peripherals. The exact amount of current available varies as peripherals are connected and disconnected from the USB.

In one embodiment of the invention, a charging circuit directly attached to the USB power lines draws current without regard to traditional USB functionality.

In another embodiment of the invention, a charging circuit uses a current analogous to the current being drawn from the USB on the Vbus rail. Several elements of the invention are provided by an ASIC thereby facilitating manufacture.

In yet another embodiment of the invention, the USB interface accessible to the mobile device isfurther adapted in order to favour two modes of operation: charging mode and communications mode.

Further features of the invention will be described or will become apparent in the course of the following detailed description.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

In order that the invention may be more clearly understood, embodiments thereof will now be described in detail by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram illustrating a non-enumerating embodiment;

Figure 2 is a block diagram illustrating an enumerating embodiment;

Figure 3 is a flowchart illustrating an enumerating method;

Figure 4 is a block diagram illustrating a current sensing embodiment, which can be used for both enumerating and non-enumerating purposes;

Figure 5 is a typical charge and voltage curve which illustrates a current-sensing method; and

Figure 6 is a flowchart which further illustrates a current-sensing method.

DETAILED DESCRIPTION OF THE INVENTION

NON-ENUMERATING EMBODIMENT

In one embodiment of the invention, a Li battery is charged by using the power available at a high-powered USB port, making no use of the D+ and D- data lines. A charger apparatus, such as a linear charger based on the LTC1734 charge controller, is used in this embodiment.

In reference to Figure 1, a USB interface 100 comprising a Vbus power line 100, D+ data line 120, D- data line 130 and GND

power line 140 is connected to a charging circuit 400 via the Vbus 110 and GND 140 power lines. A battery 500, to be charged, is connected at it's positive ent to the charging circuit 400, and at it's negative end to the GND power line 140.

It was determined experimentally that current can be drawn from several USB ports at a high rate, such as 500mA, without problem. As used in this description and in the appended claims, a high-power USB port is a USB port which can provide around 500mA to be drawn by the invention. Typical means of providing a high-power USB port are ensuring that the invention is the only USB device to attach to the USB port of a desktop computer, a laptop computer, or a self-powered hub.

First the charger is attached to the power lines of a high-powered USB port, such as that of a desktop computer. An open voltage value is measured on the USB prior to charging operation. This was about 5.16V in experiments.

Next, the battery is charged by drawing current at a rate of around 490mA.

The start of charge can be detected by observing that the Vbus voltage value settles to a charging voltage value. This was about 4.76V in experiments.

Finally, when the Vbus reaches its open value, the end of charge condition is detected. This was about 5.16V in experiments.

Additionally, when charging from the USB port of a portable computer, such as a laptop, after charging at the same rate (490mA) the Vbus voltage value settled to a charging voltage of about 4.65V. The difference between this laptop charging voltage value and the

desktop charging voltage value can be used to sense what type of high-powered device the invention is attached to.

Furthermore, still in the case of a laptop, the USB voltage disappears when the internal laptop batteries were "completely" discharged. The voltage is present again immediately after the laptop is attached to its charger. Therefore, the invention adapts both the batteries of a laptop and the power adapter of the laptop to provide power to a rechargeable mobile device via the USB port.

Furthermore, it seems that certain high-power USB ports, such as a self-powered hub, appear to implement only an over-current protection, i.e. they turn off the voltage on the Vbus line for current values exceeding 700mA-800mA.

Thus a battery charger limiting its charge current value to 500mA can be powered from a high-power USB port without being necessary to be enumerated by the host, although such a device is not currently compatible with the current USB standard.

ENUMERATING EMBODIMENT

In another embodiment of the invention, the USB interface accessible to the mobile device is further adapted in order to favour two modes of operation: a charging mode and the traditional communications mode. The traditional communications mode of operation of a USB peripheral is described in great detail in the current USB standard and is not discussed presently as it is obvious to a person skilled in the art. Both modes could be operated contemporaneously by a skilled person consulting both the standard and this specification, however this specification will positively set out and describe the charging mode.

In reference to Figures 2, one embodiment of a system used in the charging mode will be described presently in greater detail. In this embodiment, all lines of USB interface 100 are utilized. Specifically, the data D+ 120 and D- 130 lines are utilized to provide data communication between a USB controller (not shown) and a micro processor 200 of the present invention. The microporcessor 200 selectively controls soft-disconnect signal 120 to cause soft-disconnect means means 210, such as a pair of electrically controlled switches to either connect or disconnect the microprocessor from the USB Interface 100. Microprocessor 200 also communicates with power level limiting means 300 via set power level signal 220. The power level limiting means 300, such as the switched current divider formed by a plurality of first resistor 330 and switch 340, and a single second resistor 350, provides a power signal 310, such as a reference current, to charging circuit 400. Charging circuit 400 is connected to power lines Vbus 110 and GND 140, and provides power to an attached battery 500 which is electrically connected at one end to the charging circuit 400, and at the other to the GND line 140 of the USB interface.

In charging mode, the mobile device USB interface operates as a bus-powered peripheral interface, with a temporary disregard to communications functionality in favour of obtaining the maximum amount of current from the USB host controller.

A method of use of the system illustrated in Figure 2 will be described presently, in reference to Figure 3. At step 600, the microporcessor 200 sets power level signal 220 to a minimum value, such as 0 mA. At step 610, the microprocessor sets a requested

power to a maximum value, such as 500mA. At step 620, the microprocessor 200 sends soft-disconnect signal 210 so that a connection to the USB interface is detected by a USB controller, which was not expressly shown in Figure 2.

At step 630, the microprocessor monitors data lines D+ 120 and D- 130 and waits for the enumeration process to begin. At step 640, When connecting, during the enumeration process, the USB host controller obtains a power request from the mobile device USB peripheral interface. However, the USB host controller might not allot the amount requested, and at Step 650 this is determined.

In order to maximize the likelihood of obtaining a large power allotment, the mobile device USB peripheral interface is capable of electrically disconnecting and reconnecting using switches in order to force a new enumeration process as if a user had unplugged and then plugged in the mobile device USB interface to the USB host controller. This is accomplished by steps 670 and 680 respectively, after which the method continues at step 620.

By comparing the amount of power requested and the amount of power allotted, the mobile device USB interface can determine whether or not to disconnect and attempt a request for less power. When the amount of power obtained corresponds with the amount of power allotted, the USB interface can proceed to operate in communications mode. This occurs at step 660, after which the method ends.

In communications mode, one additional element is taught by the invention over a traditional USB device taught by the standard. The mobile device USB interface operates as a traditional USB

peripheral interface favouring traditional communications wherein the mobile device acts as either a self-powered or bus-powered peripheral, depending on the charge state of the portable power supply. If the portable power supply is sufficiently charged, the mobile device can act as a self-powered peripheral bypassing the charging mode. Conversely, if the portable power supply needs to be recharged, the mobile device can disconnect electrically and act as a bus-powered peripheral.

CURRENT SENSING EMBODIMENT

In reference to Figures 4-5, a third embodiment of the present invention will be described. The Charger Current Sense block 710 provides a signal 717 to the Charge Control block 732 analogous to the current being drawn from the USB on the Vbus rail. The Charge Control block 732 uses this signal 717 to turn on the linear pass element 727, such as a bipolar transistor, to a greater or lesser degree by signal 727 as necessary in order that the total current does not exceed that required by the system. In the case of USB, this is for example either 100mA or 500mA. In addition and as a parallel control, the Charge Control block 732 monitors the battery voltage level via the V_BAT 750 input, and controls the input current via the linear pass element 720 such that the battery voltage does not exceed the specified maximum, such as for example 4.20V. The Charge Control 732 block periodically inhibits delivery of current to the battery by switching off the linear pass element 720, and briefly monitoring the battery level at V_BAT 750. This information is used to determine whether the linear pass element 720 should control solely the input current, such as monitored by the Charger Current

Sense block 710, or the input current and the battery voltage during the following "charge on" cycle, which will be described in further detail in reference to Figure 5 below.

In the absence of input power at the Vbus 110, the Charge Control block 732 sets the switch 720 so that the first regulator 736 and second regulator 738 connect to and draw power from the battery 500 via the V_BAT 750 input.

In order that the microprocessor 740 can monitor and control the charge system operation, the actual current delivered to the battery 500 is monitored by the Cell Current Sense block 760. This block produces a signal ISENSE_BAT 755 that is analogous to the actual charge current, and which is converted by an analog-to-digital converter, which is not explicitly shown in the drawing but is comprised in Charge Control block 732, and which may be read serially by the microprocessor on a serial interface, which is also not shown explicitly in the drawings.

In order to favour manufacturing, a specification for an ASIC 730 to be known as Esker is provided in an appendix. The ASIC device performs charging, battery monitoring, low dropout voltage regulation, system reset control, and integration of a few other power consuming functions such as proximity sensor, vibrator, and buzzer.

LDOs 736,738 are Low Drop-Out regulators. An LDO is typically a linear regulator that can manage to keep its output within regulation tolerance, while the input falls to only a small amount above the output voltage. Note that regulator 738 may be a buck switching regulator external to Esker, as it might need to supply more current than a linear regulator could handle without overheating.

In an embodiment using Esker, charge termination will be performed by the microprocessor, as the charge current will be monitored.

Note that the Charge Control block 732 also operates an electronic switch 727 when voltage is detected at the Vbus input 110. This switch diverts power as necessary from the source to operate the regulators 736.738 powering the microprocessor 740, in order to ensure that it is possible, even in the case of a severely discharged lithium battery 500, that the necessary communications and charge management functions may be performed.

One significant innovation in the configuration illustrated in Figure 4 is that the controlled parameter is system input current, rather than battery charge current. Varying of the battery charge current is used as the means for controlling (limiting) the system input current, thereby compensating for varying power drawn by the microprocessor.

In reference to Figure 5, a "periodic charge" and "battery voltage compensation" method using the system of Figure 4 is illustrated in great detail. A battery voltage curve 800 and battery current curve 900 which illustrate the method of charging are depicted. A constant charge current 910, such as in this example 500mA, is delivered to the battery until during a constant charge current period 1000, for instance during the first five constant charge current cycles 1010A,B,C,D,E in the figure. Between each cycle, the current is stopped 920A,B,C,D,E,F and the battery voltage 820A,B,C,D,E,F (which climbs during charging) is measured. At the end of the constant charge current period 1000, the voltage

820A,B,C,D,E is sampled to be at or above a critical threshold, such as 4.2V 820F. In the next cycles 1510A,B,C,D, the charge current is regulated such that the voltage 830 stays approximately constant during a constant voltage period 1500. When the sampled current 930A,B,C reaches a cirtical threshold, such as 50mA 930D, the charging method finishes. The current is still set to zero between constant current charging cycles 935A,B,C,D.

This method is illustrated further in Figure 6 with a flowchart. At step 1020, the charge current is set to zero. This corresponds to points 920 of Figure 5. At step 1030, the voltage is sampled 820. At step 1030, the sampled voltage is compared to a threshold, such as 4.20 V. In the event that the sampled voltage is below the threshold, at step 1050 a constant current charging cycle as described above in reference to Figure 5 ensues, aftewhich the method continues at step 1020. However, in the event that the sampled voltage is determined to be above or equal to the threhold at step 1030, the method continues at step 1520 in constant current charging mode 1500. At step 1520, a constant current charge cycle, as described above in reference to Figure 5 ensures. At step 1530, the current 930 is sampled. At step 1540, the current 935 is set to zero. At step 1550, the sampled current 930 is compared to a threshold. In the event that the current is greater than the threshold, the method continues at step 1520. In the event that the sampled current 930 is below the threshold, the method ends.

It will be appreciated that the above description relates to embodiments by way of example only. Many variations on the invention will be obvious to those knowledgeable in the field, and

such obvious variations are within the scope of the invention as described and claimed, whether or not expressly described.

CLAIMS

ABSTRACT

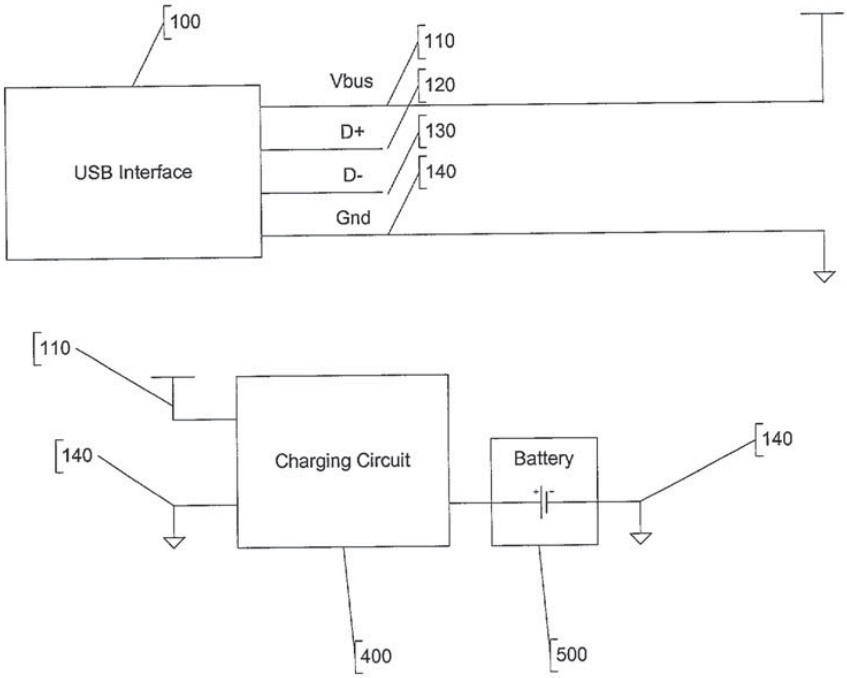

Figure 1

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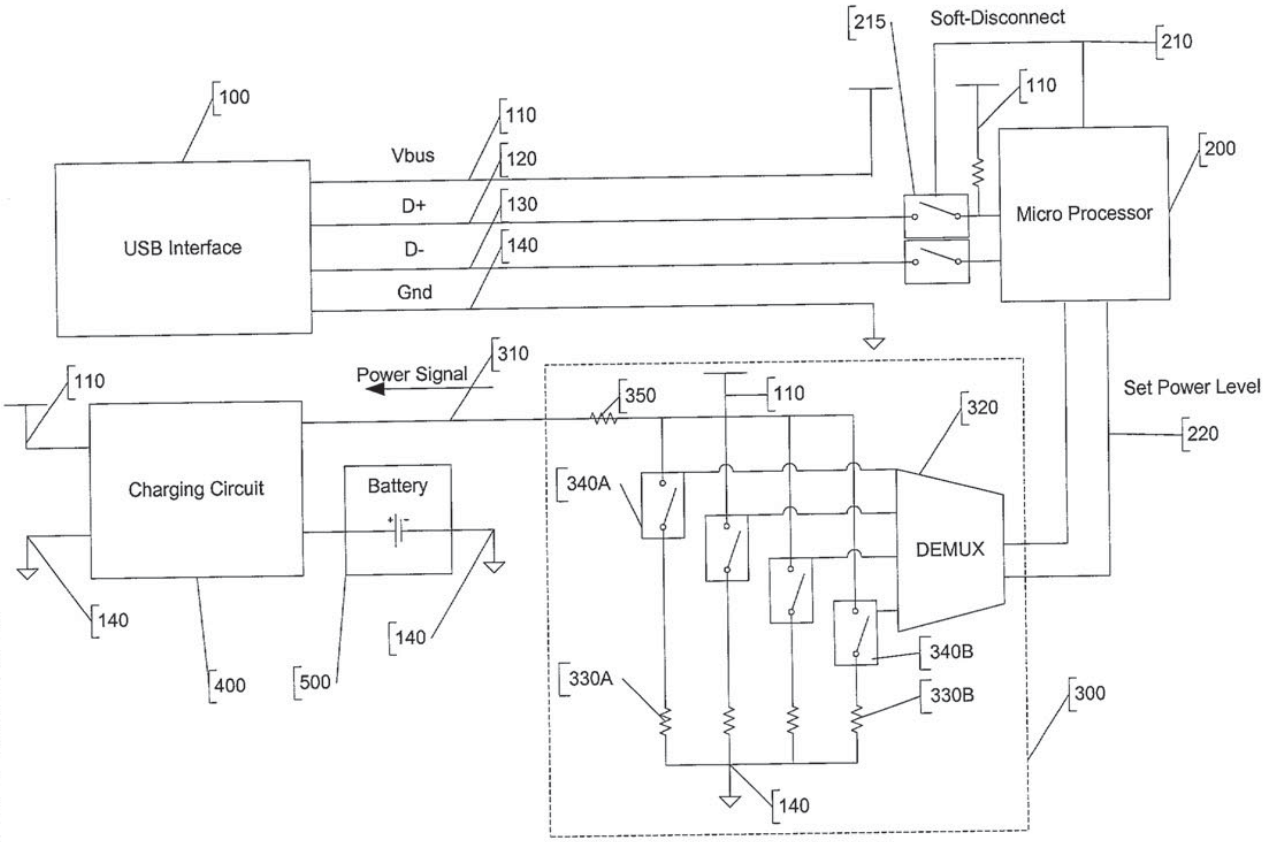

Figure 2

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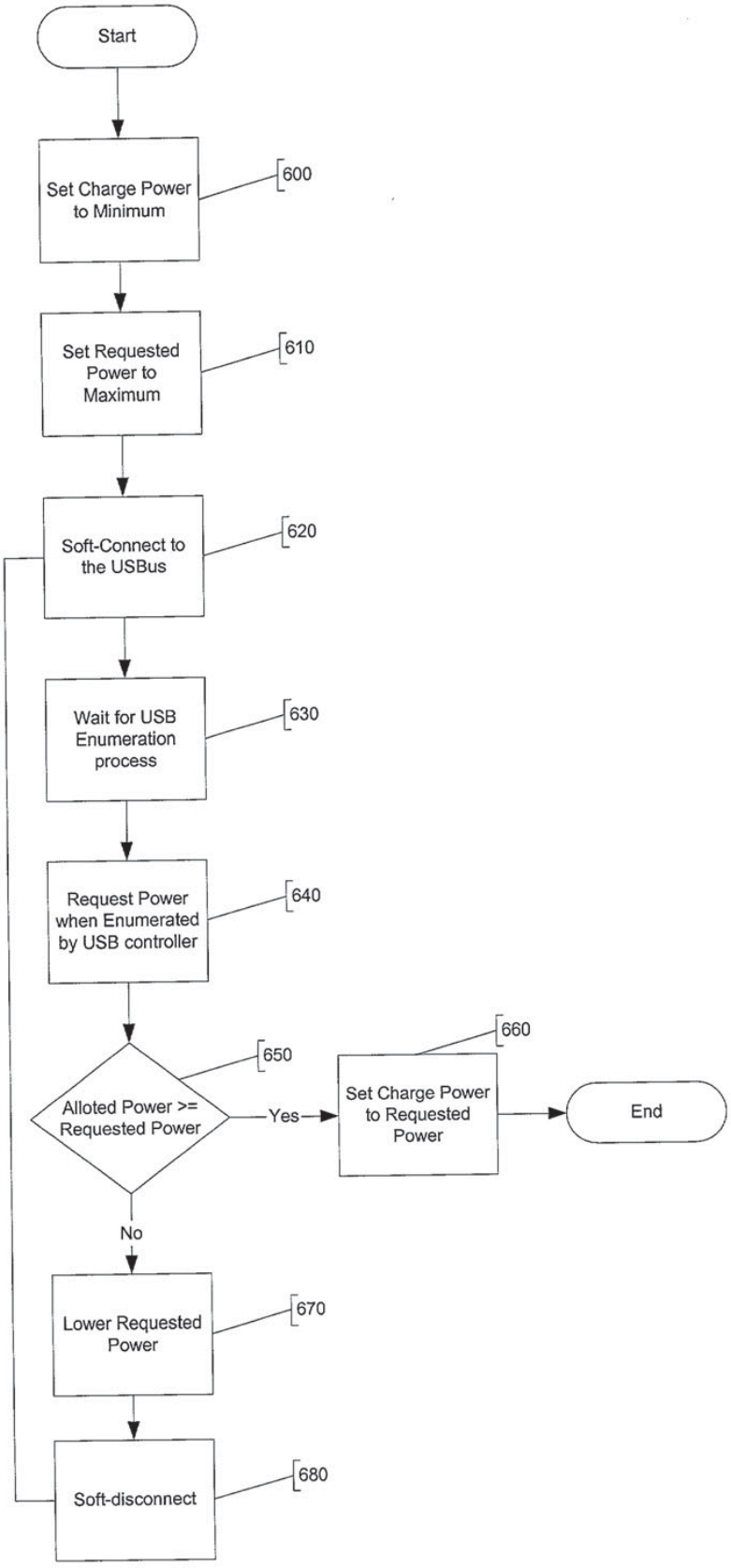

Figure 3

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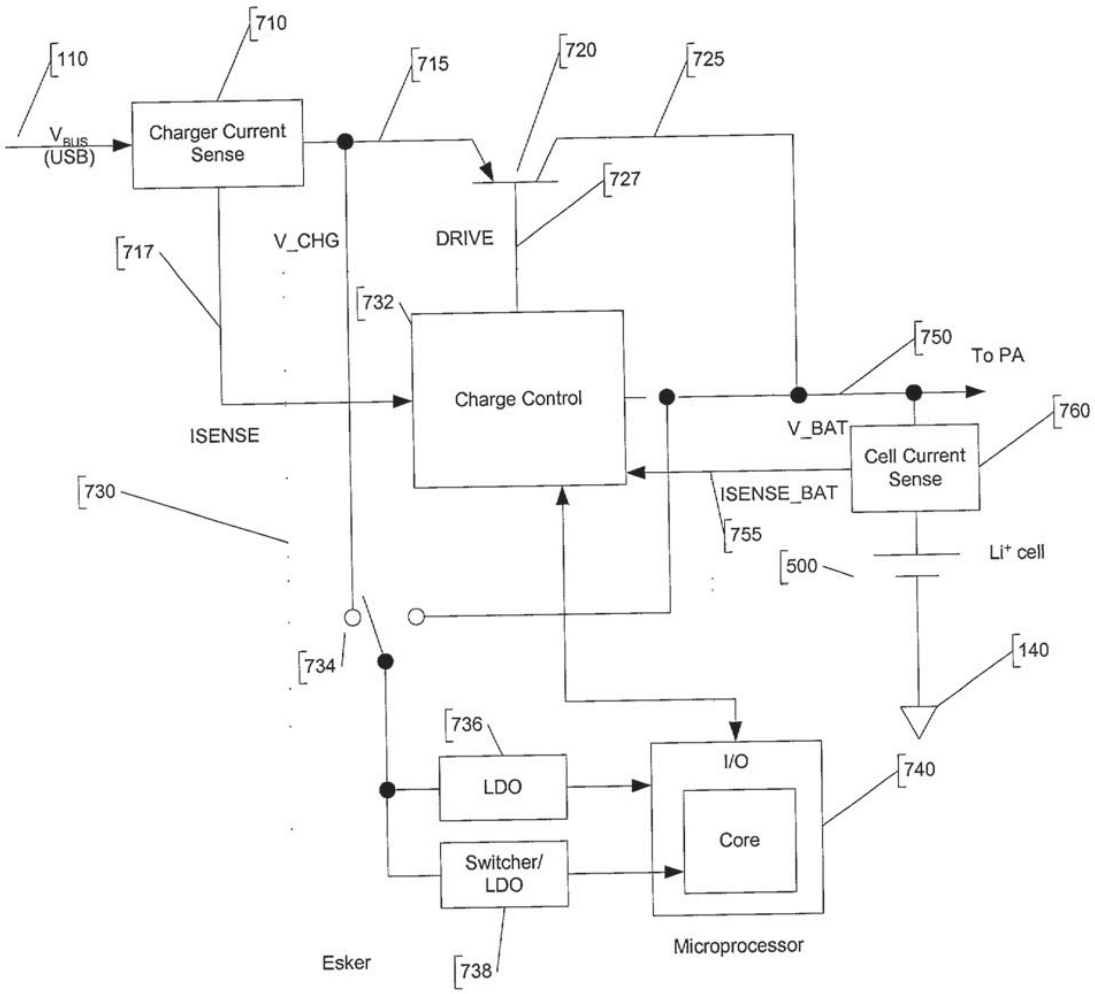

Figure 4

555255-012-132

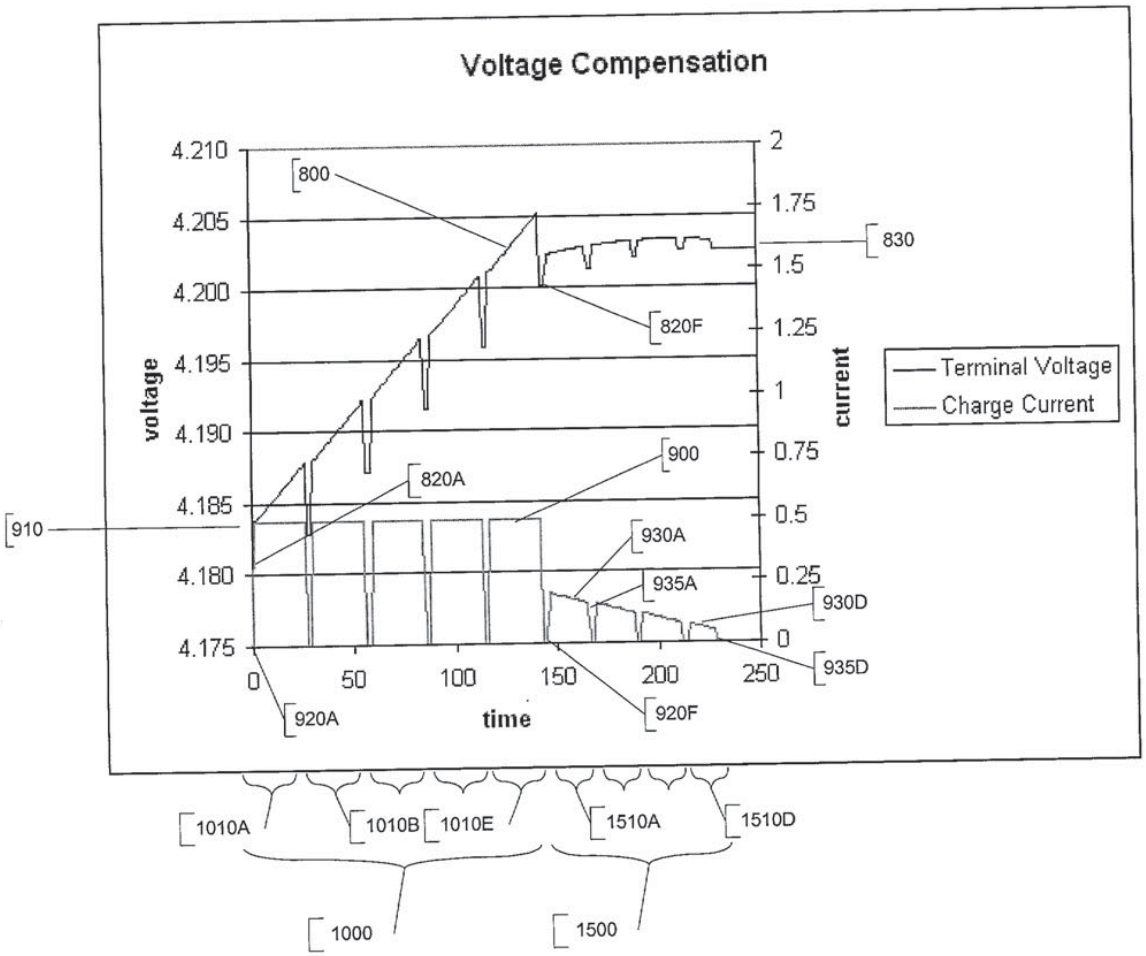

Figure 5

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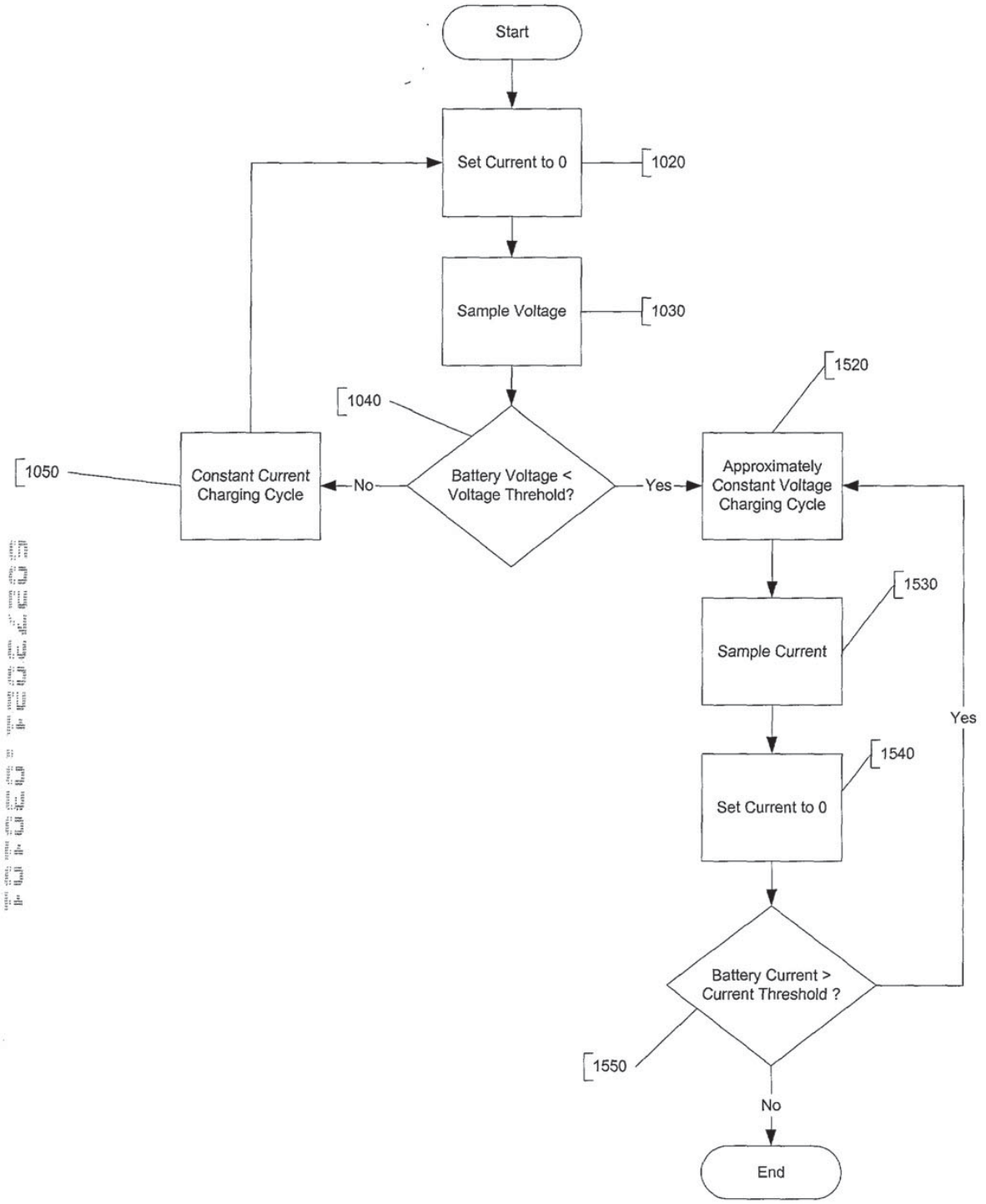

Figure 6

555255-012-132

Attorney Docket No. 555255012132 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Daniel M. Fischer Dan G. Radut Michael F. Habicher Quang Luong Jonathan Malton
Application No.:	Not Yet Assigned
Filed:	Herewith
For:	SYSTEM AND METHOD FOR ADAPTING A USB TO PROVIDE POWER FOR CHARGING A MOBILE DEVICE

POWER OF ATTORNEY FOR PROVISIONAL APPLICATION

Each inventor, identified above and signing below, hereby appoints each of the following as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Author:	Mike Habicher, mikeh@rim.net, x2207
Date:	16-Feb-2001
Document:	03126002, rev B
Vendor:	
Vendor Part #:	

Esker ASIC Specification

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4 Document History

5 Introduction

5.1 Scope

This document defines the requirements for an ASIC that provides power management functionality for a low power two-way wireless PDA.

Any information and data contained in this document is subject to change by Research in Motion, Ltd. (RIM).

Deviations from the specifications contained in this document are subject to approval by RIM.

5.2 Technical Contacts

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5.3 Functional Description

The power supply ASIC performs the following primary functions:

1. Monitor and control charging of the lithium-ion (Li^+) cell;
2. Provide several regulated voltage outputs to the PDA systems;
3. Provide the necessary drive circuitry for the PDA annunciators;
4. Provide voltage translation for the Subscriber Identity Module (SIM) interface.

5.4 References

The following documents form part of this specification to the extent specified herein:

1. EIA/JESD22-A114-A "Electrostatic Discharge (ESD) Sensitivity Testing/Human Body Model (HBM)", Electronic Industries Association.
2. EIA/JESD78 "IC Latch-Up Test", Electronic Industries Association.
3. GSM 11.11 "Specification of the Subscriber Identity Module–Mobile Equipment (SIM-ME) Interface", European Telecommunications Standards Institute, France.
4. GSM 11.12 "Specification of the 3 Volt Subscriber Identity Module–Mobile Equipment (SIM-ME) Interface", European Telecommunications Standards Institute, France.
5. JESD22-C101 "Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components", Electronic Industries Association.
6. Universal Serial Bus Revision 2.0 Specification, USB Implementers Forum, Oregon.

6 Requirements

6.1 General

6.1.1 Block Diagram

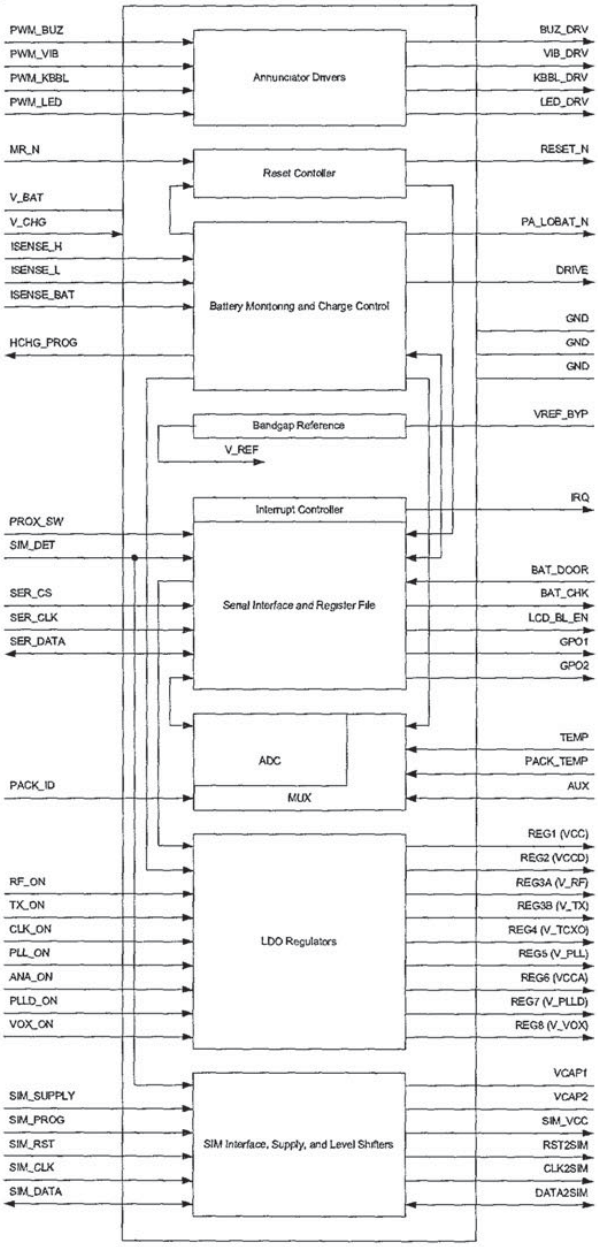

Figure 6-1: Esker ASIC Functional Block Diagram

6.1.2 Pin Descriptions

The symbols listed in the Type column of Table 6-2 are defined in Table 6-1 below.

Table 6-1: Key to Pin Types

Code	Description
A	Analog signal
B	Bidirectional
D	Digital signal. See 7.2.
I	Input
O	Output
P	Power
-pu	Pull-up
-pd	Pull-down

All signals listed as digital ("D") in Table 6-2 will be CMOS-compatible and referenced to REG1. See the Electrical Characteristics section for details.

Table 6-2: Pin Descriptions, Grouped by Function

Type	Pin Name	Description	#
LDO Control Signals			
DI	ANA_ON	Active-high logic signal to enable REG6 (VCCA). See 6.2.11.6.	
DI	CLK_ON	Active-high control signal to enable REG4 (V_TCXO). See 6.2.11.4.	
DI	PLL_ON	Active-high control signal to enable REG4 (V_TCXO). See 6.2.11.4.	
DI	PLLD_ON	Active-high control signal to enable REG7 (V_PLLD). See 6.2.11.7.	
DI	RF_ON	Active-high control signal to enable REG3A (V2_8RF). See 0.	
DI	TX_ON	Active-high control signal to enable REG3B (V_TX). See 0.	
DI	VOX_ON	Active-high control signal to enable REG8 (V_VOX). See 6.2.11.8.	
LDO Outputs			
AO	REG1	Voltage regulator output 1, VCC. See 6.2.11.1.	
AO	REG2	Voltage regulator output 2, VCCD. See 6.2.11.2.	
AO	REG3A	Voltage regulator output 3A, V_RF. See 0.	
AO	REG3B	High-side load switch from REG3A to supply V2_8TX. See 0.	

Type	Pin Name	Description	#
AO	REG4	Voltage regulator output 4, V_TCXO. See 6.2.11.4.	
AO	REG5	Voltage regulator output 5, V_PLL. See 6.2.11.5.	
AO	REG6	Voltage regulator output 6, V_VCCA. See 6.2.11.6.	
AO	REG7	Voltage regulator output 7, V_PLLD. See 6.2.11.7.	
AO	REG8	Voltage regulator output 8, V_VOX. See 6.2.11.8.	
Annunciator Driver Inputs			
DI	PWM_BUZ	Buzzer/ringer driver PWM input from microprocessor. See 6.2.5.2.	
DI	PWM_KBBL	Keyboard backlight driver PWM input from microprocessor. See 6.2.5.3.	
DI	PWM_LED	LED drive PWM input from microprocessor. See 6.2.5.4.	
DI	PWM_VIB	Vibrator motor driver PWM input from microprocessor. See 6.2.5.1.	
Annunciator Driver Outputs			
AO	BUZ_DRV	Buzzer/ringer driver output. See 6.2.5.2.	
AO	KBBL_DRV	Keyboard backlight driver output. See 6.2.5.3.	
AO	LED_DRV	LED driver output. See 6.2.5.4.	
AO	VIB_DRV	Vibrator driver output, controlled through the serial port. See 6.2.5.1.	
SIM Interface Signals			
DO	CLK2SIM	Level-shifted serial clock to the SIM. See 6.2.7.	
DB	DATA2SIM	Level-shifted serial data stream to/from SIM. See 6.2.7.	
DO	RST2SIM	Level-shifted reset signal to SIM. See 6.2.7.	
DI	SIM_CLK	SIM serial clock signal from microprocessor. See 6.2.7.	
DB	SIM_DATA	SIM serial data stream to/from microprocessor. See 6.2.7.	
DI	SIM_DET	Detects the presence of a SIM card; connected to a switch. See 6.2.7.	
DI	SIM_PROG	Programs the level of the SIM output. See 6.2.7.	
DI	SIM_RST	SIM reset signal from microprocessor. See 6.2.7.	
DI	SIM_SUPPLY	Enables the SIM power supply and output to the SIM. See 6.2.7.	
P	SIM_VCC	Power supply for SIM. See 6.2.7.	
Serial Interface			
DL	SER_CLK	Serial clock signal. See 6.2.8.	
DI	SER_CS	Active-high signal to frame serial communications. See 6.2.8.	
DB	SER_DATA	Serial data between the ASIC and the microprocessor. See 6.2.8.	
Battery Monitoring and Charging			

Type	Pin Name	Description	#
A	DRIVE	Output to control external pass element during charging. See 6.2.1.	
A	HCHG_PROG	Attache resistor from here to ground to program high current charging. See 6.2.1 and 6.2.9.2.	
AI	ISENSE_BAT	Low side of battery current sensor.	
AI	ISENSE_H	High side of charge supply current sensor. See 6.2.1.	
AI	ISENSE_L	Low side of charge supply current sensor. See 6.2.1.	
DO	PA_LOBAT_N	Active-low, open-drain output to hard-disable the RF power amplifier when battery voltage drops. See 6.2.1.	
P	TEMP_CHK	High-side load switch output that supplies power from V_{BAT} to an external temperature sensor; also powers up an internal Li^+ cell voltage scaling network for the ADC. See 6.2.4 and 6.2.9.2.	
Miscellaneous Inputs and Outputs			
AI	AUX	Auxiliary ADC input. See 6.2.4.	
DI	BAT_DOOR	Input to monitor the battery door state. See 6.2.10.	
DO	GPO1	External enable 1, controlled through the serial port. See 6.2.6.	
DO	GPO2	External enable 2, controlled through the serial port. See 6.2.6.	
DO	IRQ	Interrupt request signal to microprocessor; active high. See 6.2.10.	
DO	LCD_BL_EN	LCD backlight enable, controlled through the serial port. See 6.2.9.2.	
DI-pu	MR_N	Master reset: active-low signal that initiates system reset. See 6.2.2.	
AI	PACK_ID	Used to measure a battery pack identification voltage.	
AI	PACK_TEMP	Used to measure battery pack temperature.	
DI	PROX_SW	Input to monitor the proximity switch state. See 6.2.10.9.	
DO	RESET_N	Reset signal out to system. See 6.2.2.	
AI	TEMP	Temperature sensor ADC input. See 6.2.4.	
Power and Ground			
P	GND	Ground connection.	
P	GND	Ground connection.	
P	GND	Ground connection.	
P	V_BAT	Connection for the lithium-ion cell.	
P	V_CHG	Connection for USB (charging) power.	
P	VCAP1	SIM charge pump capacitor connection. See 6.2.7.	
P	VCAP2	SIM charge pump capacitor connection. See 6.2.7.	
AO	VREF_BYP	Reference voltage. Attach bypass capacitor here if required. See 6.2.3.	

6.1.3 Packaging

The ASIC will be packaged in a surface mountable 48 to 64-pin package with a footprint less than 100 mm^2.

The ASIC will be supplied to RIM in a suitable pick-and-place-compatible tape-and-reel format.

6.1.4 ESD and Latch-Up

The ASIC will have an ESD rating of greater than 10 kV (Class 3) on the SIM interface, V_{CHG}, and V_{BAT} pins; and 2 kV (Class 2) on all other pins, as per EIA/JESD22-A114-A "Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)".

The ASIC will be tested in accordance with JESD22-C101 "Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components".

The ASIC will be tested in accordance with EIA/JESD78 "IC Latch-Up Test".

See the Absolute Maximum Ratings section.

6.1.5 External Components

6.1.5.1 Magnetics

External magnetic components required by the ASIC will not exceed 7 x 4 x 2.5 mm (H x W x D) in size. These devices must be surface-mountable and incorporate an effective form of magnetic shielding to minimize radiated interference in the surrounding circuits. An example of such a part is Coilcraft DT1608C-103.

6.1.5.2 Capacitors

Capacitors will be surface-mountable low-ESR ceramics.

6.1.5.3 Resistors

Resistors will be surface-mountable metal-film chip resistors.

6.1.5.4 Other Devices (Transistors, etc.)

Aside from the pass element required for charging, the ASIC shall not require any external active devices.

6.1.6 Input Power and Power Sequencing

A rechargeable lithium-ion cell provides the main power to the ASIC. The system shall start up and turn on REG1 and REG2 when a supply voltage of $V_{BAT} \geq V_{BATON}$ is attached.

If REG1 and REG2 are on and V_{BAT} falls below V_{BATOFF}, REG1 and REG2 and any other enabled regulators shall turn off and remain off until V_{BAT} rises to V_{BATON} again or a charger is attached.

If $V_{BAT} < V_{BATON}$ and the charger is connected, REG1 and REG2 will be enabled to power the microprocessor. (The processor will, in turn, attempt to activate the high-power mode of USB to charge the primary cell, but the details of this process are beyond the scope of this document.)

When REG1 and REG2 first turn on, RESET_N will be held low to ensure that all external devices are properly initialized. See 6.2.2.

Under normal operating conditions, REG1 and REG2 will never turn off while $V_{BAT} \geq V_{BATOFF}$. However, a special sequence of bits written to a register via the serial bus shall allow software to turn off these two

regulators to drop current consumption to an absolute minimum. See 6.2.8. In this state, the ASIC may be turned on by either removing and replacing the lithium-ion cell or by attaching a charger.

A high-level summary of the power sequencing is presented in Figure 6-2.

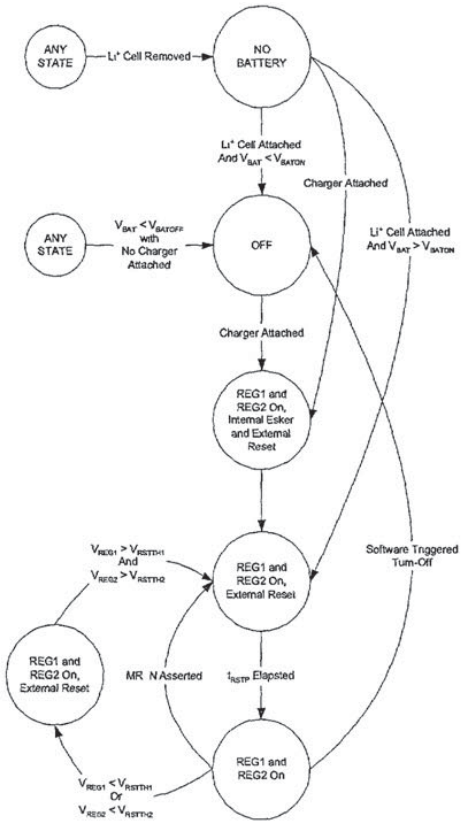

Figure 6-2: Power Sequencing

6.2 *Modules*

6.2.1 Battery Monitoring and Charge Control

The battery monitoring subsystem is responsible for notifying other subsystems of when specific voltage thresholds have been reached so that those subsystems can respond appropriately.

Voltage-sensitive effects are described in the sections where they apply.

6.2.1.1 PA_LOBAT_N

This signal is intended to kill the RF power amplifier in the event the lithium-ion cell goes unexpectedly under voltage.

PA_LOBAT_N shall be asserted when V_{BAT} falls below V_{PALBTH} for at least t_{PALBP}.

PA_LOBAT_N shall be an open-drain output requiring an external pull-up resistor.

6.2.1.2 Charging

The lithium-ion charger may be powered from a USB port, an AC wall adapter, a car adapter, or any other source providing a supply of V_{CHG}.

To minimize power consumption when not charging, the charging circuitry shall be powered from the V_CHG pin and shall be shut down when no charger is attached. This shall include any circuitry required by the ADC to make charge current measurements. See 6.2.4.

During charging, the REG1, REG2, and REG4 regulators shall be powered from V_CHG. This will allow the PDA to turn on even when the lithium-ion cell voltage is below V_{BATON}.

When the ASIC is not charging the lithium-ion cell, REG1, REG2, and REG4 shall be powered from the lithium-ion cell.

The other regulators shall be powered off the lithium-ion cell and may be turned on at any time; the microprocessor will be responsible for ensuring that they remain off when there is insufficient charge in the cell.

By default, the lithium-ion charger shall be disabled when a supply is first attached to V_CHG; the microprocessor will be responsible for activating the charger and for setting the charge level. See 6.2.9.2. The low and medium charge currents—I_{CHGL} and I_{CHGM}, respectively—shall be programmed internally. Attaching a suitable resistor to HCHG_PROG shall program the high charge current, ICHGH.

The charging subsystem shall be based on a linear scheme, with the high-side pass element external to the ASIC.

Because the PDA shall be USB compliant, the amount of current the entire PDA can draw from the USB port to which it is attached shall be limited to either I_{CHGL} or I_{CHGM}, as determined by the microprocessor. As such, the ASIC shall monitor the current flowing into the PDA from the USB host and adjust the charging current flowing into the lithium-ion in response to the demands of the microprocessor to maintain the total current draw within the aforementioned limits.

A conceptual view of the charging subsystem is contained in Figure 6-3 below.

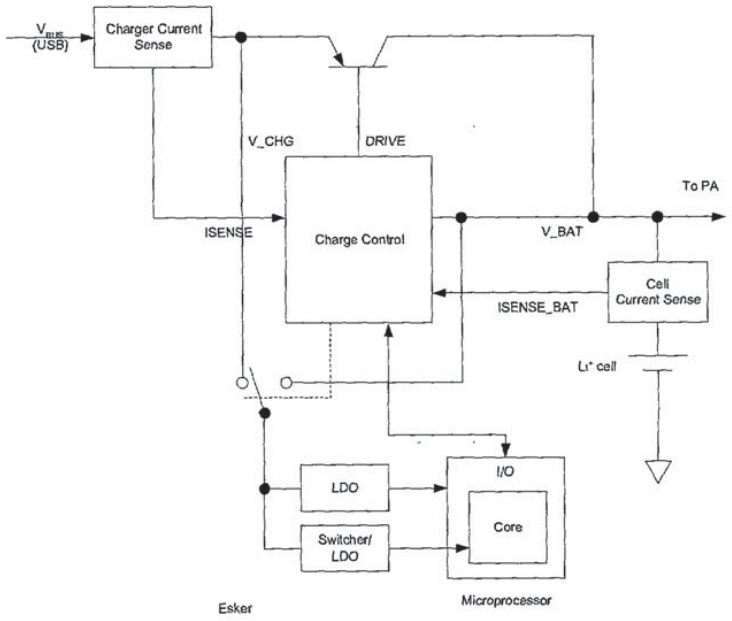

Figure 6-3: USB Charging Concept

The ISENSE_H and ISENSE_L pins will allow the ASIC to measure the voltage across a sense resistor to determine the current being drawn by the PDA.

To determine the current flowing into the lithium-ion cell, the ASIC will measure the voltage across a sense resistor between the V_BAT and ISENSE_BAT pins. It is this current that shall be measurable by the ADC as per 6.2.4.

The DRIVE pin will control the external pass element.

If the lithium-ion cell voltage is below the internal low-voltage threshold of $V_{CHGTRTH}$, the charger shall use a trickle charge of I_{CHGTR} to condition the primary cell until the voltage of the battery reaches $V_{CHGTRTH}$. A preconditioning timer with a timeout period of t_{CHGTR} shall be provided for additional safety.

Lithium-ion charging shall be constant-current/constant-voltage. That is, once the lithium-ion cell voltage has reached V_{CHGTHR}, the charge current shall be gradually reduced to hold the cell at that voltage until the current falls below I_{CHGTH}, at which point the charge current shall be turned off. Current-based charge termination will be handled by the microprocessor.

The ASIC shall allow programming of V_{CHGTHR} threshold via metal mask changes such that a future change in the cell chemistry is easily accommodated. The requested thresholds are listed in Table 6-3 below.

Table 6-3: Charge Termination Thresholds

V_BAT rising edge (V)	Cell Technology
4.30	Future Development
4.25	Future Development
4.20	Li Cobalt, Li Polymer
4.175	Li Nickel

V_BAT rising edge (V)	Cell Technology
4.15	Li-Ion Manganese
4.1	Li Metal
3.7	Future Development

6.2.2 Reset Controller

The reset controller works with the battery monitoring system to ensure that the digital power supplies have had time to stabilize before allowing the execution of any program code. This ensures that all devices start up in a known state.

The RESET_N signal shall already be asserted when REG1 and REG2 turn on. One approach may be to power the low-output driver from V_BAT or V_CHG, while powering the high-output driver from REG1.

The RESET_N signal shall be asserted whenever one of the following conditions is met:

1. REG1 and REG2 first turn on;
2. the output of REG1 or REG2 falls below V_{RSTTH1} or V_{RSTTH2}, respectively (in which case RESET_N shall remain asserted until both supplies are above this threshold again);
3. the MR_N pin is pulled low for at least the period t_{RSTMR};
4. the appropriate bit pattern is written to the CONTROL register (see 6.2.9.2).

The MR_N pin shall have an internal pull-up to REG1 of $R_{RSTMRPU}$.

Regardless of the condition that caused the reset, the RESET_N signal shall be asserted for a minimum period of t_{RSTP}.

The reset controller shall also generate an internal ASIC reset signal on conditions 1 and 2 to ensure that the register file is properly initialized. See 6.2.9.

6.2.3 Bandgap Reference

An internal low-power bandgap cell voltage reference of V_{REF} will be provided, and may have an external bypass pin if required. This reference will be low noise and have an accuracy of ΔV_{REF} or better over temperature. The bandgap cell will be suitably buffered to provide other references as required.

6.2.4 Analog to Digital Converter with MUX

Analog to digital conversions are initiated after a request via the serial port. The converter shall have 10 bits of resolution with accuracy as specified in the Electrical Characteristics section, including errors introduced from input scaling.

A six-channel analog MUX will select among the following four input sources:

1. the lithium-ion cell voltage (at the V_BAT pin);
2. a temperature sensor (National Semiconductor LM20 or similar);
3. a voltage equivalent of the charge current flowing into the lithium-ion cell;
4. three external voltage source: one to measure the battery pack identification, one to measure battery pack temperature, and one additional auxiliary source.

The ranges of each ADC input will be determined by RIM. The lithium-ion cell voltage will be scaled internally in the ASIC. To minimize current consumption, this scaling network will only be powered when the TEMP_CHK signal is on. See 6.2.9.2.

The auxiliary input will not be scaled.

The temperature sensor will range from -55°C to 130°C, which shall be converted into a 10-bit unsigned binary value, using the full ADC input range.

The ADC shall be able to measure charge current over the range specified in the Electrical Characteristics section, converting it into a 10-bit unsigned value, using the full ADC input range.

See 6.2.9.5 and 6.2.9.6 for details on the ADC software interface.

6.2.5 Annunciator Drivers

Drive circuitry for four annunciators is required. The microprocessor will provide high frequency PWM digital signals (referenced to REG1) to the ASIC to allow for efficient control of power to the four annunciators. The ASIC will use these signals to control four high-current drivers that will switch the annunciators on and off.

6.2.5.1 Vibrator Motor

This driver will pull the VIB_DRV pin to ground to drive a miniature vibrator motor. This driver shall have 'inductive kickback' protection to the primary voltage source.

6.2.5.2 Buzzer/Ringer

This driver will pull the BUZ_DRV pin to ground to drive an acoustic buzzer.

6.2.5.3 Keyboard Backlighting LED Array

This driver will pull the KBBL_DRV pin to ground to drive an array of LEDs

6.2.5.4 Notification LED

This driver will pull the LED_DRV pin to ground to drive a single LED.

6.2.6 General-Purpose Outputs

GPO1 and GPO2 are two external outputs controlled by the serial port. These are intended for future use, and are referenced to REG1. See 6.2.9.2.

6.2.7 SIM Interface

This block shall conform to the GSM 11.11 and 11.12 specifications. In the event of discrepancies between this specification and GSM 11.11 and 11.12, GSM 11.11 and 11.12 shall be taken as correct.

This module shall provide appropriate power to the SIM and also translate voltage levels between those used in the PDA and those used at the SIM (currently 3 V and 5 V).

To generate the required 5 V, this module shall use a switched capacitor charge pump topology with the output capacitor connected across the SIM_VCC pin and ground, and the pump capacitor across VCAP1 and VCAP2.

REG1 will supply the power to this block. The control logic for this module is summarized in Table 6-4 below.

Table 6-4: SIM Interface Operating Modes

Input Signals				Operating Mode
REG1	SIM_DET	SIM_PROG	SIM_SUPPLY	
X	L	X	X	Off mode SIM supply disabled: SIM_VCC open RST2SIM, CLK2SIM, and DATA2SIM low
On	H	L	L	Power-down mode Program for 5 V operation SIM supply disabled: SIM_VCC open RST2SIM, CLK2SIM, DATA2SIM low
On	H	H	L	Power-down mode Program for 3 V operation SIM supply disabled: SIMVCC open RST2SIM, CLK2SIM, DATA2SIM low
On	H	X	H	Normal operating mode SIM supply enabled SIM_VCC = 3 V or 5 V

6.2.8 Serial Interface

The serial interface between the microprocessor and the ASIC shall be a three-wire interface using a bi-directional data line. The bus shall be host-centric, with only the microprocessor driving the SER_CS and SER_CLK signals.

Information inside the ASIC will be stored in registers, which the processor will access by specifying an address.

The SER_CS signal shall control the serial bus as indicated in Table 6-5 below.

Table 6-5: SER_CS Bus Behaviour

SER_CS	Bus State
L	Bus inactive SER_DATA high-impedance
H	Bus active SER_DATA depends on whether data is being read from or written to the ASIC
L → H	Bus reset Ensures that the bus becomes active in a known state, independent of any previous operations

Protocol: TBD.

6.2.9 Register File

The registers that the ASIC will implement are summarized below in Table 6-6.

Table 6-6: ASIC Register File

Address	Name	Description
0 0000	ASIC_ID	Returns a bit-pattern identifying the ASIC revision
0 0001	CONTROL	Controls the GPO pins, LED_BL_EN, TEMP_CHK, and charging
0 0010	IRQ_EN	Set bits here to enable interruptible events to assert IRQ
0 0011	IRQ_FLAG	Set bits here indicate an interruptible event has occurred
0 0100	ADC_CTRL	Controls the analog to digital converter and MUX
0 0101	ADC_H	Holds the unsigned binary result of the ADC measurement
0 0110	INPUT	Provides additional information

The following sections describe the registers in more detail. Table 6-7 defines the notation used in the Attributes field of each register bit.

Table 6-7: Bit Attribute Definitions

Symbol	Meaning
R	Bit is read-only
W	Bit is write-only
R/W	Bit can be read and written
-0	Bit defaults to 0 on reset
-1	Bit defaults to 1 on reset
-u	Bit is undefined on reset

Writing to a read-only bit shall be allowed but shall have no effect.

6.2.9.1 ASIC_ID Register

This register allows the microprocessor to identify the revision of the power management ASIC.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Description	0	0	0	0	0	0	0	0	0	1
Attributes	R-0									R-1

This register is read only.

The ASIC will incorporate the ability to reprogram this register through metal mask changes.

6.2.9.2 CONTROL Register

This register controls various output and control signals.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	0	0	F_RST	OFF	CHG1	CHG0	LCD_BL_EN	TEMP_CHK	GPO2	GPO1
Attributes	R-0		W-u	W-u	R/W-0	R/W-0	R/W-0			

When one of the LCD_BL_EN, GPO1, or GPO2 bits is set to 1, the corresponding output pin will be a logic high. Conversely, when one of these bits is cleared to 0, the corresponding output pin will be a logic low.

When the TEMP_CHK bit is set to 1, the TEMP_CHK pin shall be connected to V_{BAT} to power an external temperature sensor, and the V_{BAT} ADC scaling network will be powered up. Conversely, when the TEMP_CHK bit is cleared to 0, the TEMP_CHK pin will be disconnected from V_{BAT} and the lithium-ion scaling network will be unpowered.

The CHG1 and CHG0 bits specify the mode of operation for the charger, as described in Table 6-8 below.

Table 6-8: Charger Modes

CHG1	CHG0	Mode	Description
0	0	OFF	The charger is disabled.
0	1	LOW	The charger will adjust current flowing into the lithium-ion cell to limit the current drawn from the charger supply to I_{CHGL}.
1	0	MEDIUM	The charger will adjust current flowing into the lithium-ion cell to limit the current drawn from the charger supply to I_{CHGM}.
1	1	HIGH	The charger will adjust current flowing into the lithium-ion cell to limit the current drawn from the charger supply to an amount determine by the external programming resistor on the HCHG_PROG pin.

The OFF bit is a write-only bit that can be used to turn off the ASIC and disable REG1 and REG2 as described in 6.1.6. To turn off the ASIC, the pattern 1, 0, 1 must be written to this bit on three consecutive register writes. Once in this state, the ASIC may be turned on again as per 6.1.6.

The F_RST bit is a write-only bit that can be used to force a system reset (see 6.2.2). To force a system reset, the pattern 1, 0 must be written to this bit on two consecutive register writes.

For both the OFF and F_RST bits, any serial transactions that interrupt the required patterns shall reset the pattern-matching circuitry.

6.2.9.3 IRQ_EN Register

This register allows the microprocessor to specify which interruptible events will cause the IRQ signal to be asserted.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	CHG_DET	PROX_SW	PA_LOBAT	O_TEMP	O_VOLT	U_VOLT	SER_ERR	BAT_DOOR	SIM_DET	ADC
Attributes	R/W-0									

When a bit is set to 1, the corresponding interrupt is enabled and will cause the assertion of IRQ. Conversely, when a bit is cleared to 0, the corresponding interrupt is disabled and will not cause the assertion of IRQ.

See 6.2.10.

6.2.9.4 IRQ_FLAG Register

This register keeps track of which interruptible events have occurred.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	CHG_DET	PROX_SW	PA_LOBAT	O_TEMP	O_VOLT	U_VOLT	SER_ERR	BAT_DOOR	SIM_DET	ADC
Attributes	R-0									

When an interruptible event occurs (see 6.2.10) the corresponding bit in this register will be set—even if the event is disabled in IRQ_EN.

After the microprocessor has read this register, all its bits will be cleared and the IRQ line will be de-asserted.

Any interrupts that occur while this register is being read or cleared or while IRQ is being de-asserted shall be caught, causing continued assertion or reassertion of the IRQ signal.

See 6.2.10.

6.2.9.5 ADC_CTRL Register

This register controls the operation of the analog to digital converter and the MUX.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	0	0	0	0	0	0	ADC_INIT	CH2	CH1	CH0
Attributes	R-0						R/W-0	R/W-0		

Bits CH0 and CH1 shall select the MUX channel to convert, as defined in Table 6-9.

Table 6-9: ADC MUX Channel Selection

CH2	CH1	CH0	MUX Channel
0	0	0	V_BAT
0	0	1	TEMP
0	1	0	I_CHG
0	1	1	AUX
1	0	0	PACK_TEMP
1	0	1	PACK_ID
1	1	0	Reserved
1	1	1	Reserved

The ADC shall initiate a conversion when a 1 is written to the ADC_INIT bit. Once a conversion has started, further writes to this bit shall have no effect—it shall remain fixed at 1.

When the conversion is complete, the ASIC shall first write the result into ADC_RES, and then store a 0 to the ADC_INIT bit and set the appropriate bit in IRQ_FLAG.

Measuring V_BAT and TEMP will require the TEMP_CHK signal to be on. See 6.2.4 and 6.2.9.2.

6.2.9.6 ADC_RES Register

After an analog to digital conversion, this register will contain the unsigned binary result.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	RES[9]	RES[8]	RES[7]	RES[6]	RES[5]	RES[4]	RES[3]	RES[2]	RES[1]	RES[0]
Attributes	R-0									

6.2.9.7 INPUT Register

This register shall contain miscellaneous inputs.

Bit	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Description	CHG_DET	PROX_SW	0	0	PA_LOBAT	CHG_ON	CHG_TR	BAT_DOOR	SIM_DET	RESET
Attributes	R-u	R-u	R-0		R-u	R-u	R-u	R-u	R-u	R-u

The RESET bit shall be set to 1 if the last reset sequence was initiated by asserting the MR_N signal. This bit shall be cleared to 0 if the last reset sequence was initiated by a battery-insertion or under-voltage condition.

The SIM_DET, BAT_DOOR, PA_LOBAT, and PROX_SW bits shall provide latched versions of the current state of the BAT_DOOR, SIM_DET, PA_LOBAT, and PROX_SW signal pins.

The CHG_TR bit shall be set to 1 if the charger is currently on and operating in trickle charge mode (see 6.2.1.2). This bit shall be cleared to 0 otherwise.

The CHG_ON bit shall be set to 1 if the charger is currently on. This bit shall be cleared to 0 otherwise.

The CHG_DET bit shall be set to 1 when a voltage V_{CHG} is detected on the V_CHG pin. This bit shall be cleared to 0 otherwise.

6.2.10 Interrupt Controller

An interrupt request line (IRQ) shall notify the processor of the noteworthy events listed in Table 6-10 below. When one of the events in Table 6-10 occurs, the corresponding bit in the IRQ_FLAG will be set, and if the corresponding bit in the IRQ_EN register is set, the IRQ signal will be asserted. Once the IRQ signal has been asserted, additional interrupts will update the appropriate bits in the IRQ_FLAG but the IRQ signal will remain asserted.

Any interrupts that occur while this register is being read or cleared or while IRQ is being de-asserted shall be caught, causing continued assertion or reassertion of the IRQ signal.

Table 6-10: Interrupts Generated by Esker

IRQ	Name	Condition
0	O_TEMP	The ASIC junction temperature exceeded T_{JMAX}
1	O_VOLT	V_{BAT} rises above V_{BATOV} for greater than t_{OVUVP}
2	U_VOLT	V_{BAT} drops below V_{BATUV} for greater than t_{OVUVP}
3	SER_ERR	Serial communication error (invalid address, bad framing, etc.)
4	BAT_DOOR	The battery door has been opened
5	SIM_DET	The SIM door has been opened or closed
6	ADC	The ADC has completed its measurement
7	PA_LOBAT	The PA_LOBAT_N signal was asserted
8	PROX_SW	The proximity switch has opened or closed
9	CHG_DET	The V_CHG pin has entered or left the V_{CHG} range

Reading the IRQ_FLAG will cause all the bits in that register to be cleared and will de-assert the IRQ signal.

6.2.10.1 O_TEMP Interrupt

This event shall occur whenever the ASIC die temperature exceeds T_{JMAX}.

6.2.10.2 O_VOLT Interrupt

This event shall occur whenever the lithium-ion cell falls below V_{BATUV} for t_{OVUVP}.

6.2.10.3 U_VOLT Interrupt

This event shall occur whenever the lithium-ion cell rises above V_{BATOV} for t_{OVUVP}.

6.2.10.4 SER_ERR Interrupt

This event shall occur whenever the serial port on the ASIC detects an error in the serial communications, including:

1. the microprocessor specified a bad address;
2. the last transaction was not completed.

6.2.10.5 BAT_DOOR Interrupt

This event shall occur whenever the BAT_DOOR signal changes state.

6.2.10.6 SIM_DET Interrupt

This event shall occur whenever the SIM_DET signal changes state.

6.2.10.7 ADC Interrupt

This event shall occur only after the ADC has completed a conversion and stored the result in ADC_RES.

6.2.10.8 PA_LOBAT Interrupt

This event shall occur whenever the PA_LOBAT_N signal is asserted. See 6.2.1.1.

6.2.10.9 PROX_SW Interrupt

This event shall occur whenever the PROX_SW pin changes state.

6.2.10.10 CHG_DET Interrupt

This event shall occur whenever the voltage on the V_CHG pin rises above or falls below V_{CHG}.

6.2.11 Regulators

There will be nine regulated outputs, derived from eight regulators. Each regulated output will allow a ±200 mV range of outputs (in 100 mV increments) through a metal mask change.

The regulators must be stable with the capacitive load profile given in the Electrical Characteristics as a minimum. It is desired that all regulators require a ceramic capacitor with **no** series load resistor in order to maintain stability.

Each regulator must meet its noise and ripple specs with any or all of the other regulators going from a minimum or quiescent current to full peak load within a 10 µs time frame.

An indefinite short circuit on any output shall not cause any permanent damage to the ASIC.

6.2.11.1 REG1: Digital I/O

REG1 supplies power for the memory devices and input/output portions of the system (VCC) at V_{REG1}. This regulator will need to have sufficient load-to-line rejection that will be determined by RIM. This regulator shall be enabled as per 6.1.6.

6.2.11.2 REG2: Digital Core

REG2 supplies power to the core of the microprocessor, the real-time clock (RTC), and digital portions of the baseband processor (VCCD), all at V_{REG2}. This output shall be enabled as per 6.1.6 and 6.2.1.2.

The components using this supply have very rapid current transitions and high peak-to-average current ratios. Therefore fast transient response for this output is important. This regulator will need to have sufficient load-to-line rejection that will be determined by RIM.

Furthermore, because the drop to V_{REG2} from V_{CHG} or V_{BAT} is large and the potential currents so high, a switching power supply is required to limit heat dissipation and to maximize efficient use of battery power.

The switching power supply will be included in the ASIC unless such a design prevents the meeting of the noise specifications for those linear regulators where it is a critical parameter. In this case, RIM may allow an external solution.

The exact configuration is left to the designer, but possibilities may include:

1. use of a switching power supply to provide VCCD directly;
2. use of a switching power supply to power REG2;
3. use of a switching power supply to provide VCCD under high load conditions, and powering REG2 from V_BAT/V_CHG under low load conditions.
4. use of a switching power supply to power REG2 under high load conditions, and powering REG2 from V_BAT/V_CHG under low load conditions.

Options 3 and 4 are put forth because the current draw from the VCCD rail may range from $I_{REG2SUS}$ to I_{REG2}; and switching power supplies tend to have poor efficiency at low loads.

The switching power supply shall limit ripple on the lithium-ion cell to ΔV_{BATSW} or less.

The switching power supply will have an efficiency of η_{REG2SW} or higher under full load conditions.

6.2.11.3 REG3: Radio Analog

REG3 supplies power for the analog sections of the radio at V_{REG3}. This includes the analog supply to the front-end and IF stages of the radio receiver, and the transmit portions of the radio. REG3 shall be split into two outputs: REG3A, which will be the main regulator output; and REG3B, which will be connected to the main regulator output via a load switch.

REG3A (V_RF) supplies power to the transceiver. REG3B (V_TX) supplies the transmit section and is required to turn on and turn off quickly, with times $t_{REG3BON}$ and $t_{REG3BOFF}$, respectively. When disabled, REG3A and REG3B will be pulled down below the low threshold by $R_{SDREG3A}$ and $R_{SDREG3B}$, respectively.

Control of the REG3A and REG3B rails is provided by the two inputs RF_ON and TX_ON. The following table illustrates the state of each line.

RF_ON	TX_ON	REG3A	REG3B
L	X	Disabled	Disabled
H	L	Enabled	Disabled
H	H	Enabled	Enabled

6.2.11.4 REG4: TCXO

REG4 (V_TCXO) supplies power to the temperature-compensated crystal oscillator (TCXO) at V_{REG4}, and as such needs to be very low noise, and have high ripple rejection. When disabled this regulator output will be pulled down below the low threshold. REG4 is controlled by the input CLK_ON.

CLK_ON	REG4
L	Disabled
H	Enabled

6.2.11.5 REG5: PLL

REG5 (V_PLL) supplies power to the phase locked loop (PLL) at V_{REG5}, and as such needs to be very low noise, and have high ripple rejection. When disabled this regulator output will be pulled down below the low threshold. REG5 is controlled by the input PLL_ON.

PLL_ON	REG5
L	Disabled
H	Enabled

6.2.11.6 REG6: Analog Baseband CODEC

REG6 (VCCA) supplies power to the analog sections of the baseband CODEC at V_{REG6}. REG6 is controlled by the input ANA_ON.

ANA_ON	REG6
L	Disabled
H	Enabled

6.2.11.7 REG7: PLL Digital

REG7 (V_PLLD) supplies power to the digital portion of the PLL system at V_{REG7}. REG7 is controlled by the input PLLD_ON.

PLLD_ON	REG7
L	Disabled
H	Enabled

6.2.11.8 REG8: Voice-Band Analog

REG8 (V_VOX) supplies power to the analog voice-band circuitry at V_{REG8}, and as such needs to have very low noise and high ripple rejection in the audio band.

REG8 is controlled by the input VOX_ON.

VOX_ON	REG8
L	Disabled
H	Enabled

6.2.11.9 Suspend Mode

When the PDA enters suspend mode, only the digital regulators REG1 and REG2 and the SIM card supply will be turned on. In this mode, the current drawn from REG1 and REG2 will drop to $I_{REG1SUS}$ and $I_{REG2SUS}$, respectively, or less; their output voltages shall remain within the specified limits, although their AC characteristics may be compromised.

Total quiescent current drawn by the ASIC shall not exceed I_{SUS}.

7 Electrical Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

Operation beyond maximum ratings may cause permanent damage.

Pin voltages:	
VIB	-0.8 to +7.0 V
Other supply input and output pins	-0.3 to +7.0 V
All other input/output	-0.3 to +7.0 V
Peak currents	Internal limits
Power dissipation	TBD @ 25°C (derate at TBD mW/°C)
Operating free-air temperature range	-40 to +85°C
Storage temperature range	-65 to +150°C
Maximum junction temperature	150°C
Lead temperature, soldering (1.6 mm from case for 10 sec.)	260°C
ESD sensitivity:	
DATA2SIM, CLK2SIM, RST2SIM	8kV HBM minimum
CHARGE	8kV HBM minimum
All other pins	2kV HBM minimum

7.2 Electrical Characteristics

3.3 V ≤ V_{BAT} ≤ 4.2 V, temperature = -40 to +85°C unless otherwise noted.

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
General						
Lithium-ion input voltage	V_{BAT}		TBD		V	
Charger input voltage	V_{CHG}	4.3		5.5	V	
Current draw from V_{CHG}	I_{CHGL}			100	mA	
	I_{CHGM}			500	mA	
Current consumption in suspend mode	I_{SUS}			100	µA	$I_{REG1} \le I_{REG1SUS}$ $I_{REG2} \le I_{REG2SUS}$
Junction temperature interrupt threshold	T_{JMAX}		TBD		°C	Specified by designer
Digital Signals						
Input load current	I_{DI}			±1	µA	V_{IN} = H or L
Output current	I_{DO}	4			mA	Sink/source
Output high voltage	V_{DOH}	V_{REG1} - 0.2			V	$I_{DOH} \le I_{DO}$
Output low voltage	V_{DOL}			0.2	V	$I_{DOL} \le I_{DO}$
Input high threshold	V_{DIH}	$0.7V_{REG1}$			V	
Input low threshold	V_{DIL}			$0.25V_{REG1}$	V	
GPO output current	I_{GPO}	16			mA	
Input rise-/fall-time	t_{IR}, t_{IF}		5		ns	from microprocessor
Output rise-/fall-time	t_{OR}, t_{OF}			10	ns	to microprocessor
Battery Monitoring and Charge Control						
Lithium-ion trickle-charging termination threshold voltage	$V_{CHGTRTH}$	2.4	2.5	2.65	V	V_{BAT} rising
Trickle-charge current	I_{CHGTR}	20	25	30	mA	
Trickle-charge timeout period	t_{CHGTR}		1800		s	
Lithium-ion charge termination threshold voltage	V_{CHGTHR}	4.158	4.2	4.242	V	See 6.2.1.2
Lithium-ion charge termination current	I_{CHGTH}		100		mA	Approximately C/10
Lithium-ion charge termination threshold hysteresis	ΔV_{CHGTH}	-100		TBD	mV	
Lithium-ion threshold voltage to activate REG1 and REG2	V_{BATON}		3.30		V	V_{BAT} rising
Lithium-ion threshold voltage to disable REG1 and REG2	V_{BATOFF}		2.55		V	V_{BAT} falling
Lithium-ion over-voltage threshold	V_{BATOV}	4.255	4.28	4.305	V	V_{BAT} rising
Lithium-ion under-voltage threshold	V_{BATUV}	3.35	3.4	3.45	V	V_{BAT} falling
Over-/under-voltage timeout period	t_{OVUVP}		3		s	
PA_LOBAT assertion threshold	V_{PALBTH}	3.00		3.15	V	V_{BAT} falling
PA_LOBAT assertion threshold hysteresis	$V_{PALBHYS}$		7		mV	
PA_LOBAT timeout period	t_{PALBP}		TBD		µs	

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
Bandgap Reference						
Reference voltage	V_{REF}		TBD		V	Voltage dictated by design
Reference tolerance	ΔV_{REF}	-0.1		+0.1	%	Over temperature
Analog to Digital Converter and MUX						
Absolute accuracy			1.5		%	Full scale, over temperature, over voltage
V_{BAT} input range			TBD		V	
V_{TEMP} input range			TBD		V	
I_{CHG} input range		0		1023	mA	
Auxiliary input range		TBD		V_{REF}	V	For AUX1 and AUX2
Input leakage	I_{ADCL}	-5		+5	nA	
Channel acquisition time	t_{ACQ}		TBD		µs	Specified by designer
Conversion time	t_{CONV}			40	µs	
Annunciator Drivers						
BUZ_DRV on resistance	R_{BUZ}			1	Ω	I_{BUZ} = 300 mA PWM_KBBL = H
BUZ_DRV peak on current	I_{BUZPK}			300	mA	
BUZ_DRV duty cycle			50		%	
BUZ_DRV off leakage	I_{BUZL}			0.5	µA	PWM_KBBL = L
KBBL_DRV on resistance	R_{KBBL}			1	Ω	I_{KBBL} = 250 mA PWM_KBBL = H
KBBL_DRV peak on current	I_{KBBLPK}			250	mA	
KBBL_DRV duty cycle			50		%	
KBBL_DRV off leakage	I_{KBBLL}			0.5	µA	PWM_KBBL = L
LED_DRV on resistance	R_{LED}			1	Ω	I_{LED} = 30 mA PWM_LED = H
LED_DRV peak on current	I_{LEDPK}			30	mA	
LED_DRV duty cycle			50		%	
LED_DRV off leakage	I_{LEDL}			0.5	µA	PWM_LED = L
VIB_DRV on resistance	R_{VIB}			1	Ω	I_{VIB} = 170 mA PWM_VIB = H
VIB_DRV average on current	I_{VIB}		130	170	mA	
VIB_DRV duty cycle			34		%	V_{MOTOR} = 1.4 V V_{BAT} = 4.1 V
VIB_DRV off leakage	I_{VIBL}			0.5	µA	PWM_VIB = L
Annunciator transition frequency	f_{TPWM}	10			MHz	
SIM Interface (refer to GSM 11.11 and 11.12)						
Charge pump capacitance	$C_{SIMPUMP}$		TBD		µF	Specified by designer
SIM_VCC output capacitance	C_{SIMVCC}		TBD		µF	Specified by designer
SIM_VCC output voltage	V_{SIM}	4.5		5.5	V	SIM_SUPPLY = H SIM_PROG = L I_{SIM} = 10 mA

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
		2.7		3.3		SIM_SUPPLY = H SIM_PROG = H I_{SIM} = 6 mA
SIM_VCC output current	I_{SIM}			10	mA	SIM_SUPPLY = H SIM_PROG = L
				6		SIM_SUPPLY = H SIM_PROG = H
Switching frequency	f_{SIMSW}	500	800	1100	kHz	
Output ripple	ΔV_{SIMO}			100	mV	SIM_PROG = L
Turn-on time	t_{SIMON}			1	ms	From stand-by to 5 V
Efficiency	η_{SIMSW}		83		%	I_{SIM} = 10 mA
Frequency on SIM_CLK/LS_SIM_CLK	f_{SIMCLK}	1		5	MHz	SIM_PROG = L
		1		4		SIM_PROG = H
Duty cycle on LS_SIM_CLK		40	50	60	%	50% duty cycle on SIM_CLK
Data rate on SIM_DATA/LS_SIM_DATA			$f_{SIMCLK}/372$	$f_{SIMCLK}/32$	MHz	
LS_SIM_RST high level output voltage	$V_{SIMRSTOH}$	V_{SIM} - 0.7		V_{SIM}	V	SIM_PROG = L
		$0.8V_{SIM}$		V_{SIM}		SIM_PROG = H
LS_SIM_RST low level output voltage	$V_{SIMRSTOL}$			0.6	V	SIM_PROG = L
				$0.2V_{SIM}$		SIM_PROG = H
LS_SIM_RST rise-time	$t_{SIMRSTR}$			400	µs	
LS_SIM_RST fall-time	$t_{SIMRSTF}$			400	µs	
LS_SIM_CLK high level output voltage	$V_{SIMCLKOH}$	$0.7V_{SIM}$		V_{SIM}	V	
LS_SIM_CLK low level output voltage	$V_{SIMCLKOL}$			0.5	V	SIM_PROG = L
				$0.2V_{SIM}$		SIM_PROG = H
LS_SIM_CLK rise-time	$t_{SIMCLKR}$			18	ns	SIM_PROG = L
				50		SIM_PROG = H
LS_SIM_CLK fall-time	$t_{SIMCLKF}$			18	ns	SIM_PROG = L
				50		SIM_PROG = H
LS_SIM_DATA high level input voltage	$V_{SIMDATAIH}$	$0.7V_{SIM}$		V_{SIM} + 0.3	V	
LS_SIM_DATA low level input voltage	$V_{SIMDATAIL}$	-0.3		0.8	V	SIM_PROG = L
		-0.3		$0.2V_{SIM}$		SIM_PROG = H
LS_SIM_DATA high level output voltage	$V_{SIMDATAOH}$	$0.7V_{SIM}$		V_{SIM}	V	
LS_SIM_DATA lowlevel output voltage	$V_{SIMDATAOL}$			0.4	V	
LS_SIM_DATA rise-time	$t_{SIMDATAR}$			1	µs	
LS_SIM_DATA fall-time	$t_{SIMDATAF}$			1	µs	
Serial Interface and Interrupt Controller						
Clock speed on SER_CLK	f_{SERCLK}			6.5	MHz	
Clock speed on SER_DATA	$f_{SERDATA}$			6.5	MHz	
Interrupt latency	t_{INT}		100	200	ns	From event to assertion of IRQ signal; see 6.2.10
Low Dropout Regulators						
REG1 (VCC, Digital I/O)						

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
Output voltage	V_{REG1}	2.925	3.0	3.075	V	Over full current range
Load current	I_{REG1}			160	mA	
Suspend mode load current	$I_{REG1SUS}$		50		mA	
Dropout voltage	V_{REG1DO}			200	mV	$I_{LOAD} = I_{REG1}$
Line regulation	$\Delta V_{REG1LNR}$	-0.05	0	0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG1LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG1}
Supply rejection	$PSRR_{REG1}$	60			dB	f_{IN} < 100 kHz
Transient response		-1		+1	%	Within 10 µs of 1 mA to I_{REG1}
Peak short circuit current	I_{REG1SC}			TBD	mA	
Output capacitor	C_{OREG1}		TBD		µF	Specified by designer
REG2 (VCCD, Digital Core)						
Output voltage	V_{REG2}	1.725	1.8	1.9	V	Over full current range
Load current	I_{REG2}			100	mA	
Suspend mode load current	$I_{REG2SUS}$	0.02	2		mA	
Dropout voltage	V_{REG2DO}			200	mV	$I_{LOAD} = I_{REG2}$
Line regulation	$\Delta V_{REG2LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG2LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG2}
Supply rejection	$PSRR_{REG2}$	60			dB	f_{IN} < 100 kHz
Transient response		-1		+1	%	Within 10 µs of 1 mA to I_{REG2}
Peak short circuit current	I_{REG2SC}			TBD	mA	
Output capacitor	C_{OREG2}		TBD		µF	Specified by designer
Switching supply efficiency	η_{REG2SW}	85	90		%	
Switching-induced ripple on lithium-ion cell	ΔV_{BATSW}			10	mV	
REG3 (V_RF and V_TX, Radio Analog)						
Output voltage	V_{REG3}	2.7	2.8	2.9	V	Over full current range RF_ON ≥ V_{DIH}
Load current	I_{REG3}			150	mA	
Dropout voltage	V_{REG3DO}			200	mV	$I_{LOAD} = I_{REG3}$
Line regulation	$\Delta V_{REG3LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG3LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG3}
Supply rejection	$PSRR_{REG3}$	60			dB	f_{IN} < 100 kHz
		40				f_{IN} = 250 kHz
Turn-on time for REG3B	$t_{REG3BON}$			8	µs	
Turn-off time for REG3B	$t_{REG3BOFF}$			30	µs	
Output noise	e_{nREG3}		30	40	μV_{RMS}	10 kHz < f < 100 kHz
Peak short circuit current	I_{REG3SC}			TBD	mA	
Output capacitor	C_{OREG3}		TBD		µF	Specified by designer
REG3A output shutdown resistance	$R_{SDREG3A}$		300		Ω	
REG3B load switch on resistance	$R_{REG3BON}$			0.25	Ω	I_{REG3B} = 30 mA
REG3B output shutdown resistance	$R_{SDREG3B}$		30		Ω	
REG4 (V_TCXO, TCXO)						
Output voltage	V_{REG4}	2.925	3.0	3.075	V	Over full current range CLK_ON ≥ V_{DIH}
Load current	I_{REG4}			20	mA	

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
Dropout voltage	V_{REG4DO}			200	mV	$I_{LOAD} = I_{REG4}$
Line regulation	$\Delta V_{REG4LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG4LDR}$			25	mV	1 mA ≤ I_{LOAD} ≤ I_{REG4}
Supply rejection	$PSRR_{REG4}$	60			dB	f_{IN} < 20 kHz
		40				f_{IN} = 250 kHz
Turn-on time	t_{REG4ON}			1	ms	
Output noise	e_{nREG4}		30	40	μV_{RMS}	10 kHz < f < 100 kHz
Peak short circuit current	I_{REG4SC}			TBD	mA	
Output capacitor	C_{OREG4}		TBD		µF	Specified by designer
REG5 (V_PLL, PLL)						
Output voltage	V_{REG5}	2.925	3.0	3.075	V	Over full current range PLL_ON ≥ V_{DIH}
Load current	I_{REG5}			35	mA	
Dropout voltage	V_{REG5DO}			200	mV	$I_{LOAD} = I_{REG5}$
Line regulation	$\Delta V_{REG5LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG5LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG5}
Supply rejection	$PSRR_{REG5}$	60			dB	f_{IN} < 100 kHz
		40				f_{IN} = 250 kHz
Turn-on time	t_{REG5ON}			2.25	ms	
Output noise	e_{nREG5}		30	40	μV_{RMS}	10 kHz < f < 100 kHz
Peak short circuit current	I_{REG5SC}			TBD	mA	
Output capacitor	C_{OREG5}		TBD		µF	Specified by designer
Output shutdown resistance	R_{SDREG5}		300		Ω	
REG6 (VCCA, Analog Baseband CODEC)						
Output voltage	V_{REG6}	2.6	2.7	2.8	V	Over full current range ANA_ON ≥ V_{DIH}
Load current	I_{REG6}			130	mA	
Dropout voltage	V_{REG6DO}			200	mV	$I_{LOAD} = I_{REG6}$
Line regulation	$\Delta V_{REG6LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG6LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG6}
Supply rejection	$PSRR_{REG6}$	60			dB	f_{IN} < 100 kHz
		40				f_{IN} = 250 kHz
Output noise	e_{nREG6}		30	40	μV_{RMS}	10 kHz < f < 100 kHz
Peak short circuit current	I_{REG6SC}			TBD	mA	
Output capacitor	C_{OREG6}		TBD		µF	Specified by designer
REG7 (V_PLLD, PLL Digital)						
Output voltage	V_{REG7}	1.8	1.9	2.0	V	Over full current range PLLD_ON ≥ V_{DIH}
Load current	I_{REG7}			10	mA	
Dropout voltage	V_{REG7DO}			200	mV	$I_{LOAD} = I_{REG7}$
Line regulation	$\Delta V_{REG7LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG7LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG7}
Supply rejection	$PSRR_{REG7}$	60			dB	f_{IN} < 100 kHz
Transient response		-1		+1	%	Within 10 µs of 1 mA to I_{REG7}
Peak short circuit current	I_{REG7SC}			TBD	mA	
Output capacitor	C_{OREG7}		TBD		µF	Specified by designer

PARAMETER	Symbol	Min	Typ	Max	Units	Conditions
REG8 (V_VOX, Voice-Band Analog)						
Output voltage	V_{REG8}	2.6	2.7	2.8	V	Over full current range VOX_ON ≥ V_{DIH}
Load current	I_{REG8}			50	mA	
Dropout voltage	V_{REG8DO}			200	mV	$I_{LOAD} = I_{REG8}$
Line regulation	$\Delta V_{REG8LNR}$			0.05	%	4 V ≤ V_BAT ≤ 6 V
Load regulation	$\Delta V_{REG8LDR}$			9	mV	1 mA ≤ I_{LOAD} ≤ I_{REG8}
Supply rejection	$PSRR_{REG8}$	60			dB	f_{IN} < 100 kHz
		40				f_{IN} = 250 kHz
Turn-on time	t_{REG8ON}			8	µs	
Turn-off time	$t_{REG8OFF}$			30	µs	
Output noise	e_{nREG8}		30	40	μV_{RMS}	10 kHz < f < 100 kHz
Peak short circuit current	I_{REG8SC}			TBD	mA	
Output capacitor	C_{OREG8}		TBD		µF	Specified by designer
Reset Controller						
Reset threshold 1	V_{RSTTH1}	2.55	2.63	2.70	V	
Reset threshold 2	V_{RSTTH2}	1.55	1.62	1.68	V	
Reset active period	t_{RSTP}	140		560	ms	
MR_N minimum pulse width	t_{RSTMR}	10			µs	
MR_N glitch immunity			100		ns	
MR_N internal pull-up resistance	$R_{RSTMRPU}$	10	20	30	kΩ	