UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEOUL SEMICONDUCTOR CO., LTD., SEOUL SEMICONDUCTOR, INC.,
CREE, INC., AND EVERLIGHT ELECTRONICS CO., LTD.,
Petitioners

v.

DOCUMENT SECURITY SYSTEMS, INC.,
Patent Owner

Case IPR2018-00333[1]
Patent 7,256,486 B2

PATENT OWNER'S DEMONSTRATIVE EXHIBITS

[1] Cree, Inc., who filed a Petition in IPR2018-01205, and Everlight Electronics Co., Ltd., who filed a Petition in IPR2018-01225, have been joined as petitioners in this proceeding.

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Seoul Semiconductor Co., Ltd., Seoul Semiconductor, Inc., Cree, Inc., and Everlight Electronics Co., Ltd.
v.
Document Security Systems, Inc.

IPR2018-00333[1] (USP 7,256,486 B2)

Oral Hearing Date: January 31, 2019

Before Hon. Sally C. Medley, Scott C. Moore, and Brent M. Dougal, Administrative Patent Judges

[1]Cree, Inc., who filed a Petition in IPR2018-01205, and Everlight Electronics Co., Ltd., who filed a Petition in IPR2018-01225, have been joined as petitioners in this proceeding.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Summary of Asserted Grounds and Prior Art

Ground	Reference[s]	Claims challenged
1	Rohm	1-3
1	Rohm and Kish	1-3
2	Matsushita and Edmond ’589	1-3

- Japanese Pat. Pub. 2003-17754, Jan. 17, 2003 (Ex. 1008) (“Rohm”)
- U.S. 5,376,580, Dec. 27, 1994 (Ex. 1010) (“Kish”)
- Japanese Pat. Pub. 2001-352102, Dec. 21, 2001 (Ex. 1009) (“Matsushita”)
- U.S. Patent 5,523,589, June 4, 1996 (Ex. 1011) (“Edmond ’589”)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Overview of Issues

Issue	Ground	Claims
Does Rohm Disclose or Suggest a Light Emitting Diode Having a Metallized ***Bottom*** Major Surface, and Does Kish Remedy Rohm's Shortcomings?	1	1
Does Rohm Disclose or Suggest a Light Emitting Diode Having a Metallized ***Top*** Major Surface, and Does Kish Remedy Rohm's Shortcomings?	1	2
Does Matsushita in view of Edmond '589 Disclose or Suggest a Light Emitting Diode Having a Metallized ***Bottom*** Major Surface?	2	1
Does Matsushita in view of Edmond '589 Disclose or Suggest a Light Emitting Diode Having a Metallized ***Top*** Major Surface?	2	2

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U.S. Patent No. 7,256,486 B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 7,256,486 B2**
(45) **Date of Patent: Aug. 14, 2007**

(54) **PACKAGING DEVICE FOR SEMICONDUCTOR DIE, SEMICONDUCTOR DEVICE INCORPORATING SAME AND METHOD OF MAKING SAME**

(75) Inventors: **Kong Weng Lee**, Penang (MY); **Kee Yean Ng**, Penang (MY); **Yew Cheong Kuan**, Penang (MY); **Gin Ghee Tan**, Penang (MY); **Cheng Why Tan**, Penang (MY)

(73) Assignee: **Avago Technologies ECBU IP (Singapore) Pte. Ltd.**, Singapore (SG)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/608,605**

(22) Filed: **Jun. 27, 2003**

(65) **Prior Publication Data**

US 2004/0262738 A1 Dec. 30, 2004

(51) **Int. Cl.**
H01L 29/22 (2006.01)

(52) **U.S. Cl.** **257/690**; 257/784; 257/690

(58) **Field of Classification Search** 257/690, 257/784, 700, 689, 774, 783, 99, 100; 361/707, 361/718, 719, 706, 717, 720
See application file for complete search history.

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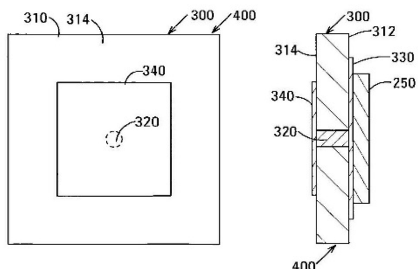
Primary Examiner—Sara Crane

(57) **ABSTRACT**

The packaging device includes a substrate, a mounting pad, a connecting pad and an interconnecting element. The substrate is substantially planar and has opposed major surfaces. The mounting pad is conductive and is located on one of the major surfaces. The connecting pad is conductive and is located on the other of the major surfaces. The conductive interconnecting element extends through the substrate and electrically interconnects the mounting pad and the connecting pad. The packaging device has a volume that is only a few times that of the semiconductor die and can be fabricated from materials that can withstand high-temperature die attach processes. The packaging device can be configured as the only packaging device used in the semiconductor device or as a submount for a semiconductor die that requires a high-temperature die attach process.

6 Claims, 8 Drawing Sheets



1. A semiconductor device, comprising:
a substantially planar substrate having opposed major surfaces;
an electrically conductive mounting pad located on one of the major surfaces of the substrate;
a light emitting diode (LED) having a metallized bottom major surface that is mounted on the electrically conductive mounting pad, the metallized bottom major surface comprising one of an anode and a cathode of the LED;
a first electrically conductive connecting pad located on the other of the major surfaces of the substrate; and
a first electrically conductive interconnecting element extending through the substrate and electrically interconnecting the mounting pad and the first electrically conductive connecting pad.

2. The semiconductor device of claim **1**, further comprising:
an electrically conductive bonding pad located on the one of the major surfaces of the substrate;
a bonding wire extending between a metallized top major surface of the LED and the electrically conductive bonding pad;
a second electrically conductive connecting pad located on the other of the major surfaces of the substrate; and
a second electrically conductive interconnecting element extending through the substrate and electrically interconnecting the bonding pad and the second connecting pad.

3. The semiconductor device of claim **2** wherein the metallized top major surface comprises a first electrode of the LED and the metallized bottom major surface comprises a second electrode of the LED.

Exhibit 1001, p. 1, 12:6-39

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